Virtualizing Memory

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• Submit your project team questionnaire by this Friday!
• Start researching on the project topic and form a plan
• Project proposal due on 1/24!

• No class next Monday (MLK Day)
Recap: Architecture of VMware’s Binary Translation

Translator

Guest Binary Code

Translation Cache

Callouts

CPU Emulation Routines

TC Index
Recap: Hardware-Assisted Virtualization

VMX Mode Transition with Intel VT-x

- VM exit/entry (to/from root mode)
  - Registers and address space swapped in one atomic operation
  - Guest- and host-states saved and loaded to VMCS during transitions
- Whenever possible, sensitive instructions only affect states within the VMCS instead of always trapping (VM exit)

- VM exit
  - `vmcall` instruction
  - EPT page faults (more next lecture)
  - Interrupts
  - Some sensitive instructions (configured in VMCS)

- VM entry
  - `vmlaunch` instruction: enter with a new VMCS
  - `vmresume` instruction: enter for the last VMCS
- Typical `vm exit/enter` tasks ~200 cycles on modern CPU

Image source: https://www.anandtech.com/show/2480/9
Software Binary Translation vs. Hardware-Assisted Virtualization

- Software binary translation wins in:
  - Trap elimination
  - Emulation speed
  - Callout avoidance

- Hardware-assisted virtualization wins in:
  - Code density
  - Precise exceptions
  - Syscalls

Figure 4. Virtualization nanobenchmarks.
Question

• With hardware virtualization extensions (e.g., Intel VT), do we still need binary translation? Why or why not?
Virtualization Approach 5: Direct Execution with Paravirtualization

- Full virtualization (no guest OS modification)
  - Tricky and has performance overhead

- Para-virtualization: modified guest OS
  - Change (rewrite) guest OS to remove sensitive but unprivileged instructions and to use other tricks to make virtualization faster
    - Guest OS works with hypervisor (i.e., knows that it is a VM) and has some exposure to hardware
    - e.g., guest OS informs hypervisor of page table changes
    - e.g., guest OS directly calls hypervisor on system calls (hypercalls)

- Guest applications are still unmodified

- Pros and Cons?
Other Virtualization Approaches

- **Container:** Essentially just a group of processes with some additional features (isolated namespace, isolated resources, etc.) (e.g., Docker)

- **Unikernel:** LibraryOS designed for a single application, running on hypervisor (as a VM) or host OS (as a process)

- **Sandboxing:** Limit what the applications (and libOS) can do (e.g., gVisor)

- **Language-based:** Running applications written in a high-level language on language runtimes (e.g., JVM)
Virtualization Approaches Summary

- Hosted interpretation
  - Interpret each instruction, super slow (e.g., Virtual PC on Mac)

- Direct execution with trap-and-emulate
  - Requires a virtualizable processor and only works for the same architecture

- Direct execution with binary translation
  - Works with non-virtualizable processor, but implementing VMM is tricky

- Direct execution with hardware-assisted virtualization
  - Needs new generation of hardware (which is the norm now), mode switching is still not optimized

- Direct execution with paravirtualization
  - Good performance and works with non-virtualizable processors, but require guest OS changes

- OS-level virtualization, library-level, language (app)-level, unikernels, etc.
  - More lightweight and faster to start, but less secure
Outline

• Software-based memory virtualization
• Hardware-assisted memory virtualization
• Memory management
  • Reclaiming
  • Sharing
  • Allocation

Acknowledgment: some slides from Carl Waldspurger’s OSDI’02 presentation
Review: Regular Virtual Memory System

Virtual address space [0, MAX]

Virtual address

VPage # | offset

VPage # | PPage # | ...

VPage # | PPage # | ...

VPage # | PPage # | ...

TLB

Hit

Miss

Real page table

PPage # | offset

Physical address

Page-map L4 base addr (CR3)

Page-map L4 table

Page-dir-ptr table

Page-directory table

Page-table entry

Physical page frame number

Physical address

Page offset

Main memory

Page table

Page-directory table

Page-dir entry

Page-dir-ptr entry

Page-map entry

Page-map L4 table

Page-dir-ptr entry

Page-directory table

Page-table entry

Physical page frame number

Page offset

Main memory

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Review: Software-controlled TLB

- On a TLB hit, MMU checks the valid bit
  - If valid, perform address translation
  - If invalid (e.g. page not in memory), MMU generates a page fault
    - OS performs page fault handling
    - Restart the faulting instruction

- On a TLB miss, HW raises exception, *traps to the OS*
  - OS parses page table and loads PTE into TLB
    - Needs to replace if TLB is full
  - Same as in a hit...
Review: Hardware-controlled TLB

• On a TLB hit, MMU checks the valid bit
  • If valid, perform address translation
  • If invalid (e.g. page not in memory), MMU generates a page fault
    • OS performs fault handling
    • Restart the faulting instruction

• On a TLB miss
  • MMU parses page table and loads PTE into TLB
    • Needs to replace if TLB is full
  • Same as hit …
Virtualizing Memory

• Extra level of memory addressing

Figure B.4: VMM Memory Virtualization
Virtualizing Memory

• TLB miss flow with software-managed TLB

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### Process
1. Load from memory:
   TLB miss: Trap

2. OS TLB miss handler:
   Extract VPN from VA;
   Do page table lookup;
   If present and valid:
   get PFN, update TLB;
   Return from trap

3. Resume execution
   (@PC of trapping instruction);
   Instruction is retried;
   Results in TLB hit

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### Operating System
1. Load from mem
   TLB miss: Trap

2. VMM TLB miss handler:
   Call into OS TLB handler
   (reducing privilege)

3. OS TLB miss handler:
   Extract VPN from VA;
   Do page table lookup;
   If present and valid,
   get PFN, update TLB

4. Trap handler:
   Unprivileged code trying to update the TLB;
   OS is trying to install
   VPN-to-PFN mapping;
   Update TLB instead with
   VPN-to-MFN (privileged);
   Jump back to OS
   (reducing privilege)

5. Return from trap

6. Trap handler:
   Unprivileged code trying to return from a trap;
   Return from trap

7. Resume execution
   (@PC of instruction);
   Instruction is retried;
   Results in TLB hit

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**Figure B.5: TLB Miss Flow without Virtualization**

**Figure B.6: TLB Miss Flow with Virtualization**
Difficulty in Virtualizing Hardware-Managed TLB

- Hardware-managed TLB
  - Hardware does page table walk on each TLB miss
  - and fills TLB with the found PTE

- Hypervisor doesn’t have chance to intercept on TLB misses

- Solution-1: shadow paging
- Solution-2: direct paging (para-virtualization) (later this quarter if have time)
- Solution-3: new hardware
Shadow Paging

Guest VM

CR3

VPN

PPN

MPN

pmap

SPT

GPT

PA

CR3

0

MPS

pmap

MPN

CR3
guest OS $\rightarrow$ CR3 $\rightarrow$ PA of PT $\rightarrow$ PTE (LUT $\rightarrow$ PA)

$\rightarrow$

vCR 3 $\rightarrow$ PA of gPT

$\rightarrow$

RO

CR3

$\rightarrow$

VA - PA

Shadow
Set Up Shadow Page Table

1. VMM intercepts guest OS setting the virtual CR3 (a sensitive operation)
2. VMM iterates over the guest page table, constructs a corresponding shadow page table
3. In shadow PT, every guest physical address is translated into host physical address (machine address)
4. Finally, VMM sets the real CR3 to point to the shadow page table
Set Up Shadow Page Table

```python
set_cr3 (guest_page_table):
    for VPN in 0 to 220
        if guest_page_table[VPN] & PTE_P /* PTE_P: valid bit */
            PPN = guest_page_table[VPN]
            MPN = pmap[PPN]
            shadow_page_table[VPN] = MPN | PTE_P
        else
            shadow_page_table = 0
    CR3 = PHYSICAL_ADDR(shadow_page_table)
```
Question

• Assume that:
  • There are 10 VMs running on a machine
  • Each VM contains 10 applications

• Q: How many shadow page tables in total?
  • Shadow page tables are per application
  • Guest page tables are per application
  • pmaps are per VM

10 pmaps
What if Guest OS Modifies Its Page Table?

• Should not allow it to happen directly
  • Since CR3 is now pointing to the shadow page table
  • Need to synchronize the shadow page table with guest page table

• VMM needs to intercept when guest OS modifies page table, and updates the shadow page table accordingly
  1. Mark the guest table pages as read-only (by setting the corresponding PTEs’ permission bits in the shadow page table)
  2. If guest OS tries to modify its page tables, it triggers page fault
  3. VMM handles the page fault by updating shadow page table
Dealing with Page Faults

- When page fault occurs, traps to VMM

- If present bit is 0 in the guest page table entry, guest OS needs to handle the fault (VMM forwards the fault to guest OS)
  - Guest OS load page from virtual disk to guest physical memory and sets present bit to 1
  - Guest OS returns from page fault, which traps into VMM again
  - VMM sees that present is 1 in guest PTE and creates entry in shadow page table
  - VMM returns from the original page fault

- If present is 1: guest OS thinks page is present (but VMM may have swapped it out), VMM handles transparently
  - VMM locates the corresponding physical page, loads it in memory if needed
  - VMM creates entry in shadow page table
  - VMM returns from the original page fault
What if a Guest App Access its Kernel Memory?

- How do we selectively allow / deny access to kernel-only pages?
- One solution: split a shadow page table into two tables
  - Two shadow page tables, one for user, one for kernel
  - When guest OS switches to guest applications, VMM will switch the shadow page table as well, vice versa
Two Memory Views of Guest VM

- **Kernel space**
  - When guest OS is running
  - User space
  - User access

- **User space**
  - When application is running
  - No user access
The Same Question

• Assume that:
  • There are 10 VMs running on a machine
  • Each VM contains 10 applications

• Q: Now, how many shadow page tables in total?
Pros and Cons of Shadow Paging?
Outline

- Software-based memory virtualization
- Hardware-assisted memory virtualization
- Memory management
  - Reclaiming
  - Sharing
  - Allocation
Hardware-Assisted Memory Virtualization

• Hardware support for memory virtualization

  • Intel EPT (Extended Page Table) and AMD NPT (Nested Page Table)

  • EPT: a per VM table translating PPN -> MPN, referenced by EPT base pointer

  • EPT controlled by the hypervisor, guest page table (GPT) controlled by guest OS (both exposed to hardware)

  • Hardware directly walks GPT + EPT (for each PPN access during GPT walk, needs to walk the EPT to determine MPN)

• No VM exits due to page faults, INVLPG, or CR3 accesses
EPT Translation: Details
EPT Increases Memory Access

One memory access from the guest VM may lead up to **20 memory accesses**! 

sPA: machine address
nCR3: root of EPT table
nL_k: EPT table level
Pros and Cons of EPT?
Outline

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Reclaiming Memory

- ESX (and other hypervisors) allow overcommitment of memory
  - Total memory size of all VMs can exceed actual machine memory size
  - ESX must have some way to reclaim memory from VMs (and swap to disk)
Reclaiming Memory

- Traditional: add transparent swap layer
  - Requires “meta-level” decisions: which page from which VM to swap
  - Best data to guide decisions known only by guest OS
  - Guest and meta-level policies may clash, resulting in *double paging*

- Alternative: implicit cooperation
  - Coax guest OS into doing its own page replacement
  - Avoid meta-level policy decisions
Ballooning

Guest OS

deflate balloon (− pressure)

inflated balloon (+ pressure)

Guest OS

may page out to virtual disk

guest OS manages memory implicit cooperation

may page in from virtual disk

special driver

hypervisor
Ballooning Details

- Guest drivers
  - Inflate: allocate pinned PPNs; backing MPNs reclaimed
  - Use standard Windows/Linux/BSD kernel APIs

- Performance benchmark
  - Linux VM, memory-intensive dbench workload
  - Compare 256 MB with balloon sizes 32 - 128 MB vs. static VMs
  - Overhead 1.4% - 4.4%

Figure 2: Balloon Performance. Throughput of single Linux VM running dbench with 40 clients. The black bars plot the performance when the VM is configured with main memory sizes ranging from 128 MB to 256 MB. The gray bars plot the performance of the same VM configured with 256 MB, ballooned down to the specified size.
Memory Sharing

- Motivation
  - Multiple VMs running same OS, apps
  - Collapse redundant copies of code, data, zeros
- Transparent page sharing
  - Map multiple PPNs to single MPN (copy-on-write)
  - Pioneered by Disco, but required guest OS hooks
- New twist: content-based sharing
  - General-purpose, no guest OS changes
  - Background activity saves memory over time
Page Sharing: Scan Candidate PPN

hash page contents

...2bd806af

hint frame

Hash: ...06af
VM: 3
PPN: 43f8
MPN: 123b
Page Sharing: Successful Match
Question

- What is the benefit of keeping a "hint" entry for each scanned (but unshared) page (as compared to not maintaining anything for the page)
Real-World Page Sharing Results

<table>
<thead>
<tr>
<th>Workload</th>
<th>Guest Types</th>
<th>Total</th>
<th>Saved</th>
<th>%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Corporate IT</td>
<td>10 Windows</td>
<td>2048</td>
<td>673</td>
<td>32.9</td>
</tr>
<tr>
<td>Nonprofit Org</td>
<td>9 Linux</td>
<td>1846</td>
<td>345</td>
<td>18.7</td>
</tr>
<tr>
<td>VMware</td>
<td>5 Linux</td>
<td>1658</td>
<td>120</td>
<td>7.2</td>
</tr>
</tbody>
</table>

Corporate IT – database, web, development servers (Oracle, Websphere, IIS, Java, etc.)
Nonprofit Org – web, mail, anti-virus, other servers (Apache, Majordomo, MailArmor, etc.)
VMware – web proxy, mail, remote access (Squid, Postfix, RAV, ssh, etc.)
Conclusion

- Software and hardware solutions for memory virtualization both have pros and cons

- More things to take care of besides the basic mechanism of memory virtualization
  - Allocation, sharing, overcommitment and reclamation