Richard Strong

Experience

2006–2013 **Graduate Researcher under Tajana S. Rosing**, *Univ. of Ca.*, San Diego.

- *Mordia*: created a Linux module to support and debug a prototype microsecond optical switch, to evaluate TCP/IP and data center applications on optical networks
- *MAPG*: created and evaluated a memory access power gating technique for processors
- *Fast thread migration*: reduced Linux process migration overhead by a half or more
- *CMP Scheduling*: leveraged thread migration between cores to improve processor longevity. Created a fast, long-term simulation framework for a 16-core CMP.
- *McPAT*: helped create, integrate, and evaluate the McPAT power model for GEM5
- *Cluster Administrator*: setup a virtualized, pxeboot, SGE, 20 node cluster

2009–2010 **Teaching Assistant**, *Univ. of Ca.*, San Diego.
CSE15L, Scientific Debugging

2008–2009 **Intern under Jeffrey Mogul**, *HP Labs*, Palo Alto, CA.
Researched fast thread migration, full-system simulation, and core asymmetry

2008 **Teaching Assistant**, *Univ. of Ca.*, San Diego.
CSE141, Introduction to Computer Architecture

2007 **Intern under Radhika Thekkath**, *MIPS Technologies Inc.*, Mountain View, CA.
Ported the GEM5 simulator to boot Linux on the MIPS ISA

2006 **Software Engineer under Nolan Bushnell**, *Uwink Inc.*, Van Nuys, CA.
Python and LAMP development for a digital restaurant

2005 **Intern under Steven Flanagan**, *City of Hope*, Duarte, CA.
Performed variation studies of microarray image analysis software

Education

2009–2013 **PhD**, *University of California*, San Diego.
Computer Science (Computer Engineering)

2006–2009 **M.S.**, *University of California*, San Diego.
Computer Science

2002–2006 **B.S.**, *University of California*, Los Angeles.
Computer Science and Engineering (Summa Cum Laude)

1999–2002 **Highschool**, *Redlands High School*, Redlands, CA.
(Valedictorian)

Computer skills (* Denotes Most Familiarity)

Low-Level Languages	C/C++*, Java, Swig, MIPS Assembly	High-Level Languages	Python*, Bash*, R, Visual Basic, Scheme, Matlab, Perl, Lisp, Prolog
Web Design	PHP, Apache, Ruby on Rails, XHTML, CSS, XML, JavaScript	Storage Systems	Redis*, MySQL*, HDFS, SQL, Samba, Microsoft Access
Cluster Experience	SGE*, Hadoop, PBS, LSF, TFTP, DHCP, PXEBOOT, NFS, vSwitch	Hardware Design Tools	M5*, GEM5*, McPAT, Wattch, VHDL, HDL, Xilinx, MaxPlus Studio

San Diego – California
(951)267-9977 • *r.d.strong@gmail.com* • *cseweb.ucsd.edu/ rstrong*

Misc. Skills	LaTeX*, Gimp, Photoshop, Inkscape, Matplotlib, Gnuplot, Microsoft Suite	OS Experience	Ubuntu, Debian, Redhat, Gentoo, Mac OSX, Windows 3.1–8, Solaris
Version Ctrl.	Mercurial*, Git, Subversion, CVS		

Awards and Achievements

2006 **Academic Award**, *University of California*, Los Angeles.
The Outstanding Bachelor of Science & Engineering Award recognizes GPA, creativity, research, and community service

2002-2006 **Dean's Honor List**, *University of California*, Los Angeles.
The Dean's Honor List recognizes high GPA while taking a full load each quarter

2002-2006 **Lyndon Byrd Scholarship**, *University of California*, Los Angeles.
The Lyndon Byrd Scholarship is a four year merit scholarship pendant on maintenance of high academic standing with a full load each quarter

2007–2010 **Open Source Development**, `www.gem5.org`.
Participated in the open source development of GEM5 including: McPAT power model integration, full-system support for the MIPS ISA, simpoints, checkpoint support, and general bug fixes.

Interests

Data Centers	Servers, Processors, Memory, Disks	Networks	Optical, Electrical, Scalability
OS	Linux, Modules, Traffic Shaping	Scheduling	Multi-Cores, Switches
Virtualization	KVM, Xen, Virtualbox, VMWare	Open Source	GEM5, McPAT
Distributed Systems	Big data, Scalability, Fault Tolerance, MapReduce	Machine learning	Online & Offline

Publications

[1] R. Strong. *Low-Latency Techniques for Improving System Energy Efficiency.* PhD thesis, University of California at San Diego, 2013.

[2] G. Porter, R. Strong, N. Farrington, A. Forencich, P. Chen-Sun, T. Rosing, Y. Fainman, G. Papen, and A. Vahdat. Integrating Microsecond Circuit Switching into the Data Center. In *Proc. SIGCOMM*, 2013.

[3] A. B. Kahng, S. Kang, T. S. Rosing, and R. Strong. Many-Core Token-Based Adaptive Power Gating. *IEEE TCAD*, 2013.

[4] K. Jeong, A. B. Kahng, S. Kang, T. S. Rosing, and R. Strong. MAPG: Memory Access Power Gating. In *Proc. DATE*, pages 1054–1059, 2012.

[5] A. B. Kahng, S. Kang, T. S. Rosing, and R. Strong. TAP: Token-Based Adaptive Power Gating. In *Proc. ISLPED*, pages 203–208, 2012.

[6] R. Strong, J. Mudigonda, J. C. Mogul, N. Binkert, and D. Tullsen. Fast Switching of Threads Between Cores. *SIGOPS OSR*, 43(2):35–45, 2009.

[7] A. K. Coskun, R. Strong, D. M. Tullsen, and T. S. Rosing. Evaluating the Impact of Job Scheduling and Power Management on Processor Lifetime for Chip Multiprocessors. In *Proc. SIGMETRICS*, pages 169–180, 2009.

[8] R. Strong, J. Mudigonda, J. C. Mogul, and N. Binkert. Initial Experiments in Visualizing Fine-Grained Execution of Parallel Software Through Cycle-Level Simulation. Technical Report at HP Labs, 2008.

[9] S. Li, J. Ahn, R. Strong, J. B. Brockman, D. M. Tullsen, and N. P. Jouppi. McPAT: An Integrated Power, Area, and Timing Modeling Framework for Multicore and Manycore Architectures. In *Proc. MICRO*, pages 469–480, 2009.