Meenakshi Sundaram Bhaskaran

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RESEARCH

My research involves operating systems and hardware optimizations required to effeciently utilize novel stroage technology. Presently, I am working on building presistent block device cache on Moneta.

EDUCATION

University of California, San Diego
In-Progress PhD**,** Computer Science **Sept 2010 – Present**

College of Engineering, Guindy, Anna University, India
Bachelor of Engineering, Electrical & Electronics Engineering **Jul 2003-Apr 2007**

COURSES

Design and Analysis of Algorithm, Principles of Database Systems, Distributed Computing and Systems, Graduate Computer Architecture, Graduate Operating System, Advanced Micro-architecture, Parallel Computer Architecture, VLSI Integrated Computing Circuitry, Advanced Compiler Design

TECHNICAL SKILLS

C, Verilog, Python

WORK EXPERIENCE

Teaching Assistant, UCSD **Jan 2011 – March 2011/Jan 2012 – Present**

Assist students of CSE141L, Computer Architecture lab in course project, including support for Xilinx ISE/Quartus and Verilog programming, evaluating work and grading labs. Also design labs that eventually makes the students build a 5 stage MIPS pipeline.

Intern, Samsung Information Systems America **June 2011 – August 2011**

Explored the application of low latency, high-density non-volatile memory in **real time distributed stream processing system**. Designed and developed new storage manager in **Java for Yahoo! S4** distributed stream system. Defined a dynamic storage management policy to exploit the physical properties of DRAM-PCM-SSD hybrid memory hierarchy.

Product Application Engineer, SanDisk Corp **Aug 2007 - Aug 2010**

Debugged application, signal and protocol issues with Compact Flash and Memory Stick products. Document issues and present problem analysis reports to product development team.

Developed a HW/SW host simulation platform for Memory Stick Flash memory cards on Xilinx Spartan3A-DSP board with MircoBlaze microprocessor. *Reduced product development time* by enabling application level testing of prototypes.

Accelerated debugging using Python to generate test scripts from protocol traces for reproducing MemoryStick host behavior on an in-house test board

Co-developed an optimized algorithm in C for traversing Microsoft File Allocation Table (FAT) directory tree.

Played key role in securing design wins for *SanDisk PATA SSD at Computex'08*. Involved in the study of usage models of netbooks and I/O access. Built python scripts to run regression test and extract reports.

Developed the backend test application in C for executing configurable regression test on memory devices. Implemented an application level *thread synchronization primitive* that resolves concurrency and avoids deadlock.

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RESEARCH EXPERIENCE

Research Assistant, Non-Volatile Systems Laboratory, UCSD **Sept 2010-present**

Advisor: Prof. Steven Swanson

Worked with *Monenta PCIe based FPGA emulation* platform for Non-volatile memory technology. Designed a modular memory interface for Moneta to provide unified interface for different memory technologies.

Developed a **Linux kernel device** driver in C. The device driver is responsible for performing hybrid NAND Flash Translation operations for the Moneta System. Implemented a runtime optimized kernel level locking primitive to enable thread-safe kernel space operation.

Created a NAND emulator in Verilog that integrates with the Moneta Architecture.

Research Assistant, San Diego Super Computer Center, La Jolla **April 2011 – June 2011**

Advisor: Dr.Robert Sinkovits

Worked on Gordon Supercomputer a data intensive system built using flash based SSD.

Using **xdd and fio benchmarking tools** characterized the performance of SSD storage array. Accelerated the measurement and the analysis of results using dynamically configurable python scripts for launching tests and generating reports.

Research Associate, ANna University SATellite (ANUSAT) Group, Chennai **Nov 2005-Apr2007**

Advisor: Dr. Umamaheswari

ANUSAT, India's first university satellite program developed jointly with India Space Research Organization (ISRO) and launched on April 20, 2009.

Designed and developed a state observer for a DC-DC buck/boost converter using Xilinx-Spartan 3 FPGA

PROJECTS

Port memcached from C to Cyclone for compilers project. Cyclone is a safe dialect of C. **Sept 2011**

Design of a data and instruction cache L1 prefetch unit in a simple processor memory reference simulator. The markov prefetcher was ranked 6th best in the graduate class of 90 **Sept 2010**

Designed the architecture and organization of a control system processor and implemented a subset of the same on a Spartan-3 FPGA. **Apr 2006 -Apr 2007**

AWARDS

Student Manager Workshop and Guest lectures organization committee of Kurukshetra'07, a technical festival of Anna University and first student-organized event of India to be bestowed with patronage from UNESCO.

Developed an artificial intelligence program in C++ for Mission Mars, a programming competition organized at Kshitij'05 - technical festival of IIT, Kharagpur. The code was judged one among the top 10 codes in the country.

Designed and fabricated a mine detector robot for National level robotics competition conducted at Shaastra 2005 a technical festival of IIT-Madras

Ranked among the top 0.2% of 100,000 students in the Tamil Nadu Professional Course Entrance Examination held in March 2003.