ILP/SAT/SMT-based Techniques for Layout Design Automation

Routability Analysis, Diagnosis, and Optimization

Korea Test Conference 2020

UCSD VLSI CAD Group

Chung-Kuan Cheng

OUTLINE

- ***Introduction***
- ***Ch.0) Formulation Background***
- ***Ch.1) Routability Analysis (ILP/SAT)***
- ***Ch.2) Routability Diagnosis (SAT)***
- ***Ch.3) Standard Cell Synthesis (SMT)***
- ***Future***

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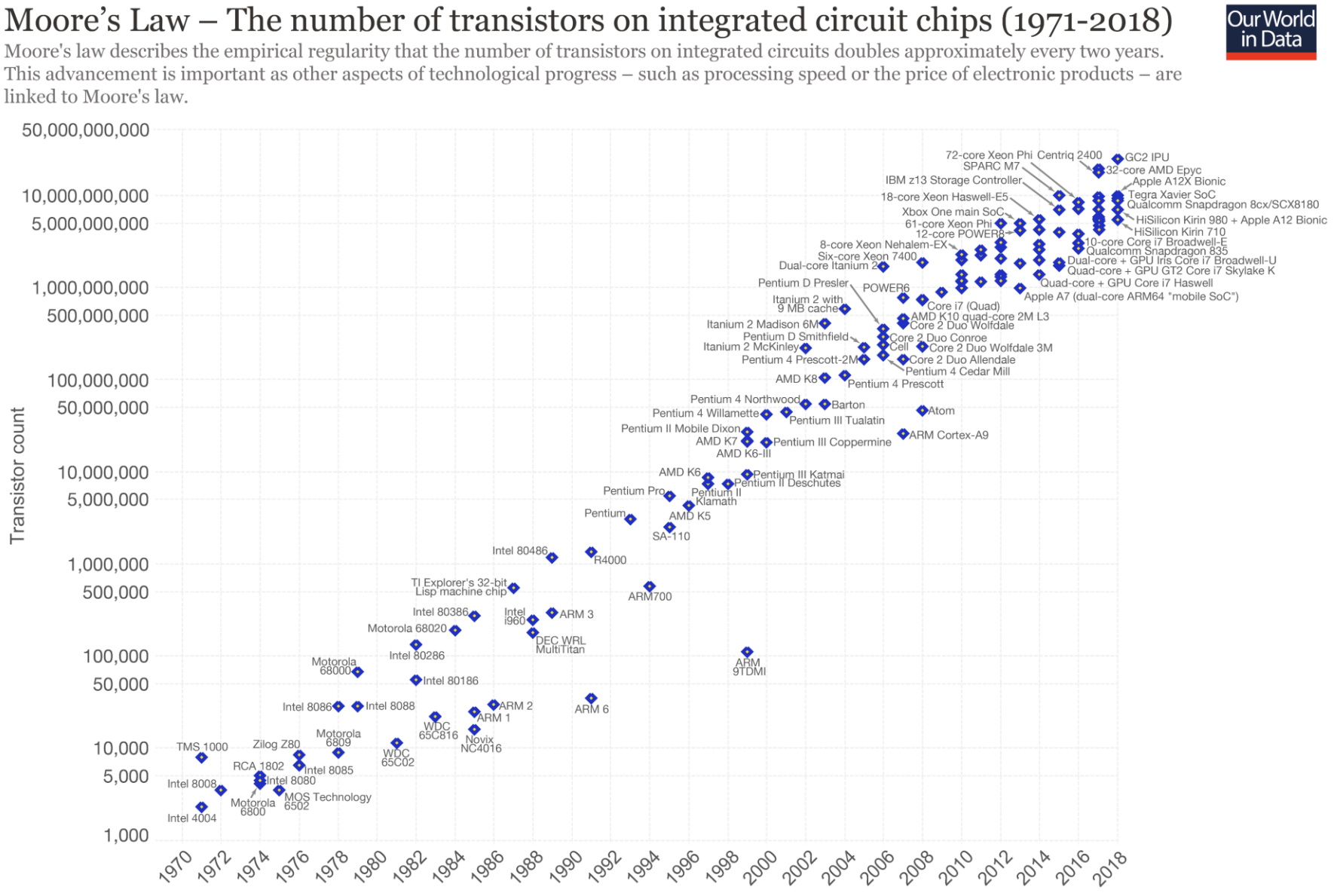
Moore in1965:

The complexity for minimum component costs has increased at a rate of roughly a factor of two/yr.



Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

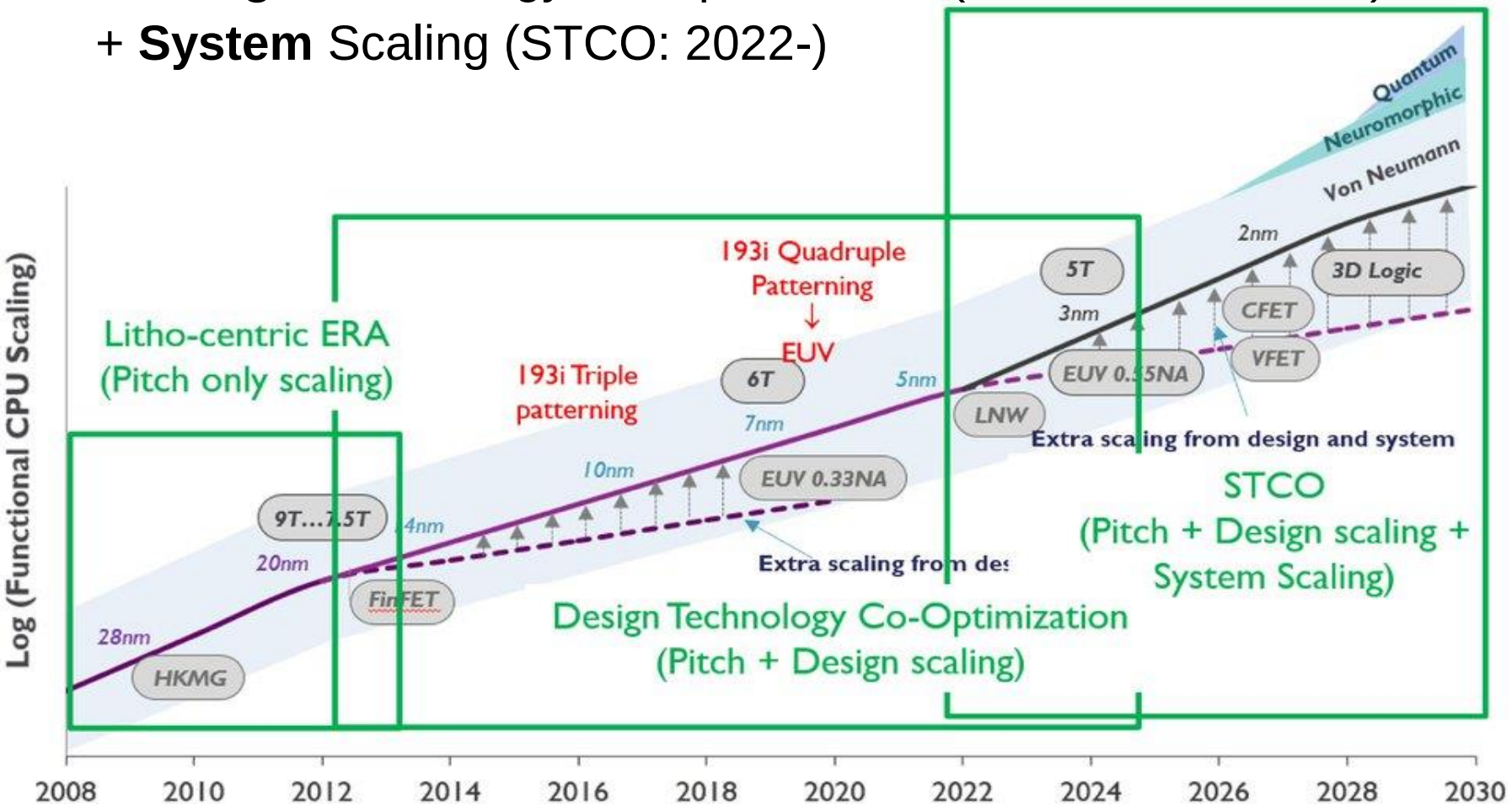
MOORE'S LAW

Scaling Methods:

Pitch only (-2013)

\+ **Design** Technology Co-Optimization (DTCO: 2012-2025)

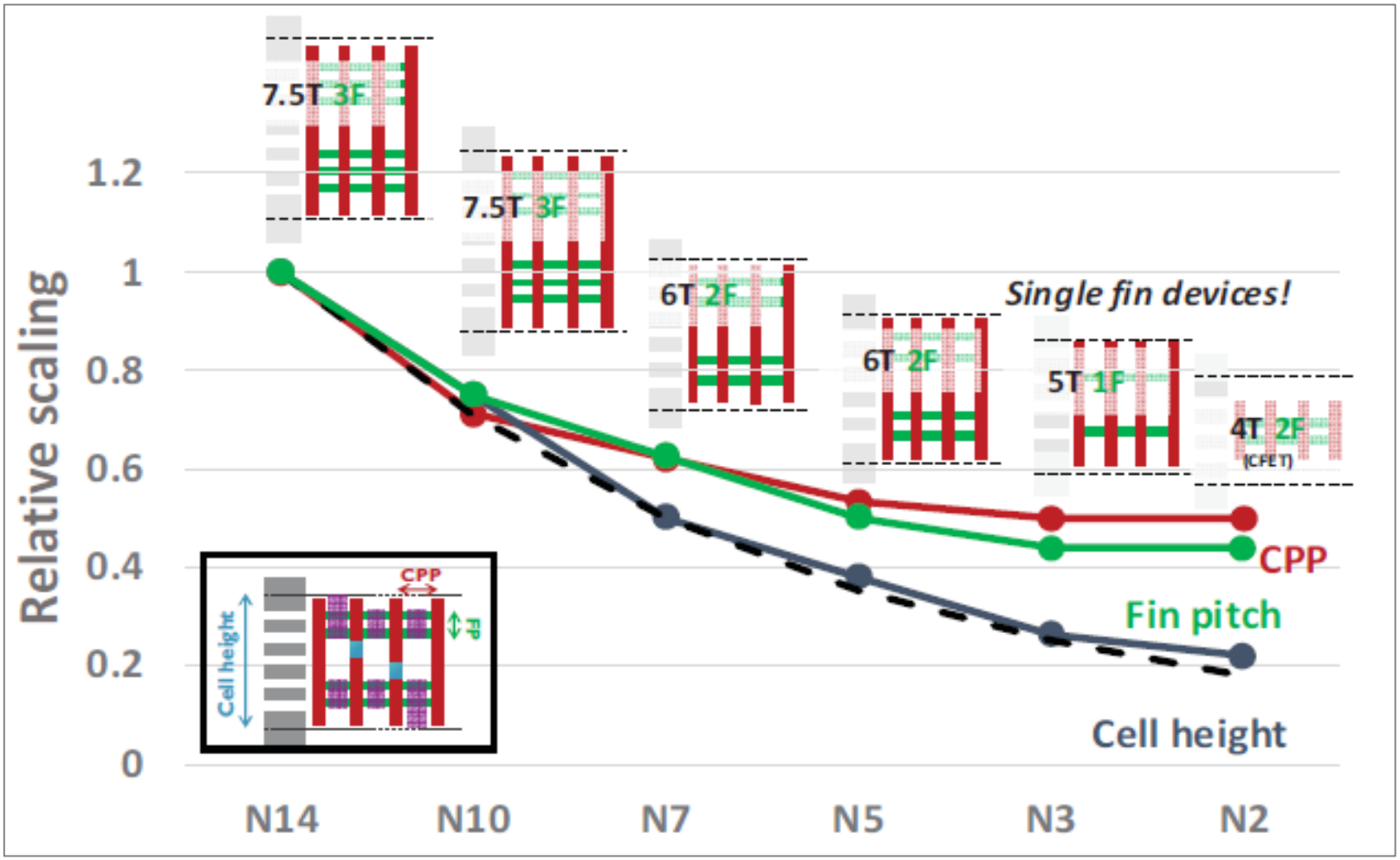
\+ **System** Scaling (STCO: 2022-)



[S. M. Y. Sherazi et al., "Standard-cell design architecture options below 5nm node: The ultimate scaling of FinFET and Nanoshee,"keynote, Proc. SPIE, 2019]

MOORE'S LAW: DESIGN TECHNOLOGY CO-OPTIMIZATION

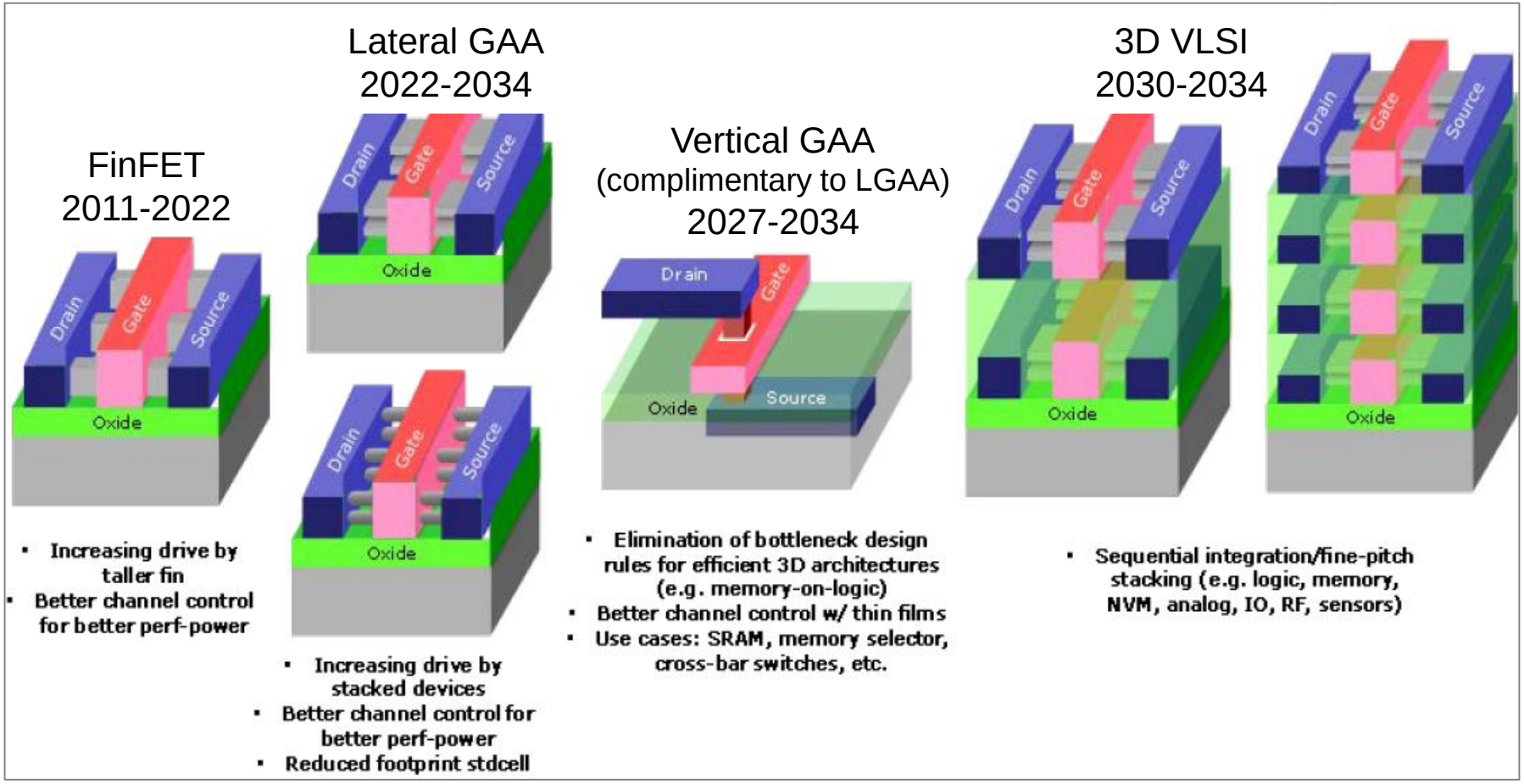
- Poly pitch scaling becomes challenging
- Horizontal track reduction decreases cell height
- Layout design rule exploration



Source: https://www.imec-int.com/en/imec-magazine/imec-magazine-november-2018/the-supervia-a-promising-scaling-booster-for-the-sub-3nm-technology-node

MOORE'S LAW: SYSTEM TECHNOLOGY CO-OPTIMIZATION

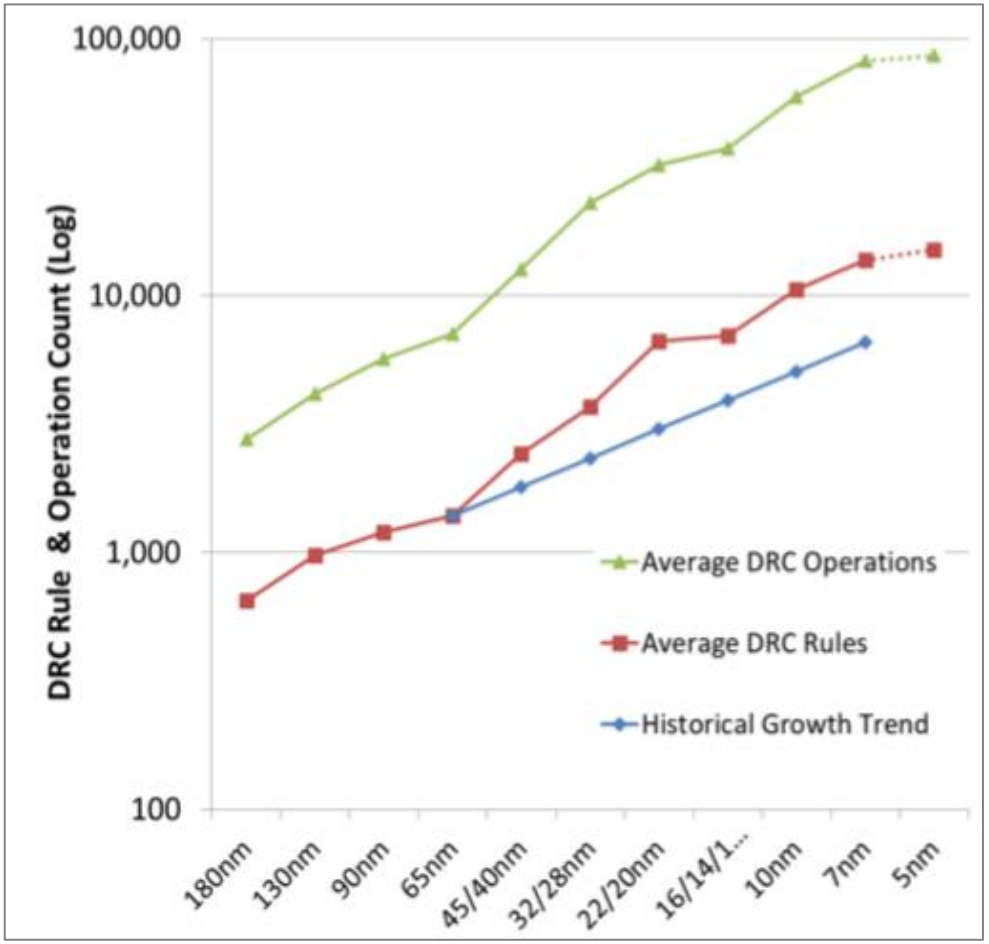
2.5D/3D fine-pitch assembly + stacking



Change in the MOSFET device architecture from the 2D planar through 2.5D FinFets to 3D monolithic VLSI.

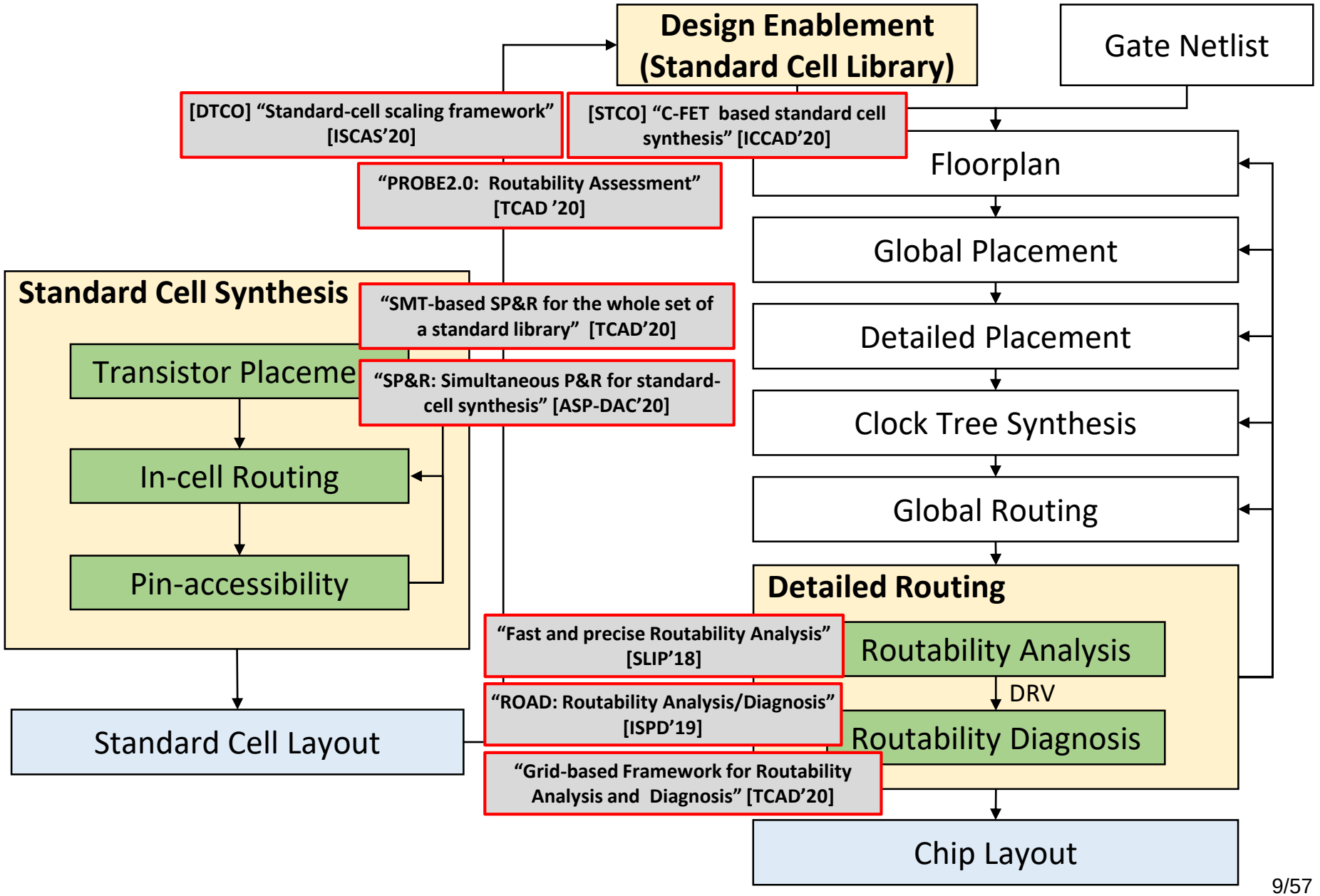
CHALLENGES

- **Complex Design Rules**
  - The number of rules grows from 100s to 10,000.
- **Reduced Routing Resources**
  - The number of horizontal tracks drops from 12 to 4
- **Fidelity of Exploration**
  - Optimality of solution
  - Precision of sensitivity derivation
- **Complexity of Derivation**
  - VLSI layout problems are NP complete



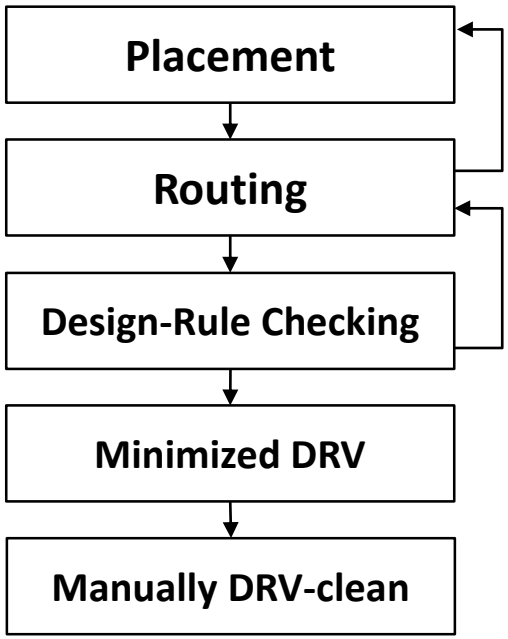
[*Design Rule Complexity Rising , semiengineering.com*]

Our Contributions in PD Flow



Our Approaches for PD Problems

**CSP : Constraint Satisfaction Problem*



Majority in physical design community	*Our Approach (Reasonable Scalability)*
Sequential	Simultaneous (Concurrent)
↓	↓
Iteration / heuristic	One-time/Exact solving of CSP*
↓	↓
Limited Optimality	Optimized Solution

Complexity is exploding.. How?

1) Matured fast reasoning methods (SAT/SMT): Boolean-based fast feasibility (Satisfiability)

2) Simplified P&R graph (e.g. on-grid) / Encoded constraints: Refined Variables / Clauses

3) Logical Pruning to cut the search space: More Constrained, Faster Reasoning

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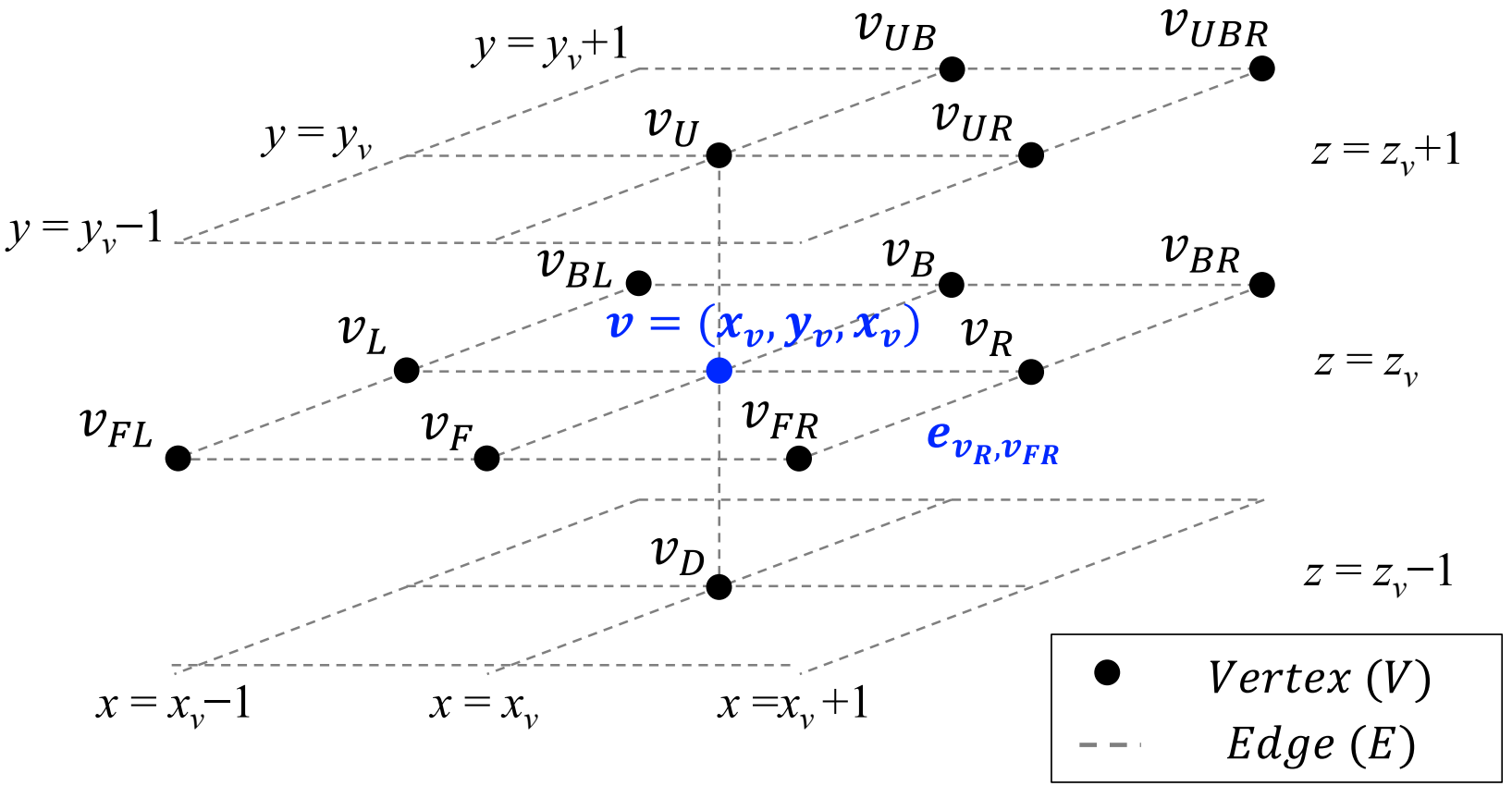
ON-GRID & UNIDIRECTIONAL ROUTING GRAPH

- A multiple metal layered routing graph *G = (V,E)*
  - Available routing resource: horizontal/vertical tracks, inter-layer vias
  - Process resolution in sub-10nm → Grid-based Unidirectional Routing
- Grid-based sub-10nm technologies fit Boolean-based SAT/ILP techniques.



BINARIZED CFC (COMMODITY FLOW CONSERVATION)

$$f_m^n(v) + \sum_{u \in a(v)} f_m^n(u, v) - \sum_{u \in a(v)} f_m^n(v, u) = 0$$

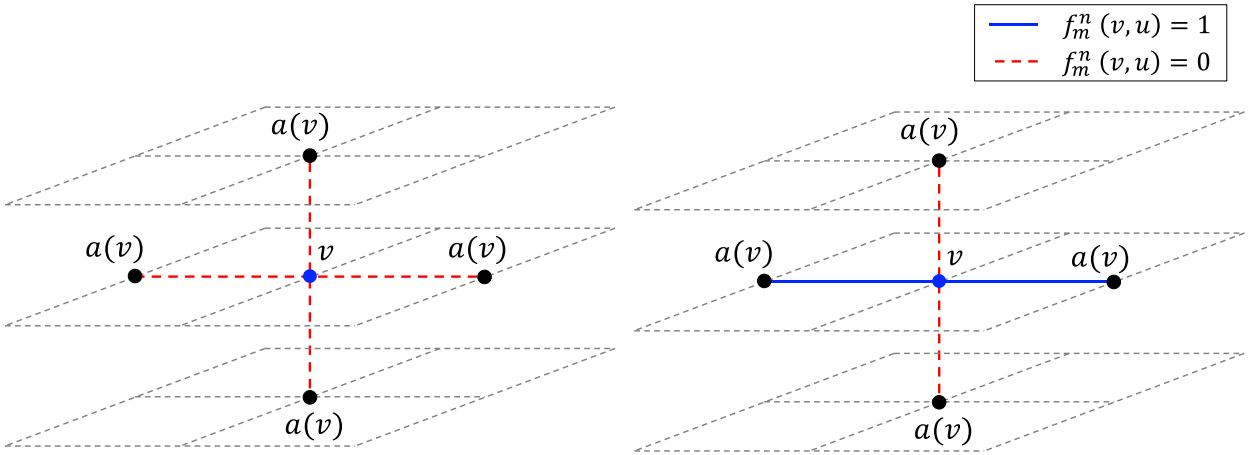
$$\forall v \in V,\ \forall n \in N,\ \forall d_m^n \in D^n$$

$$\sum_{u \in a(v)} f_m^n(v, u) = \begin{cases} 1, & \text{if } v = s^n, t_m^n \\ 2p, p = \{0, 1\}, & \text{otherwise} \end{cases}$$

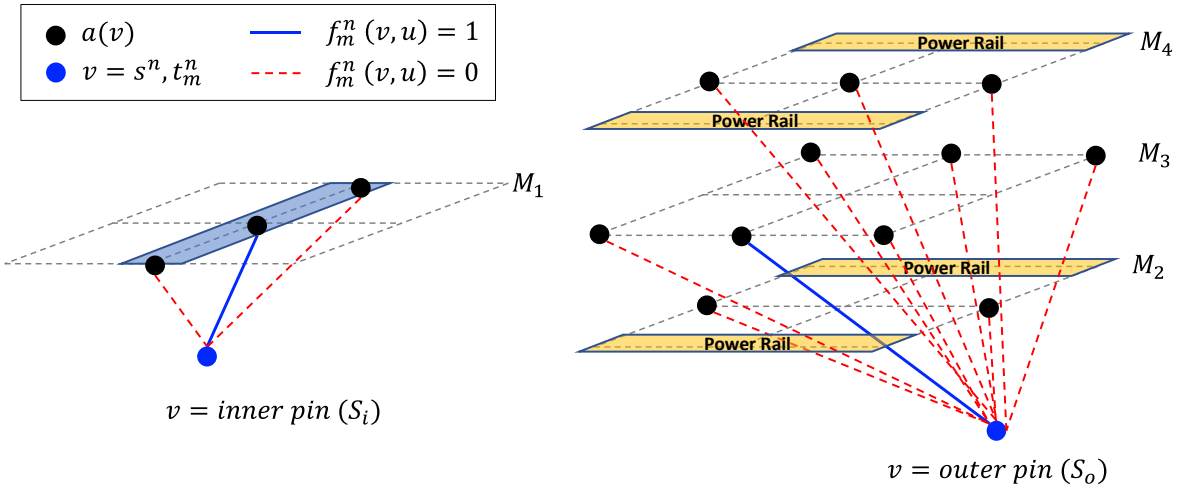
$$\forall v \in V,\ \forall n \in N,\ \forall t_m^n \in T^n$$

$$f_m^n(v) = \begin{cases} 1\ , & \text{if } v = s^n \\ -1\ , & \text{else if } v = d_m^n \\ 0, & \text{otherwise} \end{cases}$$

Grid



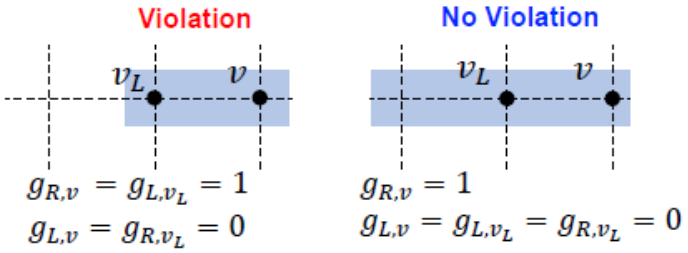
Pin (Source/Sink)
[Supernodes]



BOOLEAN CARDINALITY CONSTRAINT DESIGN RULES

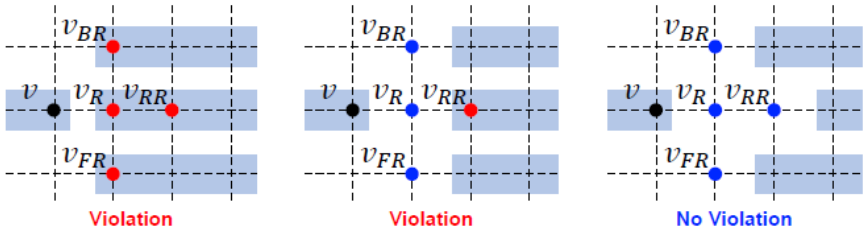
- Minimum Area Rule (MAR), End-of-Line (EOL)
- Self-Aligned Double Patterning (SADP): Parallel Run-Length Rule (PRL), Step-Height Rule (SHR)

MAR



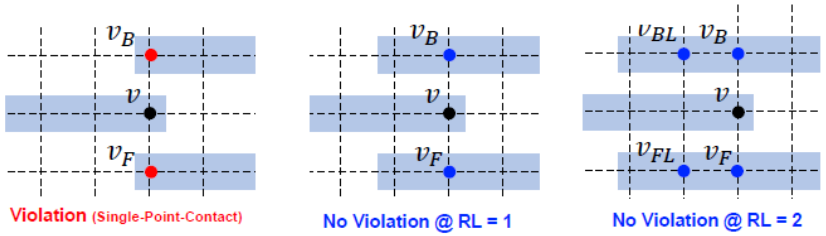
$$g_{L,v} + g_{R,v} + g_{L,v_L} + g_{R,v_L} \leq 1, \quad \forall v \in V_2$$

EOL



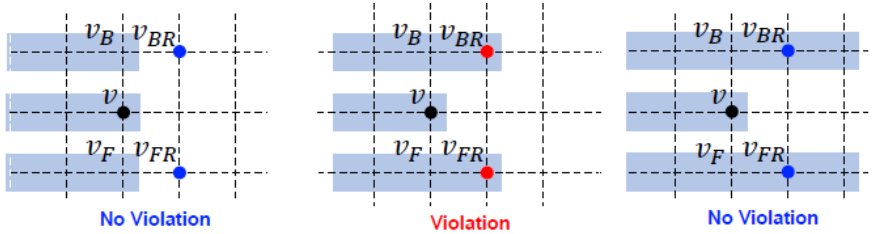
$$g_{R,v} + g_{L,v_{FR}} \leq 1;$$
$$g_{R,v} + g_{L,v_R} + g_{L,v_{RR}} \leq 1; \quad \forall v \in V_2$$
$$g_{R,v} + g_{L,v_{BR}} \leq 1;$$

PRL



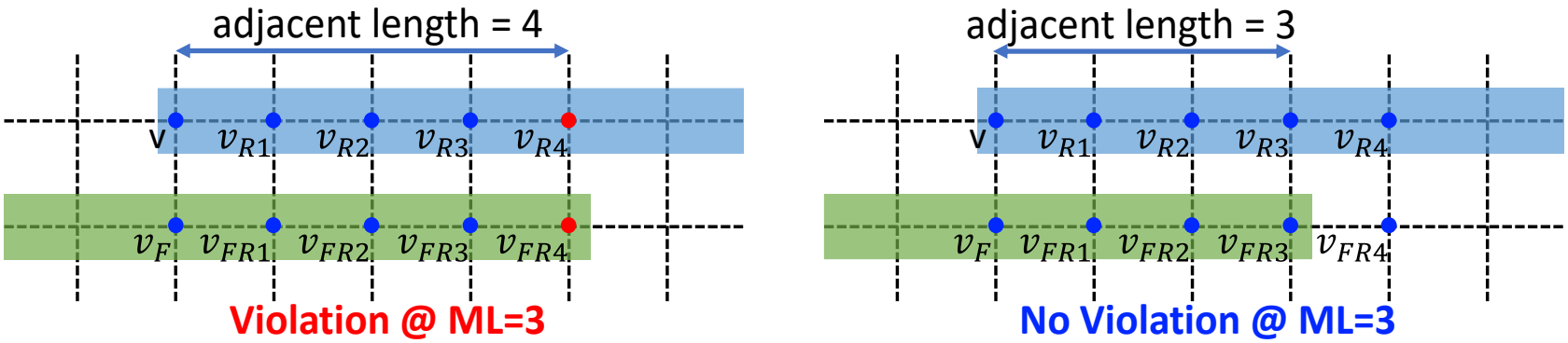
$$g_{R,v} + g_{L,v_B} + g_{L,v_{BL}} \leq 1;$$
$$g_{R,v} + g_{L,v_F} + g_{L,v_{FL}} \leq 1; \quad \forall v \in V_2$$

SHR



$$g_{R,v} + g_{R,v_{BR}} \leq 1; g_{R,v} + g_{R,v_{FR}} \leq 1, \quad \forall v \in V_2$$

PERFORMANCE DRIVEN DESIGN RULES

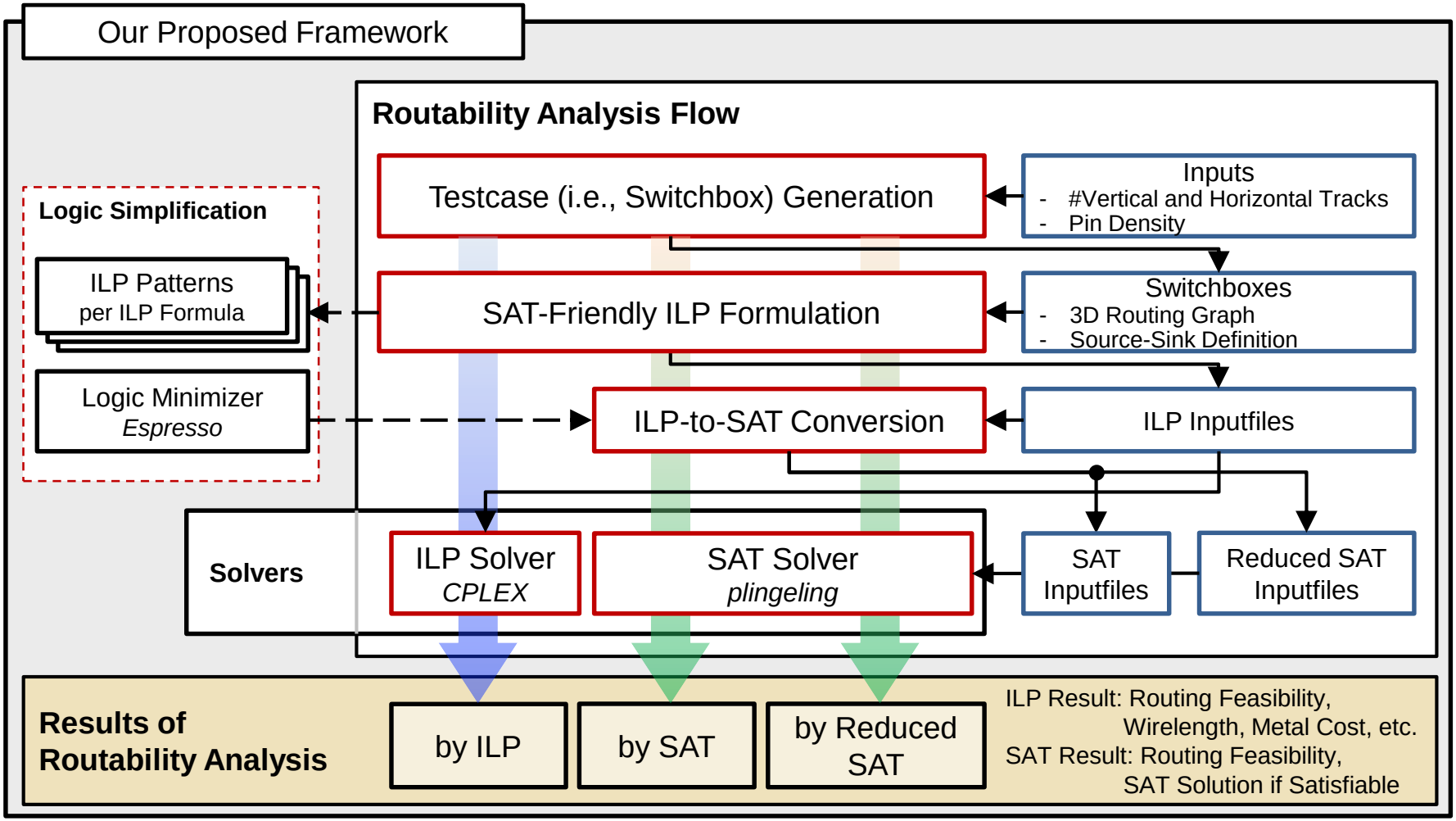


edges of a net n

edges of a net m ($n, m \in N_c$, N_c is a pair of nets with crosstalk mitigation)

FORMULATION & TOOL-CHAIN

- ILP-based routability optimization
- SAT-based routability analysis
- Reduced SAT-based routability analysis



IBM ILOG *CPLEX*, http://www.ilog.com/products/cplex/.
plingeling, Multi-Threading SAT Solver, http://fmv.jku.at/lingeling/.

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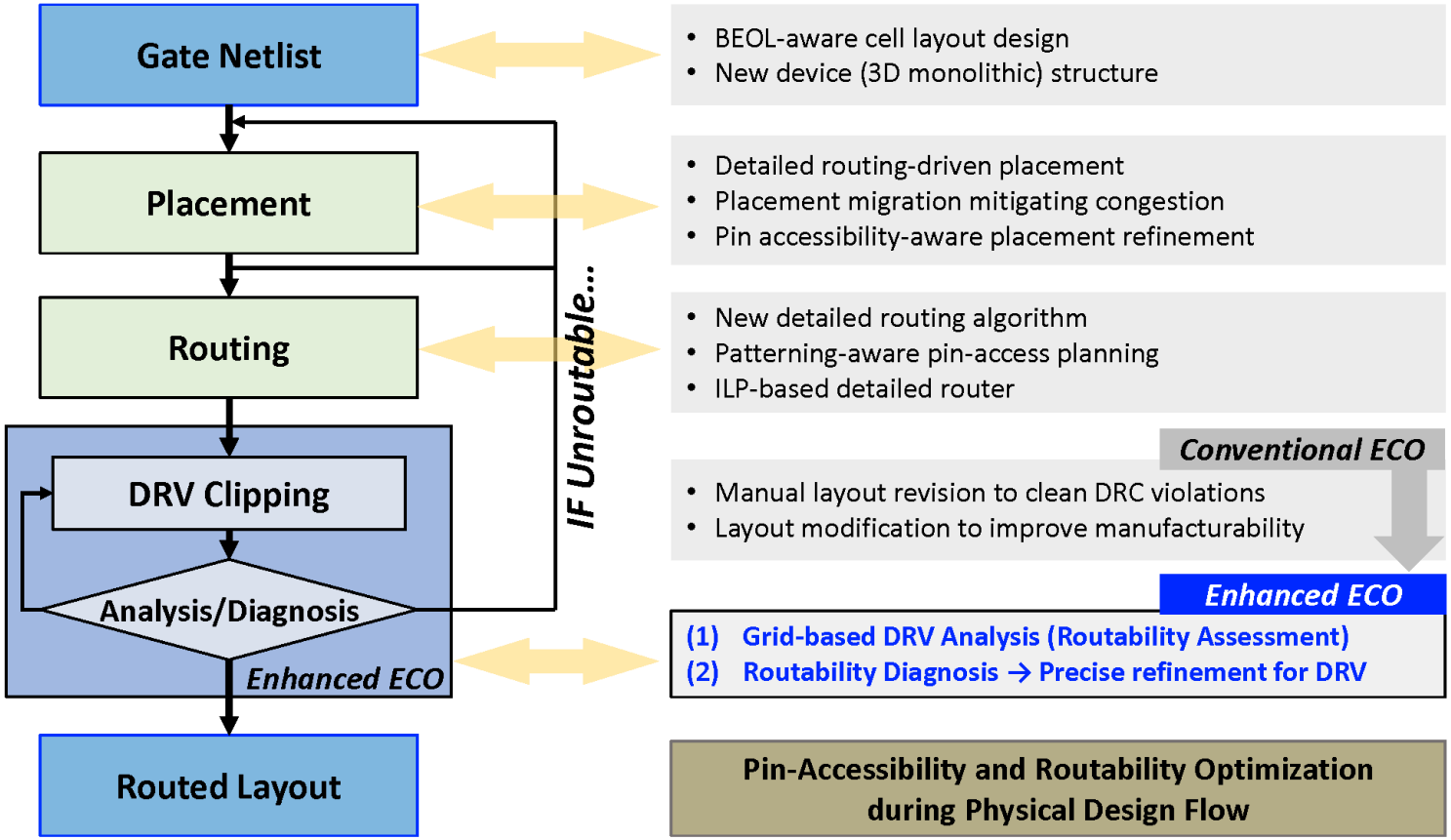
EFFORTS TO IMPROVE ROUTABILITY AND OUR APPROACH

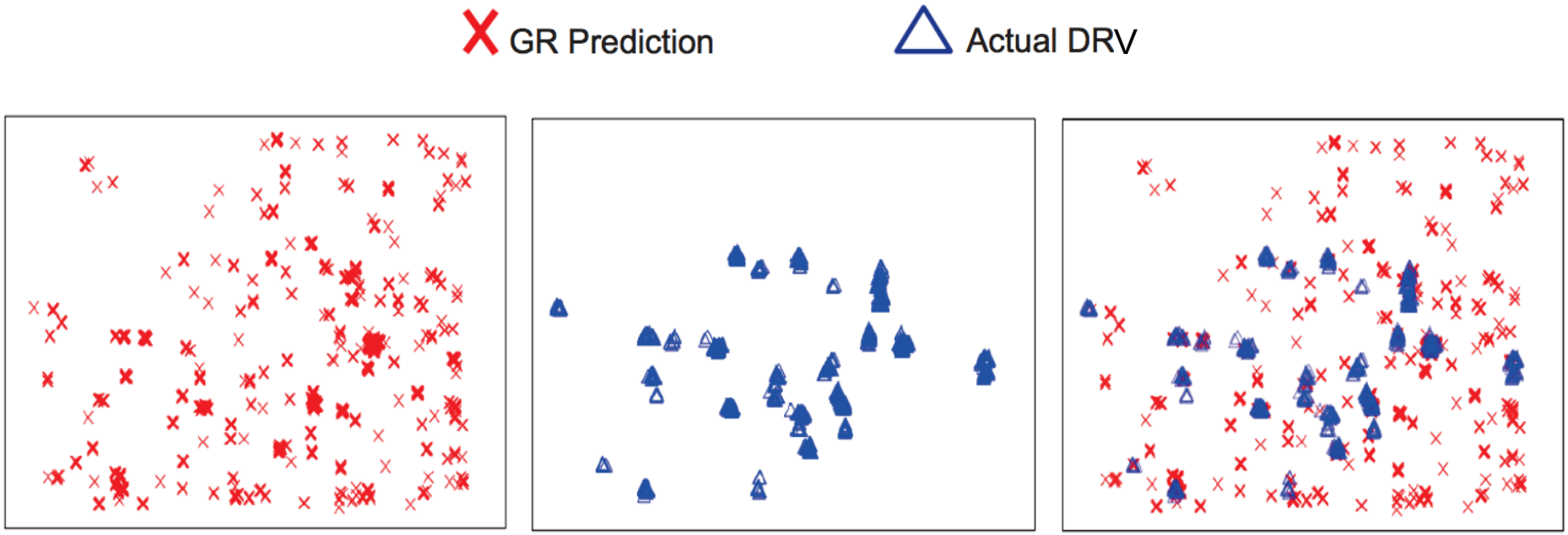
*ECO : Engineering Change Order

- Ensuring Routable layout is non-trivial problem
  - Design for Manufacturability (DFM) in sub-10nm → Complex Design rules
  - Fewer routing tracks / Higher pin density → Limited Routability (including pin-accessibility)
- **Our SAT-based routability analysis → Fast and Precise Assessment**



GROWING MISMATCH BETWEEN GR AND DR

- Global Route based congestion map vs. Actual DRV (Design rule violation)
  - Failure to predict and solve actual routing problem, causing DRVs later.



(a) Overflows extracted from GR-based congestion map (per GCell)

(b) DRVs after detailed routing

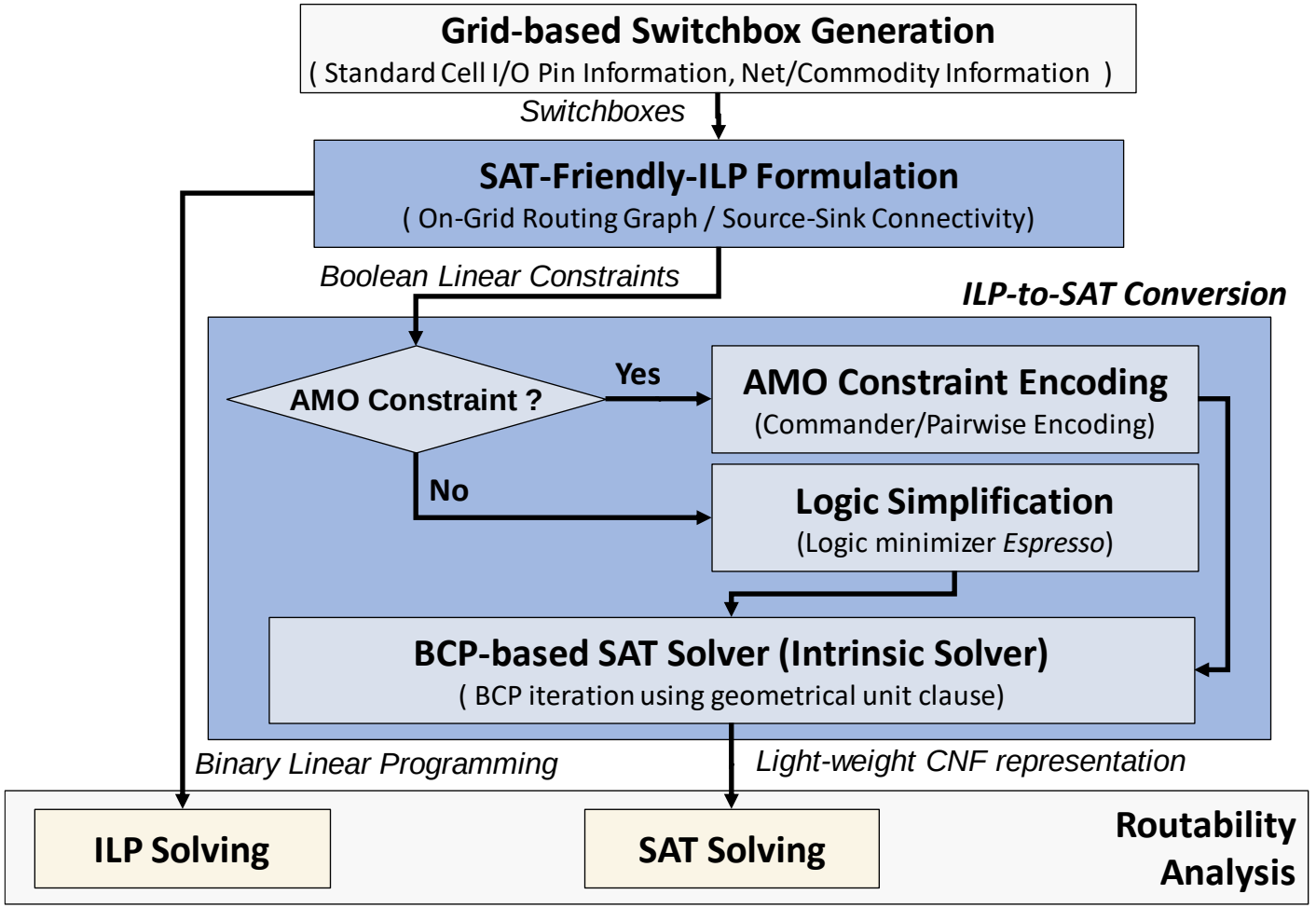
(c) An overlay of the GR predicted overflows and actual DRVs

W.-T. J. Chan, P.-H. Ho, A. B. Kahng and P. Saxena, "Routability Optimization for Industrial Designs at Sub-14nm Process Nodes Using Machine Learning", *Proc. ISPD*, 2017, pp. 15-21.

FRAMEWORK OVERVIEW

*BCP : Boolean Constraint Propagation

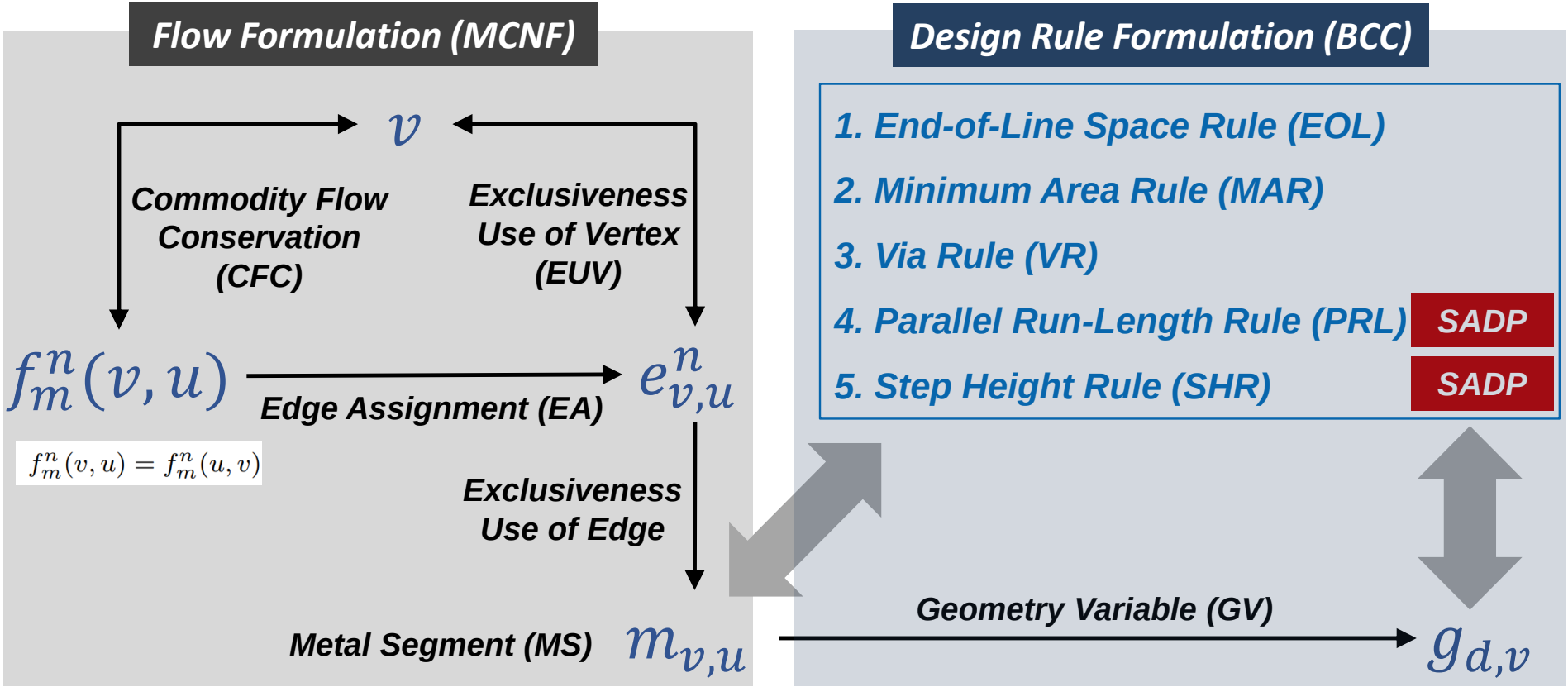
- DRV (Design Rule Violation) Reasoning Techniques
  - ILP (Integer Linear Programming) : Multi-objective → Optimized Routed Layout
  - SAT (Boolean Satisfiability): No Optimization → Fast Routability Analysis



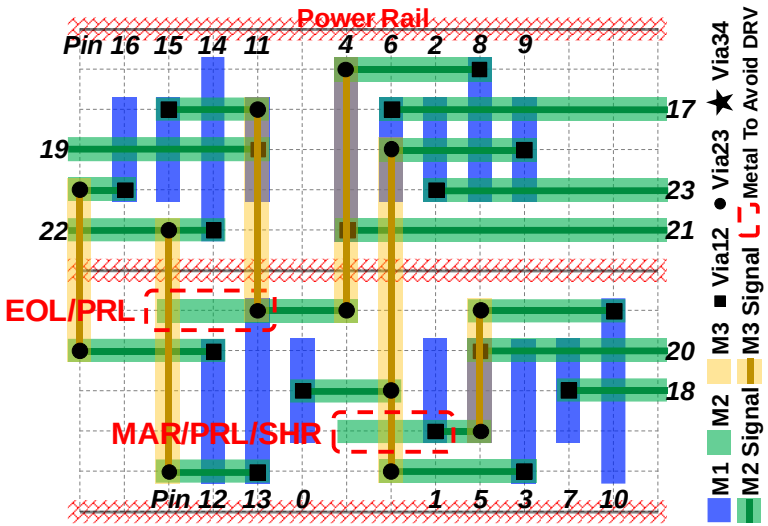
CONSTRAINT FORMULATION FOR DFM-AWARE ROUTING

*SADP : Self-aligned Double Patterning

- Flow (for routing graph) & Design Rule Constraints
  - Flow: Binarized/Undirected multi-commodity network flow (MCNF) theory
  - Design Rule: Geometry variable-based Boolean cardinality constraints (BCC)



AN EXAMPLE OF ROUTABILITY ANALYSIS (ILP & SAT)



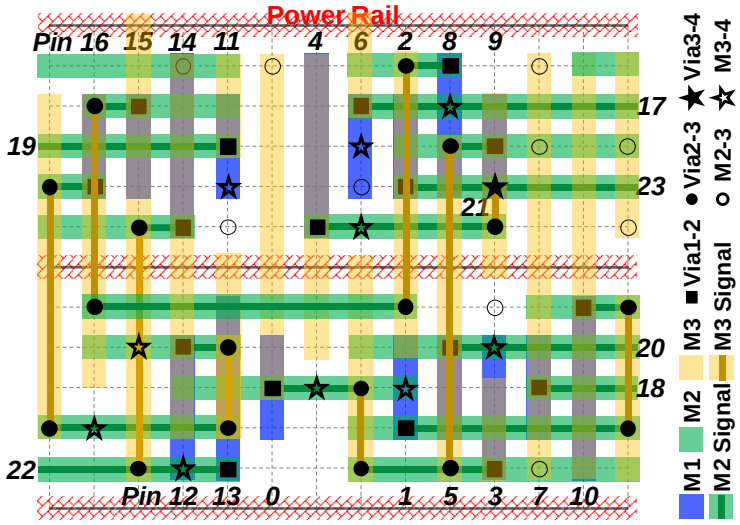
- **#V_Tracks= 14, #H_Tracks= 13**
- **PinDensity= 70%**
- **24 Pins**: 0-23
- **7 Outer Pins**: 17-23
- **11 Nets**: {0 3 9}, {13 14 22}, {7 18}, {6 17}, {4 21}, {11 19}, {1 10}, {8 15}, {5 20}, {2 23}, {12 16}
- ILP Results: **Routable**
- Routing Cost by ILP
  Metal Segments= 212
- Runtimes= (5015s, 1.2s)
  Where (ILP, SAT)

ILP (Integer Linear Programming)

Feasible Solution: 0.6Hr

Optimal Solution: 1.5Hr

Objectives:
Routed Metal Lengths



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- SAT Results: **Routable**
- Routing Cost by SAT
  (*Not Optimized*)
  Metal Segments= 416
- Runtimes= (5015s, 1.2s)
  where (ILP, SAT)

SAT (Boolean Satisfiability)

Feasible Solution: 1.2 second

No Optimization

IMPROVEMENT OF FRAMEWORK COMPLEXITY

- Scalability Improvement compared to our previous publication [SLIP'18]
  - Only **26.7/0.8/0.6%** of Variable/Literal/Clause Number
  - Runtime for 20x19x70: 9.7Hr (ILP with Optimization) → 2.8s (SAT with Routability) **(<0.02%)**

EXPERIMENTAL RESULTS PRESENTING THE ILP-BASED OPTIMIZATION VS. THE SAT-BASED ROUTABILITY ANALYSIS WITH COMPARISON BETWEEN [25] AND OUR PROPOSED FRAMEWORK. IN THE TABLE, RED. = REDUCTION RATIO, T = RUNTIME (IN ILP, *CPLEX* IS TERMINATED BY THE TIME LIMIT), AND T% = RUNTIME% VS. ILP. T% AVERAGE = THE AVERAGE T% OF THE SAT. DESIGN RULES [GRIDS]: MAR/EOL = 2, VR = $\sqrt{2}$, PRL/SHR = 1.

Testcase [25]	Spec.		ILP-based Routing Optimization							SAT-based Routability Analysis											
			#Variables			#Constraints			T(s)	#Variables			#Literals			#Clauses			T(s)	T%
	$\|N\|$	$\|P\|$	[25]	Modified	red.	[25]	Modified	red.		[25]	Modified	red.	[25]	Modified	red.	[25]	Modified	red.		
14_13_60	10.0	21.8	144,721.2	44,314.6	69%	232,174.2	48,167.0	79%	1,076.6	80,315.6	26,345.8	67.2%	6,807,435.0	302,362.4	95.6%	3,471,788.6	125,504.0	96.4%	0.4	0.04
14_13_70	12.0	26.4	195,522.0	53,139.4	73%	312,683.8	56,672.0	82%	3,363.0	107,112.6	34,699.8	67.6%	12,046,890.0	350,503.6	97.1%	6,048,136.6	140,793.6	97.7%	0.4	0.06
14_19_60	14.2	32.2	357,111.8	93,396.4	74%	578,829.2	97,775.8	83%	33,241.4	194,278.6	60,034.0	69.1%	27,316,733.8	580,761.4	97.9%	13,743,476.8	230,531.6	98.3%	1.2	0.01
14_19_70	16.4	36.0	417,015.6	103,795.4	75%	663,016.0	107,065.8	84%	34,677.7	225,426.4	68,852.8	69.5%	38,228,830.0	668,236.2	98.3%	19,287,022.2	265,419.0	98.6%	1.7	0.03
20_13_60	14.6	32.8	368,255.8	92,873.4	75%	595,007.8	97,315.8	84%	35,920.7	199,829.8	59,319.8	70.3%	29,761,672.6	577,675.2	98.1%	14,947,286.4	229,584.2	98.5%	1.0	<0.01
20_13_70	16.4	36.2	415,530.2	101,787.0	76%	662,946.0	106,092.8	84%	>43200	224,503.8	66,902.4	70.2%	38,550,581.4	646,517.2	98.3%	19,287,022.2	256,145.2	98.7%	1.5	<0.01
20_19_60	16.6	44.8	797,507.6	182,478.8	77%	1,293,681.0	186,431.2	86%	35,902.8	427,871.0	123,491.6	71.1%	95,090,666.4	1,143,092.0	98.8%	47,596,732.8	449,297.4	99.1%	9.8	0.03
20_19_70	23.0	52.6	1,037,195.2	213,066.6	79%	1,677,742.8	214,339.2	87%	35,163.2	552,123.0	147,245.0	73.3%	176,174,452.4	1,354,865.8	99.2%	87,585,849.8	528,807.4	99.4%	2.8	0.01
T% Average			(reference) 100.00																	<0.02

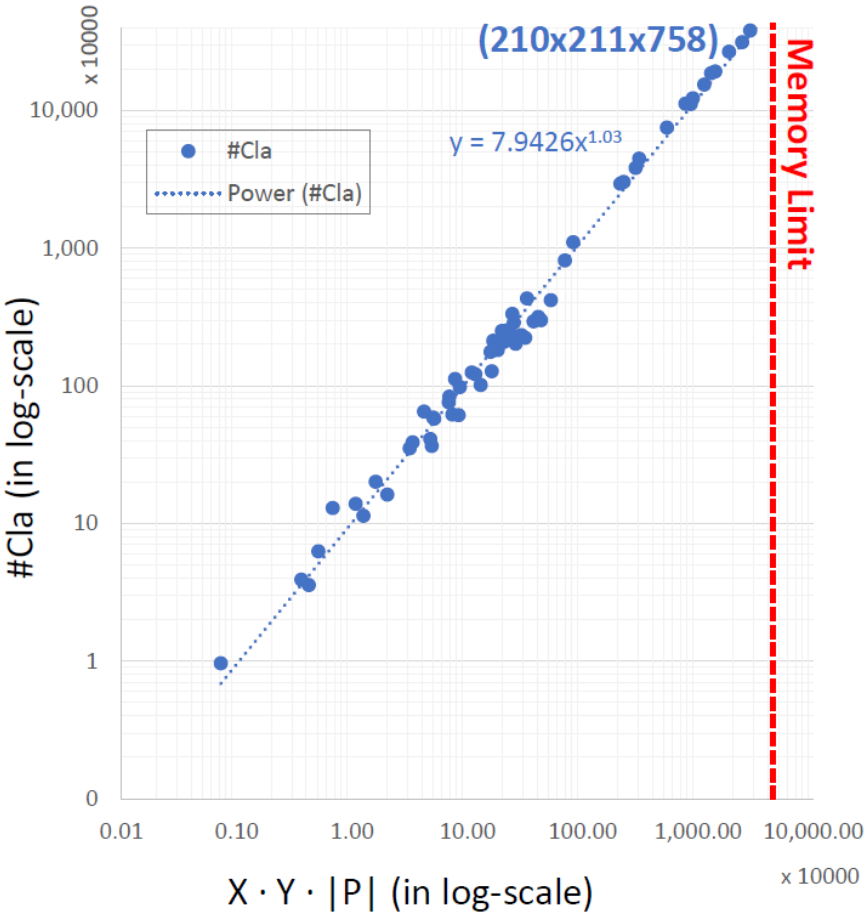
Table III: Analysis for complexity of SAT formulation. In the table, $|N|$ = #Nets, $|T|$ = #Commodities, $|S_o|$ = #OuterPins, $|S_i|$ = #InnerPins, $|P|$ = #Pins, $|D|$ = #Design_rules. $|P| = |T| + |N|$.

Group	Constraint	#Clauses	#Literals	Complexity
Flow	CFC, for grids	$\approx 96 \cdot X \cdot Y \cdot \|T\|$	$\approx 224 \cdot X \cdot Y \cdot \|T\|$	$O(X \cdot Y \cdot \|T\|)$
	CFC, for pins	$\approx 14 \cdot X \cdot Y \cdot \|S_o\|$	$\approx 28 \cdot X \cdot Y \cdot \|S_o\|$	$O(X \cdot Y \cdot \|S_o\|)$
	VE, for grids	$\approx 30 \cdot X \cdot Y \cdot \|N\|$	$\approx 60 \cdot X \cdot Y \cdot \|N\|$	$O(X \cdot Y \cdot \|N\|)$
	VE, for pins	$\approx 10 \cdot \|S_i\|$	$\approx 20 \cdot \|S_i\|$	$O(\|S_i\|)$
	EA	$7 \cdot X \cdot Y \cdot \|T\|$	$14 \cdot X \cdot Y \cdot \|T\|$	$O(X \cdot X \cdot \|T\|)$
	MS	$\approx \frac{49}{2} \cdot X \cdot Y \cdot \|N\|$	$\approx 49 \cdot X \cdot Y \cdot \|N\|$	$O(X \cdot Y \cdot \|N\|)$
Flow Complexity		$\approx 103 \cdot X \cdot Y \cdot \|P\|$	$\approx 238 \cdot X \cdot Y \cdot \|P\|$	$O(X \cdot Y \cdot \|P\|)$

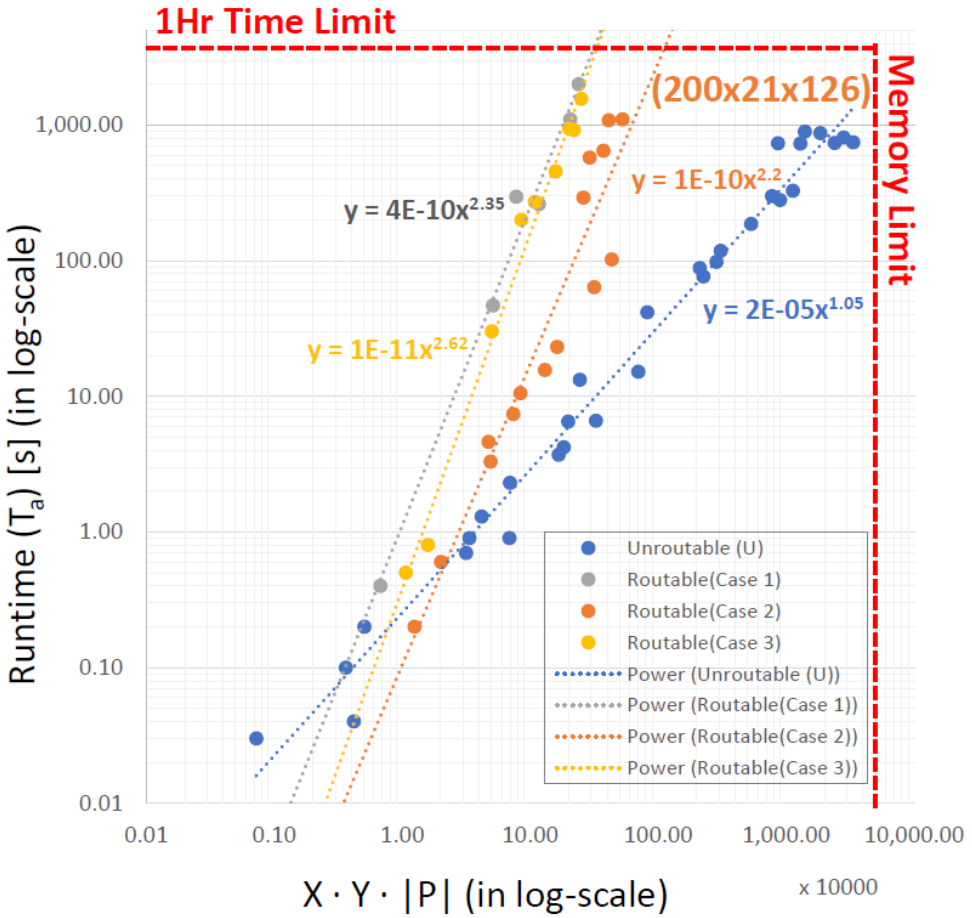
Design Rule	GV	$\approx 12 \cdot X \cdot Y$	$\approx 28 \cdot X \cdot Y$	$O(X \cdot Y)$
	MAR	$\approx 12 \cdot X \cdot Y$	$\approx 24 \cdot X \cdot Y$	
	EOL	$\approx 20 \cdot X \cdot Y$	$\approx 40 \cdot X \cdot Y$	
	PRL	$\approx 24 \cdot X \cdot Y$	$\approx 48 \cdot X \cdot Y$	
	SHR	$\approx 8 \cdot X \cdot Y$	$\approx 16 \cdot X \cdot Y$	
	VR	$\approx 21 \cdot X \cdot Y$	$\approx 42 \cdot X \cdot Y$	
Design Rule Complexity		$\approx 97 \cdot X \cdot Y$	$\approx 198 \cdot X \cdot Y$	$O(X \cdot Y)$
Framework Scalablility		$O(X \cdot Y \cdot \|P\|) + O(X \cdot Y \cdot \|D\|)$		

SCALABILITY OF ANALYSIS FRAMEWORK

- "Unroutable" case: 116.6x Switchbox size (20x19 [SLIP'18] → 210x211)
- "Routable" case: 16.2x Switchbox size (20x13 [SLIP'18] → 200x21)



(a) Complexity of Clause



(b) Analysis Runtime

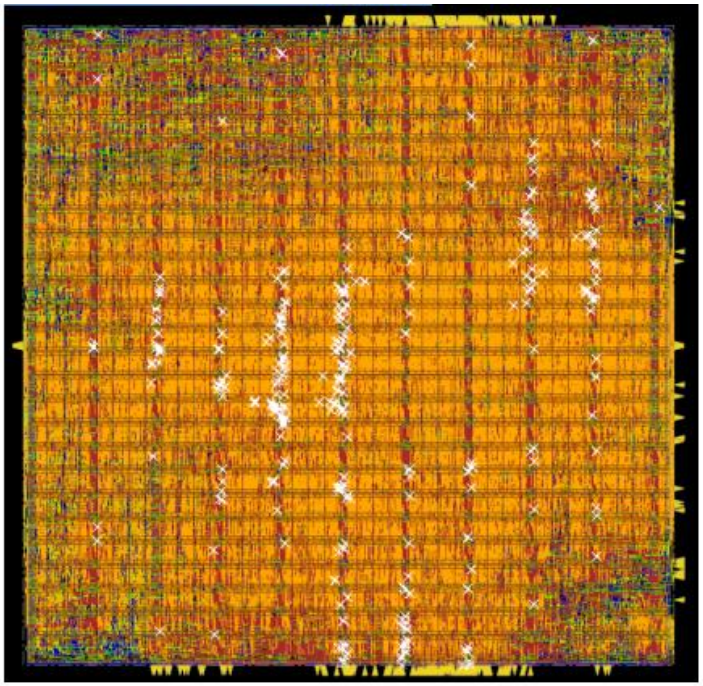
CHAPTER 1 – ROUTABILITY ANALYSIS

- **SAT-based routability analysis in DR (detailed routing)**
  - Design rule-correct routability assessment
  - Offers an early (i.e., before routing) “go/no-go” decision opportunity
- **Fast and precise routability assessment**
  - Out refined SAT-based routability analysis gives design rule-correct routability assessment within **0.02%** of ILP runtime on average
- **Efficient ILP-to-SAT conversions**
  - Supernode Simplification, Unidirectional/Binarized MCNF
  - Commander Encoding for BCC: Refined Complexity $O(n^2)$ → **O(n)**
- **Improved Scalability of Routability Analysis**
  - Compared to [SLIP’18], covers up to **116.6x** Switchbox (20x19 → 210x211)

- *Introduction*
- *Ch.0) Formulation Background*
- *Ch.1) Routability Analysis (ILP/SAT)*
- ***Ch.2) Routability Diagnosis (SAT)***
- *Ch.3) Standard Cell Synthesis (SMT)*
- *Future*

DRV(Design-Rule Violation) Report In DR

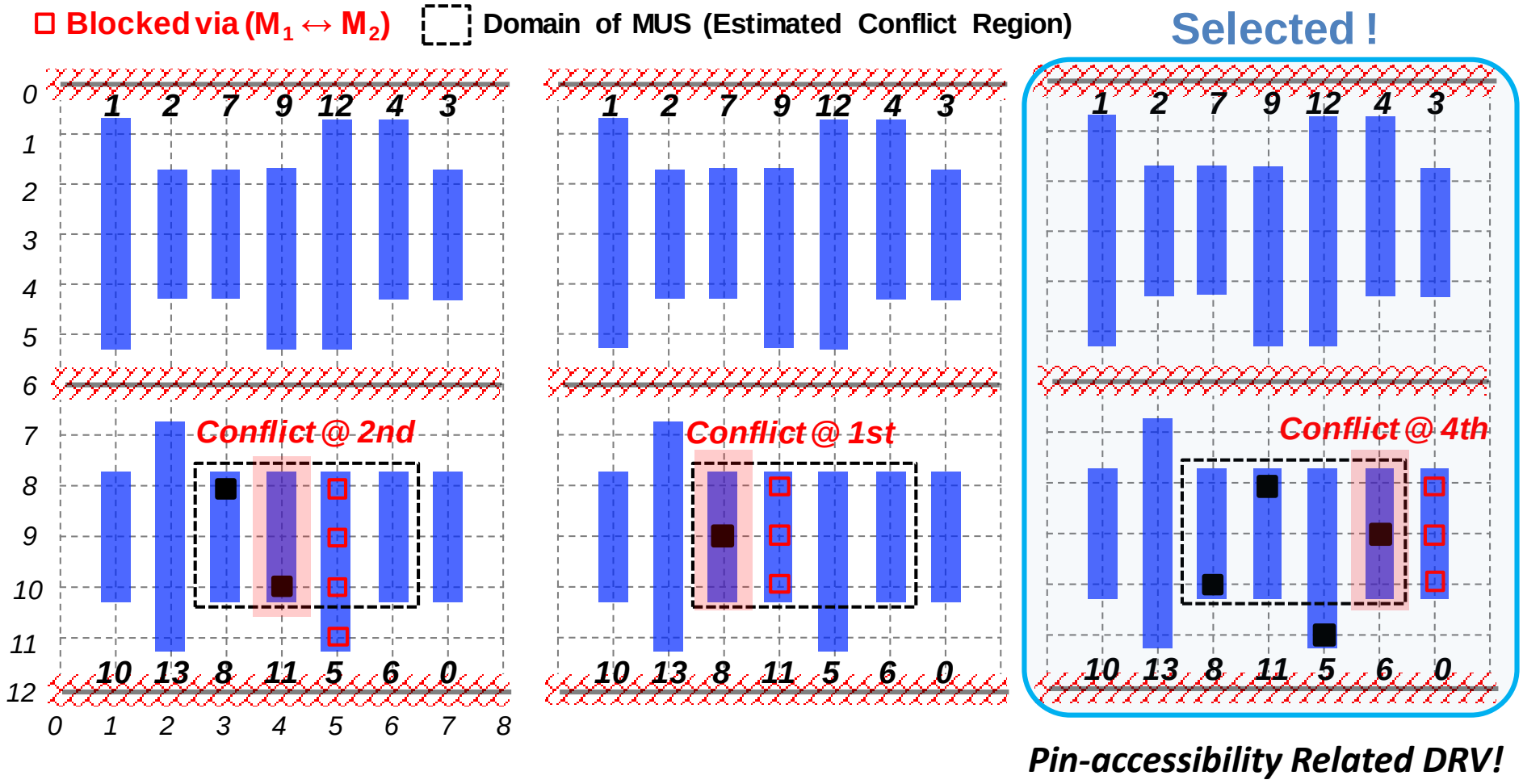
- Required information for a timely troubleshooting
  - Exact Location of Failure & Root cause of the conflict
- Limitation of DRV Report in Commercial Tool
  - Heuristic manner of Routing Algorithm → Often Non-Comprehensible
  - Ambiguous Root Cause: Pin-accessibility related? Routing Congestion related?
  - **Hard to Debug...**



```
#############################################################
#  Generated by:      Cadence Innovus 18.14-s088_1
#  OS:                Linux x86_64(Host ID soi.ucsd.edu)
#  Generated on:      Thu Jul 16 09:06:49 2020
#  Design:            bsg_chip
#  Command:           verify_drc -limit 100000000 -report verify_drc.rpt
#############################################################

SHORT: ( Metal Short ) Special Wire of Net VDDIO_0 & Pin of Cell bp_v18_17  ( LB )
Bounds : ( 2654.100, 2935.807 ) ( 2655.900, 2937.607 )


SHORT: ( Metal Short ) Special Wire of Net VSSIO_0 & Pin of Cell bp_vzz_17  ( LB )
Bounds : ( 2724.100, 2935.807 ) ( 2725.900, 2937.607 )


MAR: ( Minimum Area ) Regular Wire of Net net47193  ( C4 )
Bounds : ( 2769.364, 2822.380 ) ( 2769.506, 2822.420 )


MAR: ( Minimum Area ) Regular Wire of Net net47862  ( M3 )
Bounds : ( 2627.516, 2822.231 ) ( 2627.548, 2822.441 )


MAR: ( Minimum Area ) Regular Wire of Net net47185  ( M3 )
Bounds : ( 2629.436, 2822.231 ) ( 2629.468, 2822.441 )


MAR: ( Minimum Area ) Regular Wire of Net net47185  ( C4 )
Bounds : ( 2629.366, 2822.380 ) ( 2629.508, 2822.420 )


MAR: ( Minimum Area ) Regular Wire of Net net47188  ( M2 )
Bounds : ( 2686.563, 2822.256 ) ( 2686.649, 2822.288 )


MAR: ( Minimum Area ) Regular Wire of Net net47864  ( M2 )
Bounds : ( 2691.355, 2822.256 ) ( 2691.445, 2822.288 )


MAR: ( Minimum Area ) Regular Wire of Net net47187  ( M2 )
Bounds : ( 2694.547, 2822.256 ) ( 2694.645, 2822.288 )
```

Our Approach: Comprehensible/Richer Explanation

- Determined explanation among the candidates: Longest Path Searching
  - **Exact Geometry/Design-Rules** and **DRV Classification**

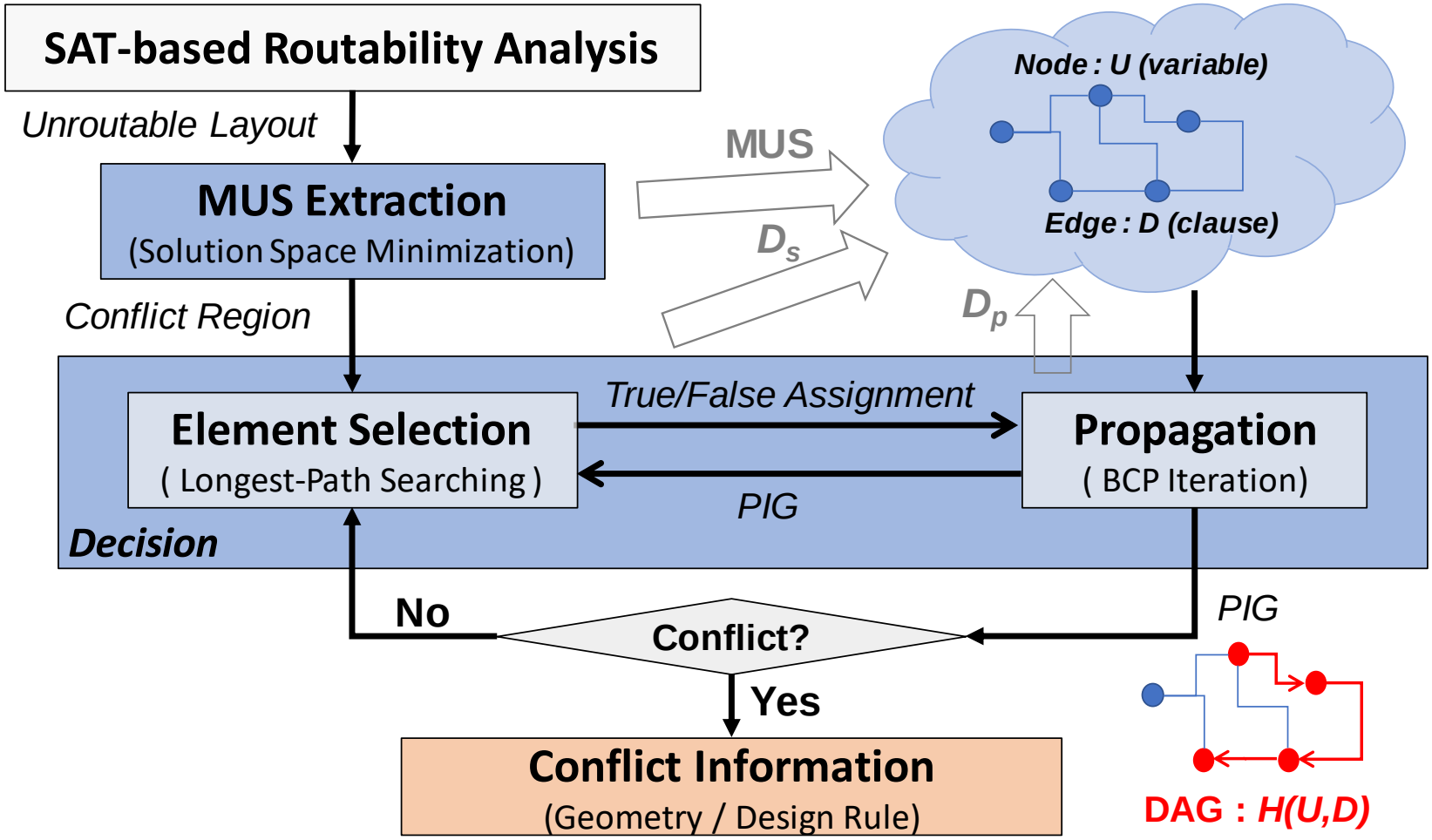


Pin-accessibility Related DRV!

ROUTABILITY DIAGNOSIS FRAMEWORK OVERVIEW

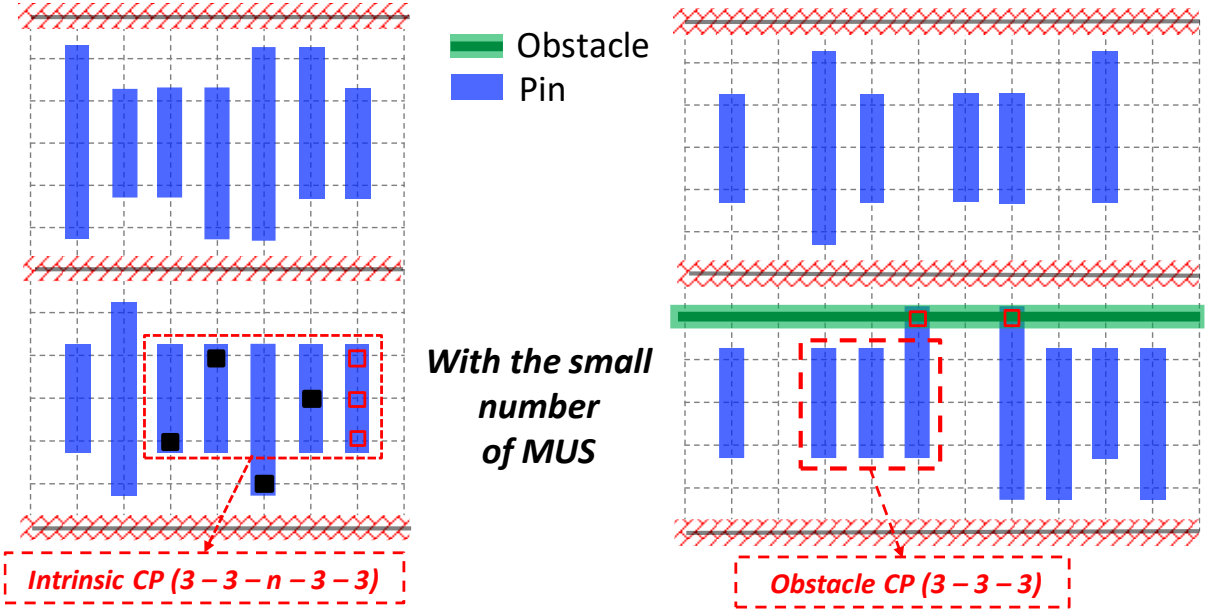
- Logical Reasoning using SAT techniques
  - A special version of SAT Solver for describing DRVs expertly.

**MUS : Minimal Unsatisfiable Subset*
** BCP : Boolean Constraint Propagation*
** PIG : Partial Implication Graph*

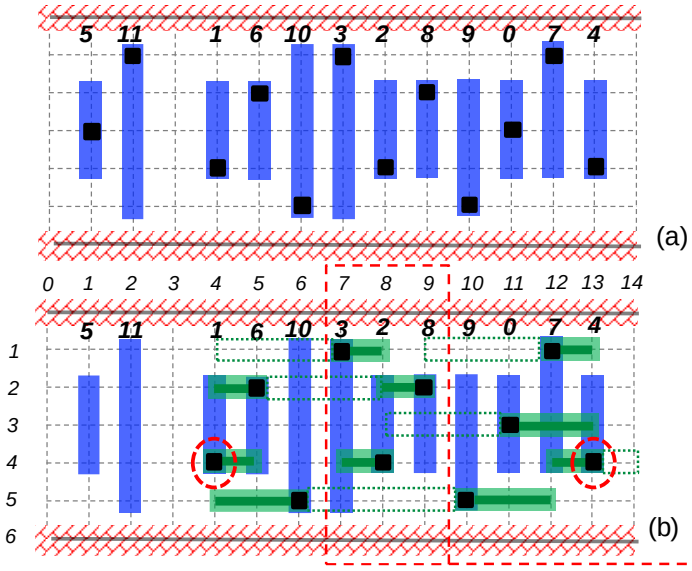


DRV CLASSIFICATION

Conflict Pin-shape (CP)



Routing Congestion (RC)



- **#V_Tracks=15, #H_Tracks=7, PinDensity= 90%**
- **12 Pins**: 0-11
- **8 Outer Pins**: 12-19
- **9 Nets**: {2 11 14}, {5 8 13}, {3 15}, {6 12}, {9 16}, **{1 4},** {7 19}, {0 17}, {10 18}

For net 5, no available track in routing box (7-9th column)!

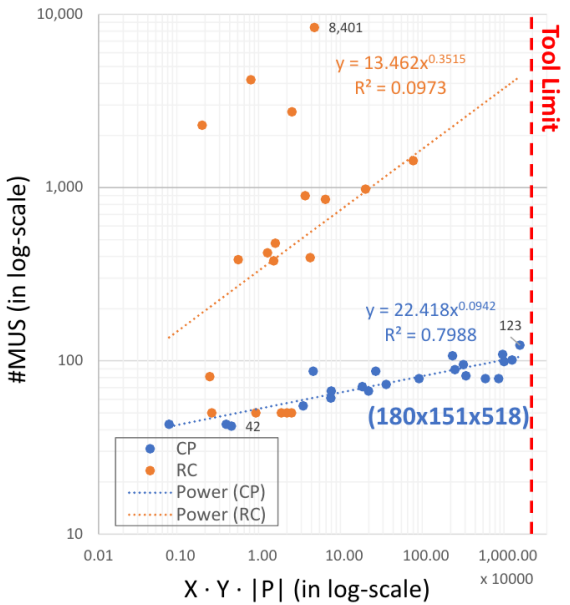
SCALABILITY OF DIAGNOSIS FRAMEWORK

- MUS complexity is linearly increasing as switchbox
- Scalability of MUS extraction: up to 180x151x518

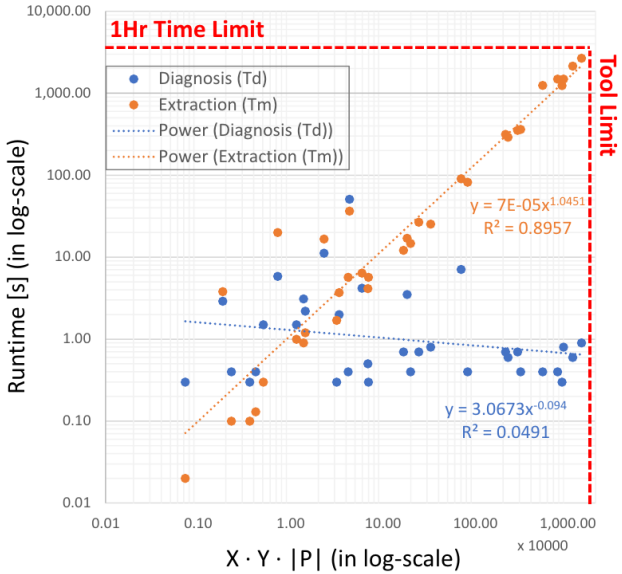
TABLE V

EXPERIMENTAL RESULTS PRESENTING THE SAT-BASED ROUTABILITY ANALYSIS/DIAGNOSIS USING BENCHMARK. IN THE TABLE, RES. = ANALYSIS RESULT (R:ROUTABLE, U:UNROUTABLE, UN:UNDETERMINED WITHIN 1 HR), T_a = ANALYSISTIME, T_m = MUS EXTRACTIONTIME, T_d = DIAGNOSISTIME USING MUS. ALL TIMES IN SECONDS. DESIGN RULES[GRIDS]: MAR/EOL = 2, VR = $\sqrt{5}$, PRL/SHR = 1.

DRV Region	$G(V,E)$ X	Y	Spec. $\|N\|$	$\|P\|$	SAT formulation #Variables	#Literals	#Clauses	Analysis RES.	T_a	Diagnosis #MUS	T_m	T_d	Causes
I	22	11	11	28	25,849	305,070	129,541	R	0.4	DRC-Clean			
II	11	11	3	6	2,390	21,904	9,662		0.03	43	0.02	0.3	Intrinsic CP
	50	51	31	78	711,600	6,223,044	2,499,951		6.5	67	14.7	0.4	
	100	101	107	306	12,640,796	114,246,609	44,676,894	U	118.0	82	361.8	0.4	
	130	131	150	456	31,548,414	287,132,957	111,851,885		299.0	79	1,487.5	0.4	
	120	251	203	617	75,905,221	686,564,221	267,125,453		869.8	Tool Limit			
III	40	21	20	50	181,486	1,622,798	649,429		1.3	87	5.7	0.4	Obstacle CP
	50	51	34	96	935,559	8,414,325	3,334,900		13.2	87	26.8	0.7	
	100	101	73	210	8,377,845	74,828,963	29,433,312		88.1	107	315.1	0.7	
	150	151	97	383	31,527,855	288,360,468	111,787,511	U	731.3	109	1,239.9	0.3	
	160	151	150	468	43,731,414	395,879,429	154,551,067		327.1	101	2,143.6	0.6	
	180	151	163	518	54,701,153	493,161,312	192,196,400		893.0	123	2,674.8	0.9	
	200	201	142	599	88,239,306	814,945,216	314,412,425		737.2	Tool Limit			
	210	211	143	618	99,872,227	923,921,781	356,118,269	UN		Tool Limit			
	210	211	229	758	128,603,347	1,164,414,397	452,603,482	U	744.7				
	60	21	24	61	314,276	2,816,983	1,122,807	R	295.8	DRC-Clean			
IV	41	21	16	39	104,706	944,948	389,512		0.9	896	3.7	2.0	RC
	130	21	25	67	525,432	4,481,977	1,821,497	U	4.2	979	17.0	3.5	
	240	21	50	139	2,297,158	20,407,862	8,148,453		15.2	1,431	90.8	7.1	
	50	21	19	49	165,854	1,414,446	575,577		46.7	Case1 (DRC-Clean)			
	60	31	24	63	348,492	2,987,555	1,213,592	R	260.7				
	80	31	29	83	597,254	5,141,238	2,082,008		1,100.9				
	90	31	30	86	681,806	5,836,976	2,368,057		1,997.3				
	140	11	20	48	180,629	1,506,547	618,057		7.4	Case2 (DRC-Clean)			
	200	11	30	74	373,814	3,122,504	1,277,833	R	23.1				
	200	21	49	126	1,211,678	10,227,342	4,186,623		1,099.8				
	60	21	16	40	156,921	1,432,690	587,317		30.0	Case3 (DRC-Clean)			
	100	21	22	52	358,481	3,094,894	1,252,142	R	271.1				
	150	21	31	80	821,833	7,184,471	2,884,399		1,559.2				



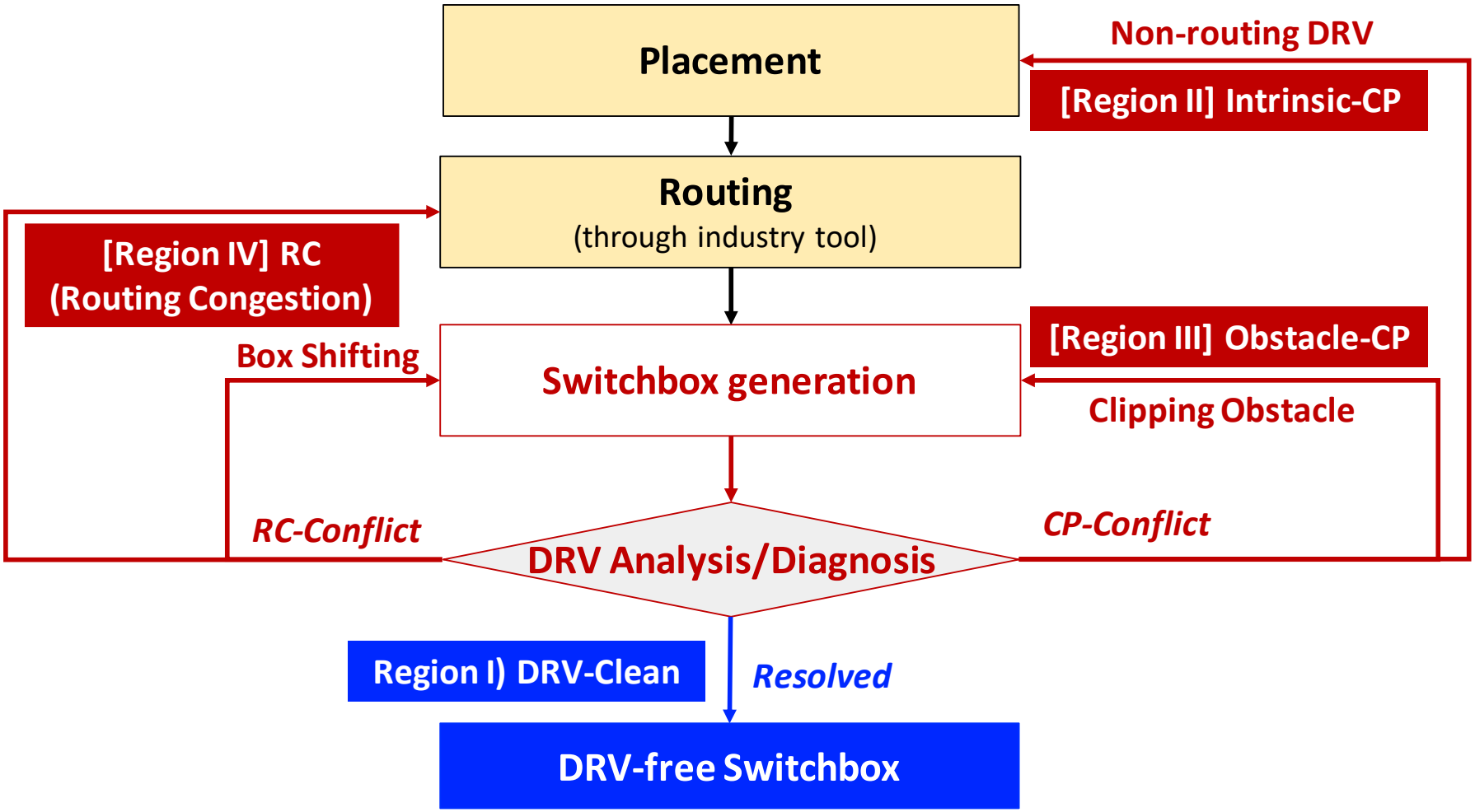
(a) Complexity of MUS



(b) MUS Extraction / Diagnosis Runtime

ENHANCED ECO: PRACTICAL SCENARIOS USING DIAGNOSIS REPORT

- Diagnosis Information → Useful information in ECO stage
  - 4 different kinds of practical scenarios for timely troubleshooting



CHAPTER 2 – ROUTABILITY DIAGNOSIS

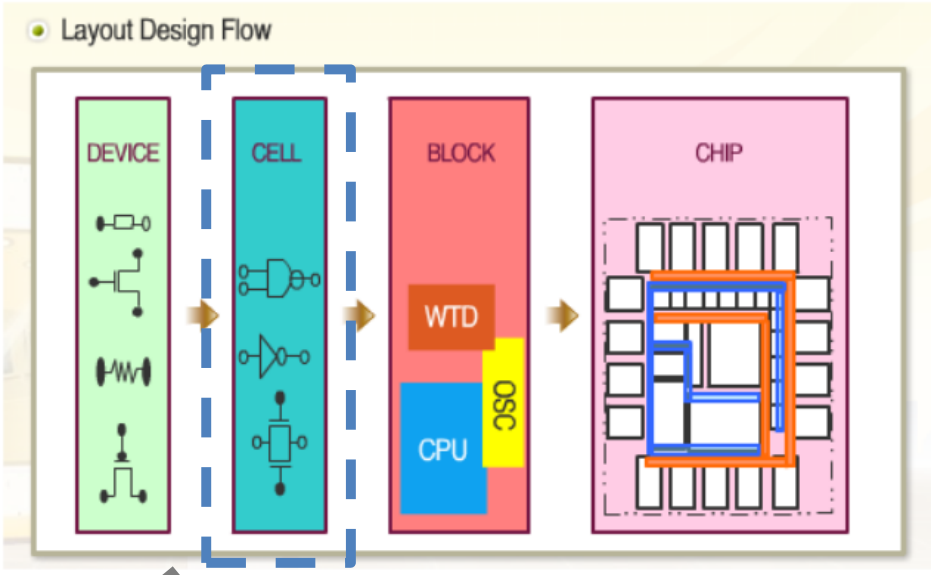
- **SAT-based routability diagnosis for DRVs**
  - A special version of SAT solver for describing design failures.
  - Comprehensive Diagnosis Information through exhaustive exploration.

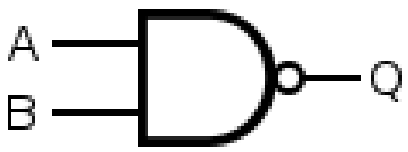
- **Efficient Decision Procedures for Diagnosis Report**
  - Minimized Diagnosis Target: MUS (Minimum Unsatisfiable Subset)
  - Formulation-based Element Selection Scheme: Implication Rule
  - BCP-based iterative Propagation Procedure: Longest-Path DAG

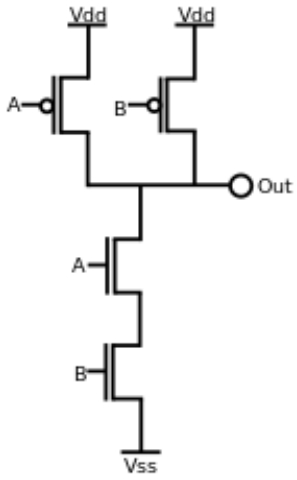
- **Root-cause based DRV classification → Enhanced ECO**
  - Pin-accessibility Problem: **Conflict Pin-shape (CP)** case
    - Intrinsic-CP: Cell Placement Problem → Feedback to Detailed-Placement
    - Obstacle-CP: Routing Obstacle Problem → Switchbox Regeneration in DR
  - Lack of routing resources: **Routing Congestion (RC)** case
    - Feedback to Global Routing (e.g., track assignment overflow)

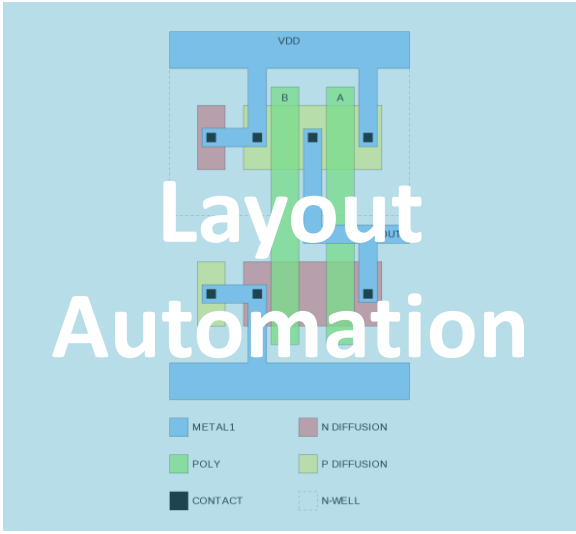
- *Introduction*
- *Ch.0) Formulation Background*
- *Ch.1) Routability Analysis (ILP/SAT)*
- *Ch.2) Routability Diagnosis (SAT)*
- ***Ch.3) Standard Cell Synthesis (SMT)***
- *Future*

STANDARD CELL LAYOUT IN DESIGN FLOW





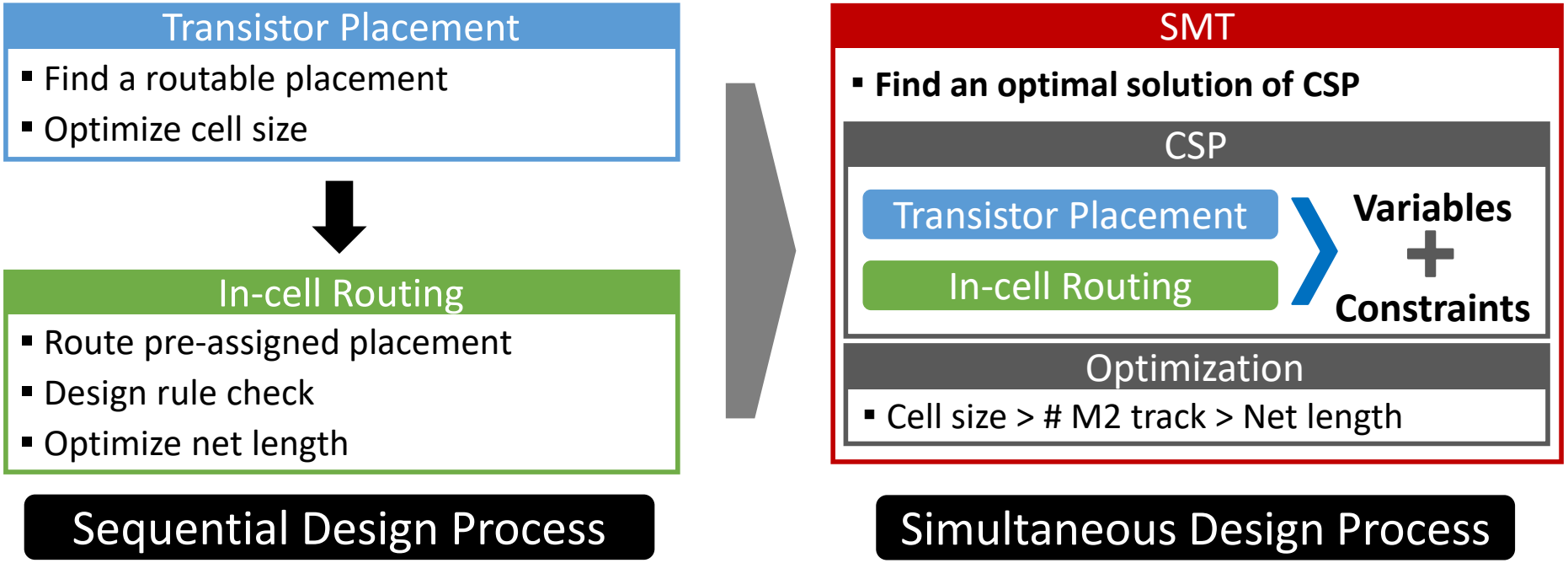




Symbol ***Schematic*** ***Layout***

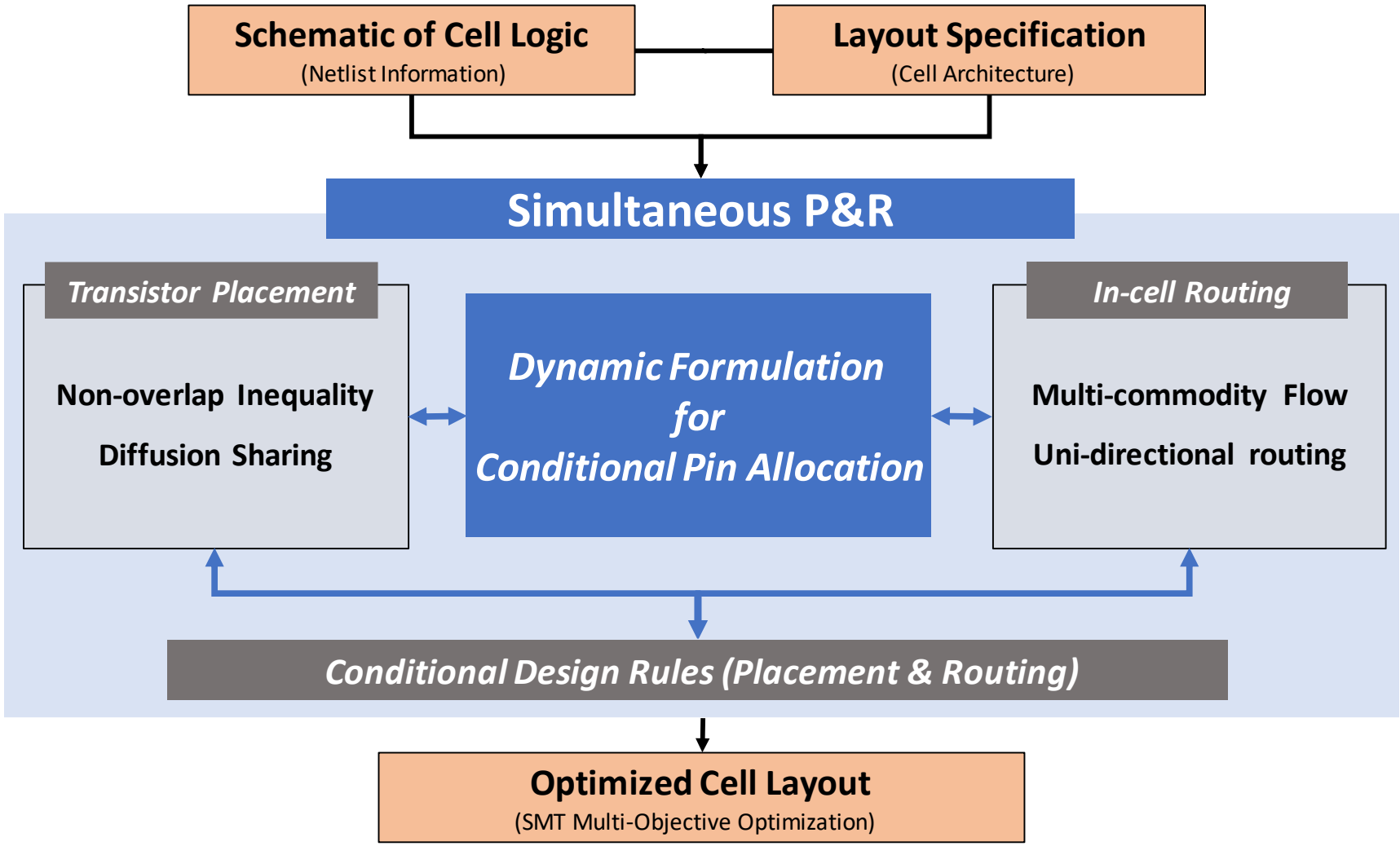
STANDARD CELL SYNTHESIS: SEQUENTIAL → SIMULTANEOUS

- Conventional Approach: **Sequential / Iterative P&R**
- Our Approach: **Simultaneous / Non-iterative P&R (SP&R)**
- SAT/ILP → SMT (Satisfiability Modulo Theory) with Optimization (OMT)
  - Richer modeling language than SAT
    (e.g., conditional constraint (*if-then-else*), Boolean cardinality function (*at-most, at-least*))
  - More concise implementation for conditional constraints than ILP
    (No need of auxiliary variables and constraints)



SP&R Framework Overview

- Dynamic Pin Allocation (DPA) - Integrated Place-and-Route Formulations
- Lexicographic Multiple-Objective Optimization
  - CellSize → #M2 Track → Metal Length

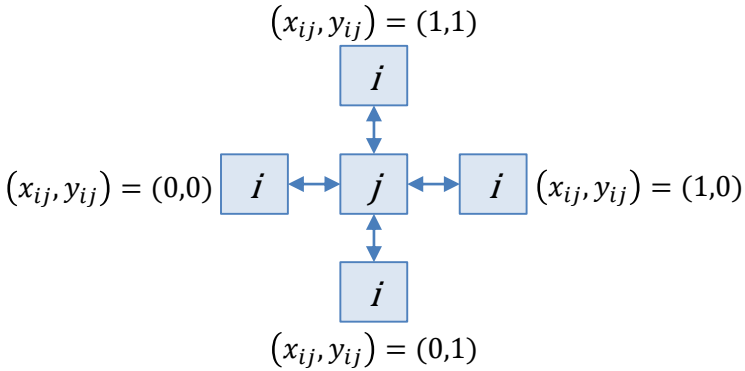


PLACEMENT & ROUTING MODEL

- Transistor Placement
  - Relative Positioning Constraints for Floorplanning

$$x_i + w_i \le x_j + W(x_{ij} + y_{ij})$$
$$x_i - w_j \ge xj - W(1 - x_{ij} + y_{ij})$$
$$y_i + h_i \le y_j + H(1 + x_{ij} - y_{ij})$$
$$y_i - h_j \ge y_j - H(2 - x_{ij} - y_{ij})$$

(x_i, y_i): *lower left corner of module i*
w_i, h_i: *width, height of module i*
W, H: *maximum allowed width&height of chip*



[*Suphachai Sutanthavibul et al., An Analytical Approach to Floorplan Design and Optimization, TCAD 1991*]

- In-Cell Routing
  - Grid-based Routing Graph using Multi-Commodity Flow

$$f_m^n(v) + \sum_{u \in a(v)} f_m^n(u, v) - \sum_{u \in a(v)} f_m^n(v, u) = 0$$

$$\forall v \in V,\ \forall n \in N,\ \forall d_m^n \in D^n$$

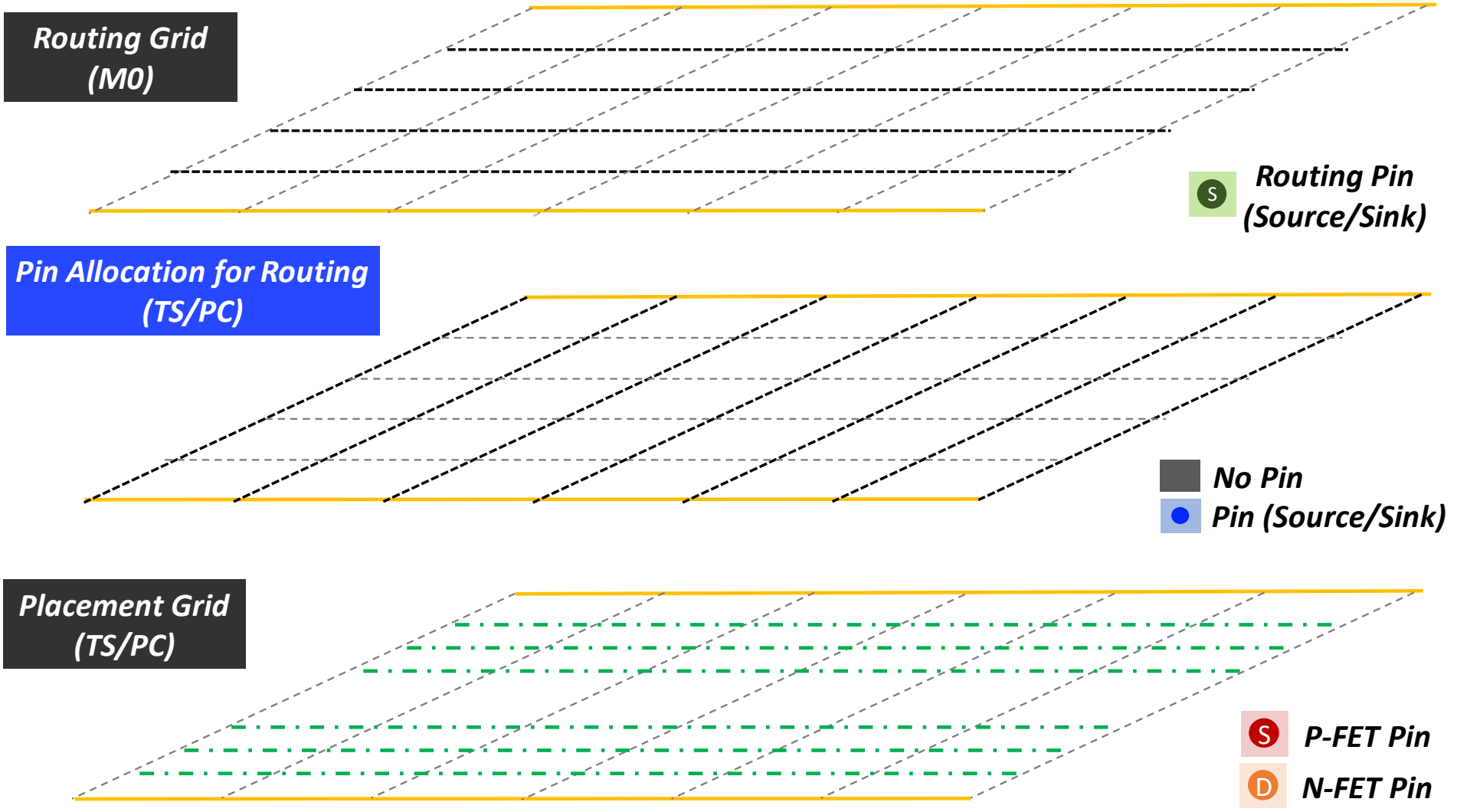
$$f_m^n(v) = \begin{cases} F_m^n, & \text{if } v = s^n \\ -F_m^n, & \text{else if } v = d_m^n \\ 0, & \text{otherwise} \end{cases}$$

V: *Set of vertices in the routing graph G*
N: *Set of multipin nets in the given routing box*
v: *A vertex on the routing graph G*
$a(v)$: *Set of adjacent vertices of vertex v*
s^n: *A source of* n_{th} *net*
d_m^n: m_{th} *sink of* n_{th} *net*
f_m^k: m_{th}*commodity flow of* n_{th} *net*

[*Ilgweon Kang et al., Fast and precise routability analysis with conditional design rules, SLIP 2018*]

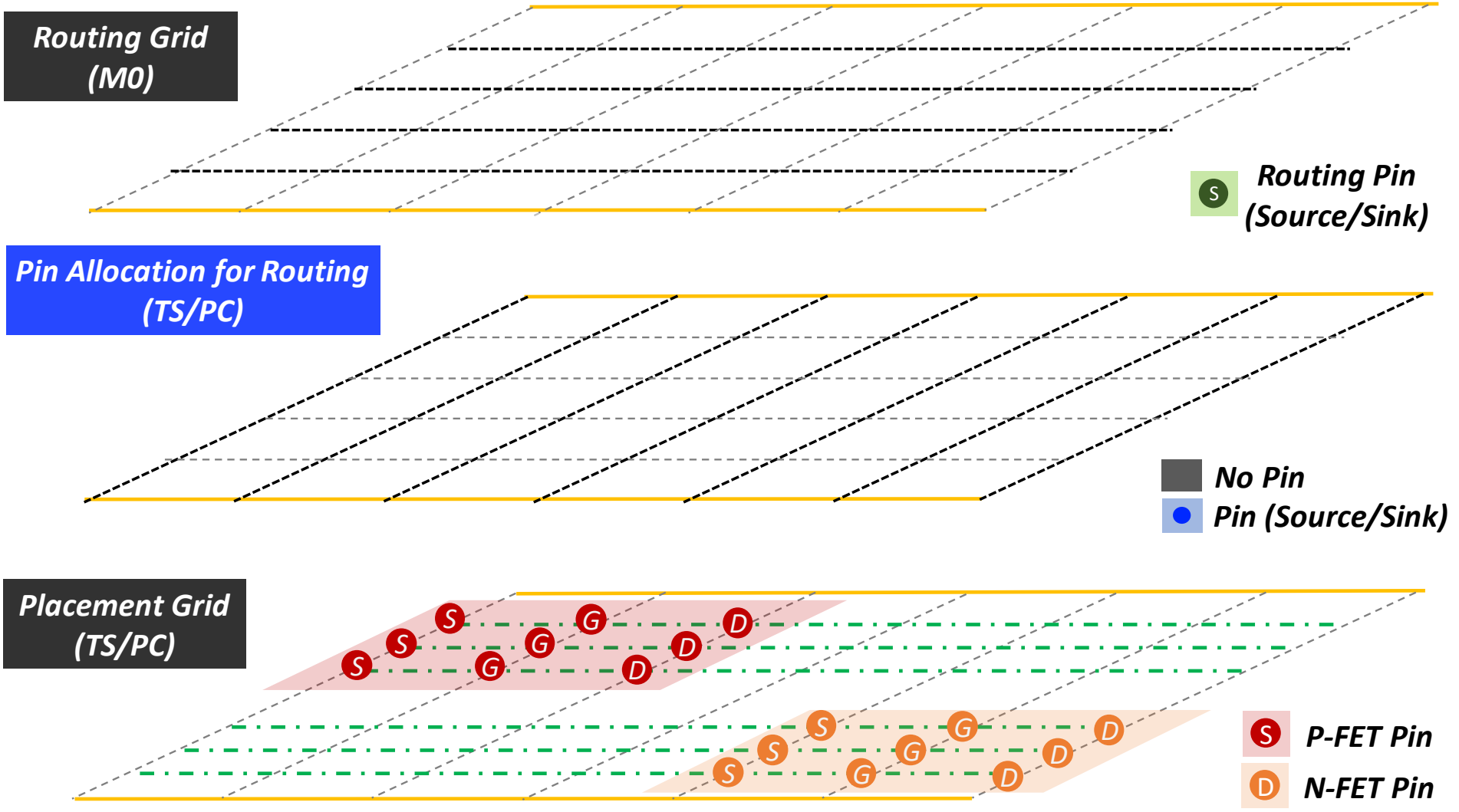
How to Combine?

- Dynamic Pin Allocation (DPA)



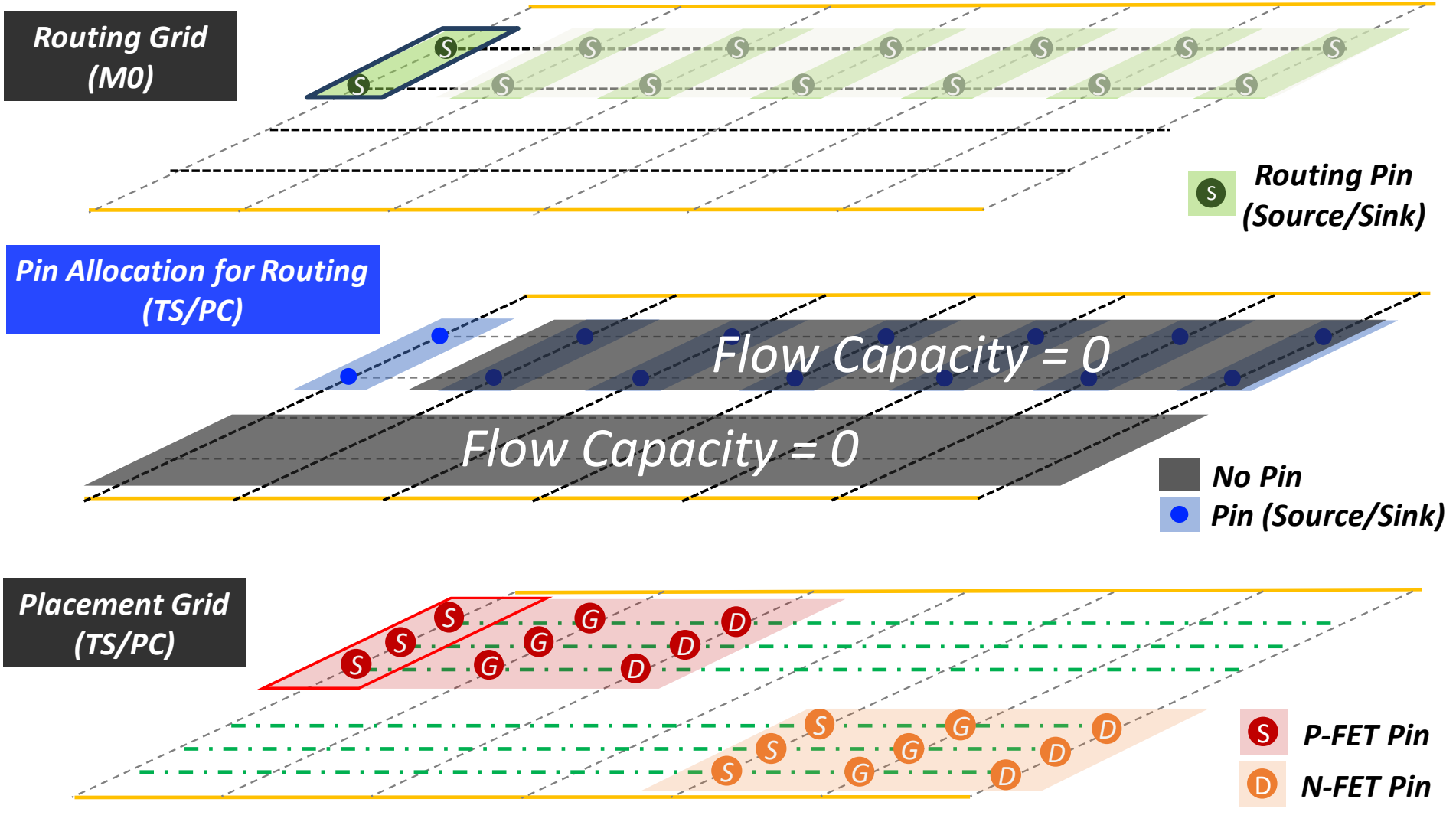
How to Combine?

- Dynamic Pin Allocation (DPA)



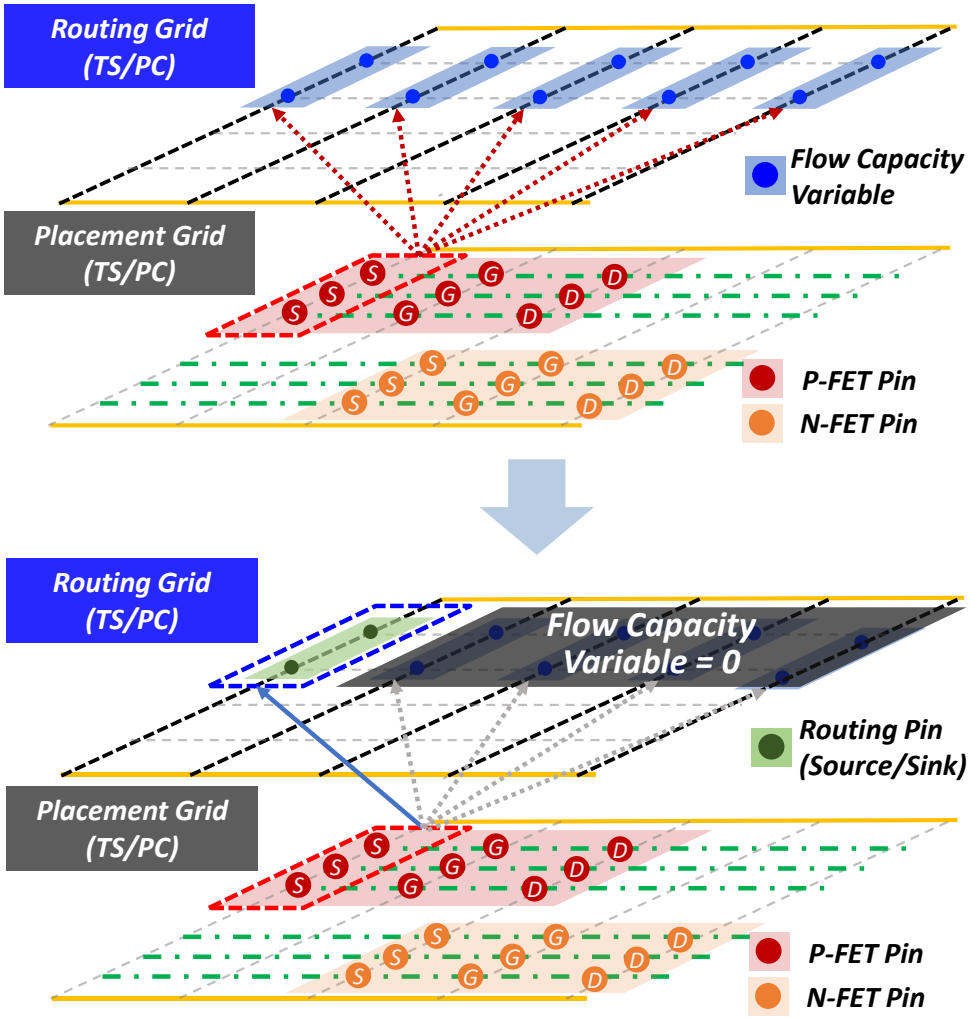
How to Combine?

- Dynamic Pin Allocation (DPA)



DYNAMIC PIN ALLOCATION: SATISFIABILITY MODULO THEORY

- Connection Constraints between Placement and Routing
  - From Placement → Flow Capacity Control / Connection → To Routing



From Placement (Flow Capacity Control)

$$
\begin{aligned}
&if\ \left((x_r \neq x_p) \vee (y_r < y_p) \vee (y_r > y_p + h_p)\right)\ then \\
&\quad C_m^n(p,r) = 0 \\
&else \\
&\quad C_m^n(p,r)\ is\ determined\ by\ CFC^*. \\
&end\ if
\end{aligned}
$$

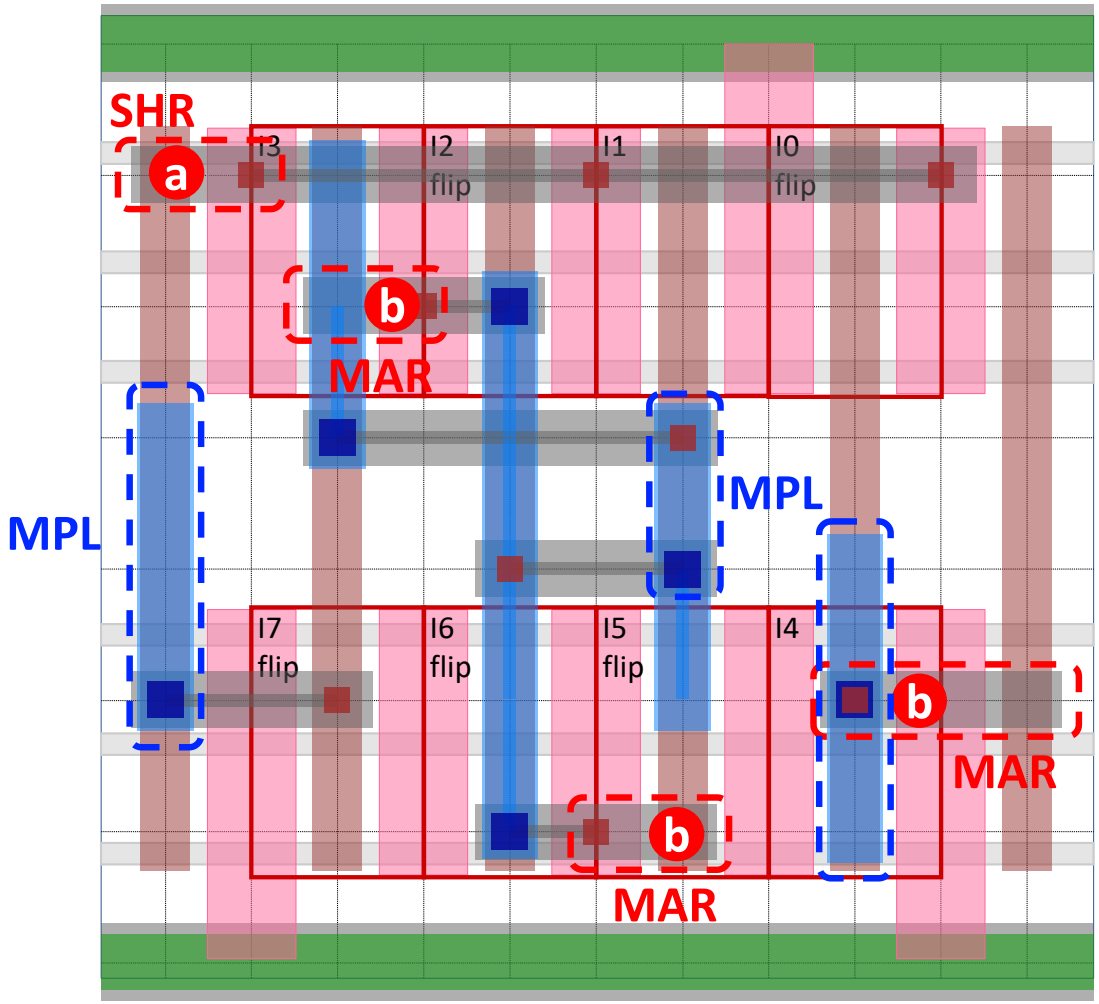
*CFC – Commodity Flow Conservation

To Routing (Flow Capacity Connection)

$$f_m^n(v = p, u = r) \leq C_m^n(p,r)$$

DESIGN RULE-CORRECTED CELL LAYOUT

- AOI22_X1
  - Conditional design rules are successfully applied to the optimized layout



: Gate
: Source/Drain
: M0
: M0 Signal
: M1
: M1 Signal
: M2
: CA
: VIA01

Metal Extension for Design Rule

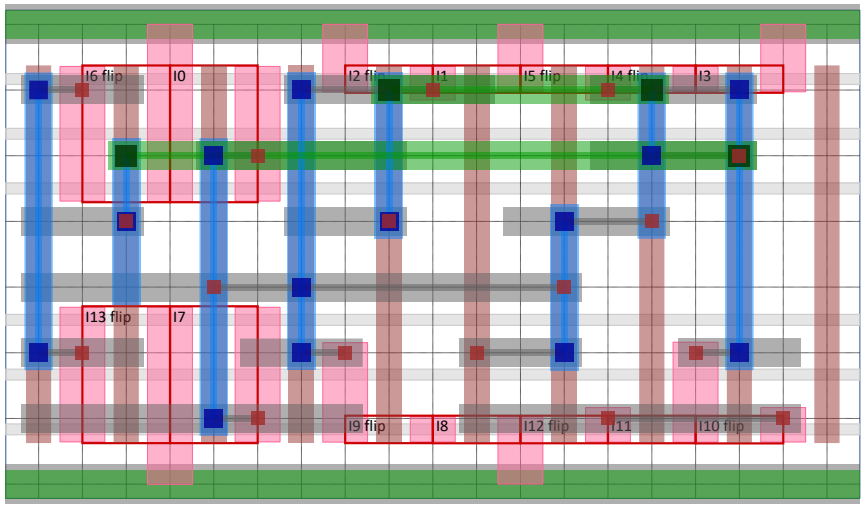
Metal Extension for Pin Access

***AOI22_X1**
#FET=8, #Net=10

*** Optimized Result**
Cell Size (w) = 6 CPP, Metal Length = 95

SEQUENTIAL- VS. SIMULTANEOUS-P&R

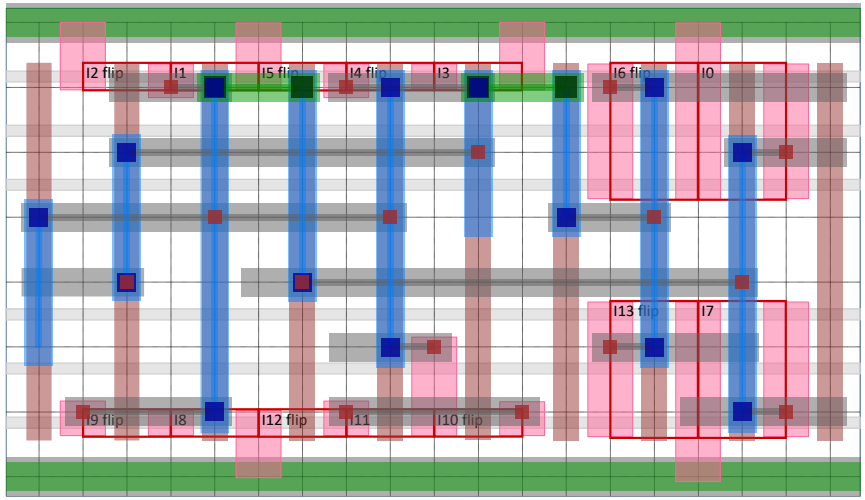
- Key Metric Comparison (size, metal length, # of M2 track)
  - Reduces metal length & #M2 track compared to simulated sequential approach (Metal Length: **10.5%↓**)



: Gate
: Source/Drain
: M0
: M0 Signal
: M1
: M1 Signal
: M2
: M2 Signal
: CA
: VIA01
: VIA12

***HA_X1 (Sequential)**
#F=14, #Net=11

*** Optimized Result**
Cell Size = **10** CPP
Metal Length (ML) = **241**
#M_2 Track = **2**



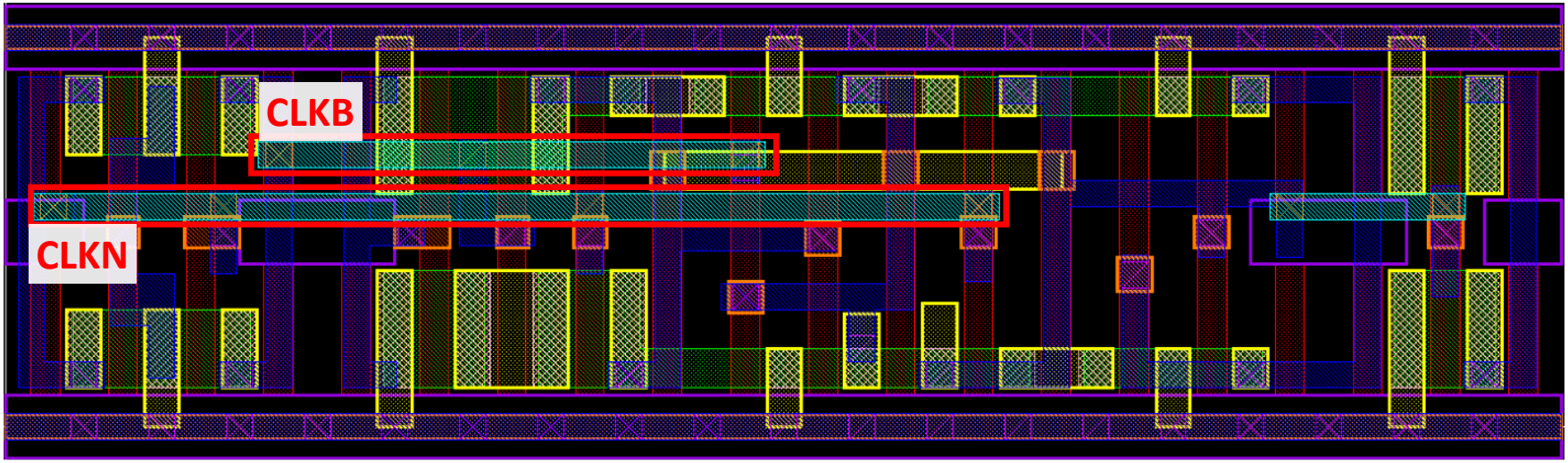
DPA

***HA_X1 (SP&R)**
#F=14, #Net=11

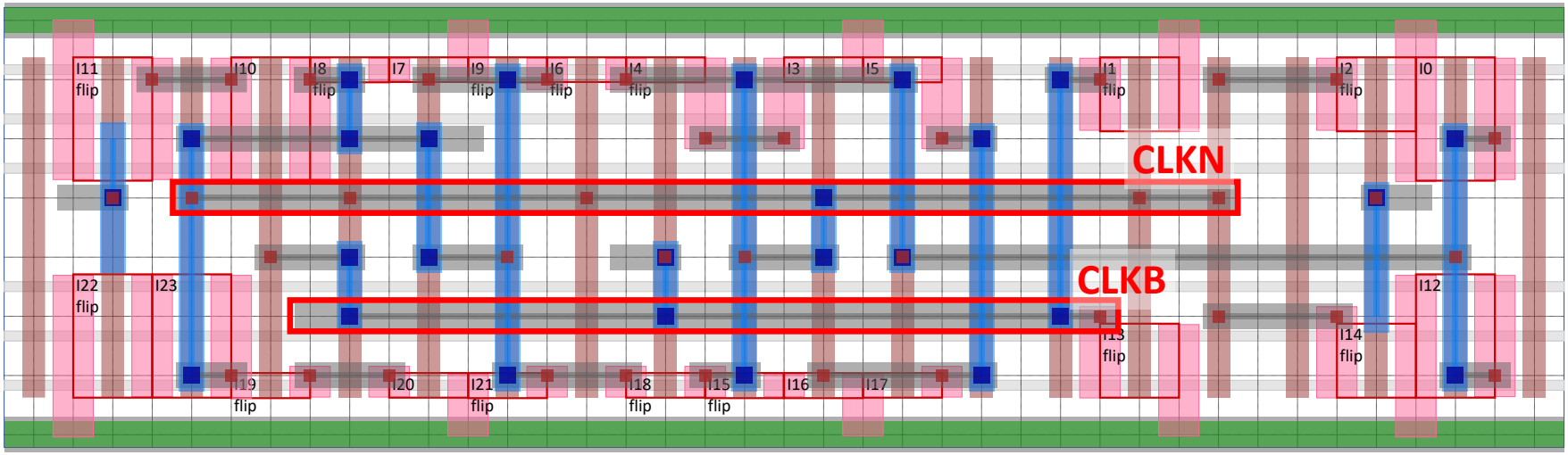
*** Optimized Result**
Cell Size = **10** CPP
Metal Length (ML) = **230**
#M_2 Track = **1**

CROSSTALK MITIGATION

- DFFHQNx1
  - Known layout in ASAP7 PDK library

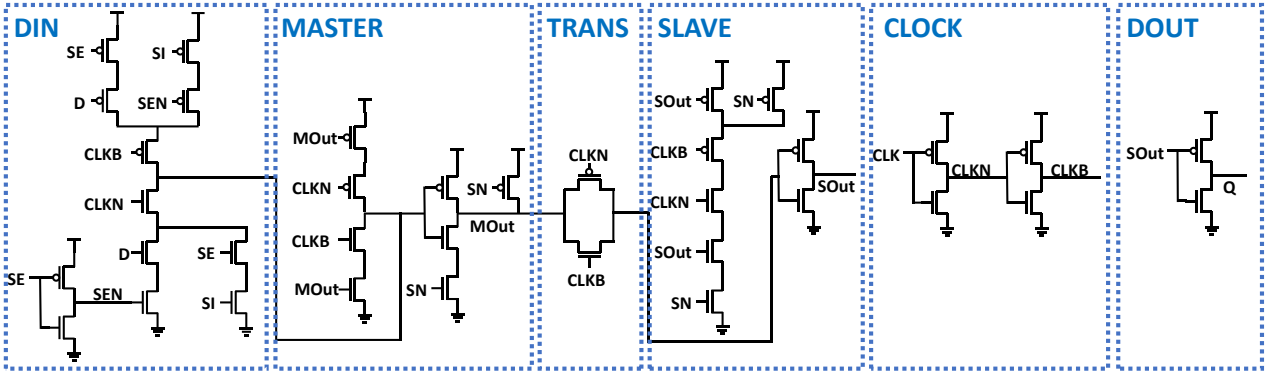


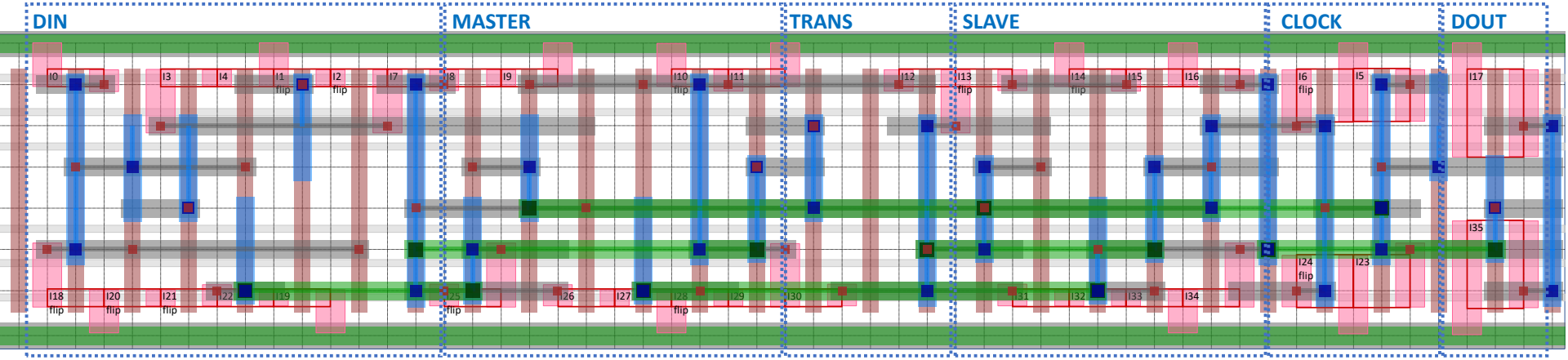
  - Generated layout using SP&R framework



CELL PARTITIONING

- SDFFSNQ_X1
  - 6 Function Modules : DIN, MASTER, TRANS, SLAVE, CLOCK, and DOUT
  - Generation Time: 1.75 Hours (TAT of Cell Design Specialist: 4-5 Hours per one cell layout)

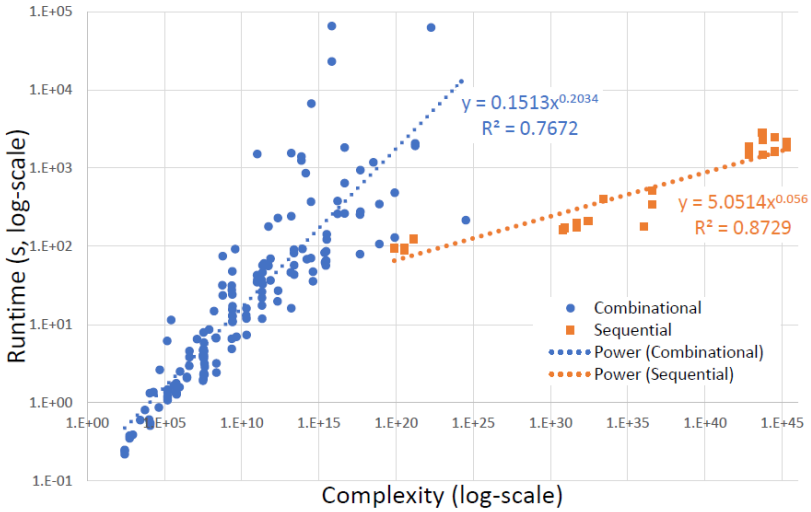




A WHOLE SET OF THE STANDARD CELL LIBRARY (7*NM*)

- Better Results than the State-Of-The-Art Library (ASAP7)
  - Cell Size **1.4%↓** (22.3 → 22.0) , M2 Track Use for routability **63.0%↓** (2.7 → 1.0)

Scalability of SP&R framework for a whole set of library



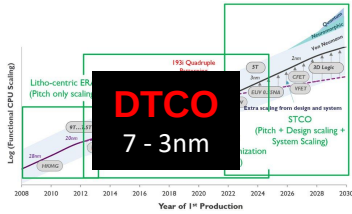
SP&R RESULTS OF 22 LATCH CELLS FROM ASAP7 LIBRARY: #CELL = THE NUMBER OF VARIANTS OF EACH CELL IN COLUMN 1, #FET / #NET = THE NUMBER OF FETS / NETS, M_2 = THE NUMBER OF USED $M2$ TRACKS.

Cell	#FET	#NET	ASAP7 [25]		*SP&R*		Runtime (s)
			Size	M_2	Size	M_2	
DHLx1	16	13	15	2	15	0	95.3
DHLx2	16	13	16	2	16	0	95.8
DHLx3	16	13	17	2	17	0	124.3
DLLx1	16	13	15	2	15	0	93.1
DLLx2	16	13	16	2	16	0	90.0
DLLx3	16	13	17	2	17	0	126.1
DFFHQNx1	24	17	20	2	20	0	170.7
DFFHQNx2	24	17	21	2	21	0	174.6
DFFHQNx3	24	17	22	2	22	0	212.5
DFFHQx4	26	18	25	2	25	0	342.5
DFFLQNx1	24	17	20	2	20	0	173.2
DFFLQNx2	24	17	21	2	21	0	197.5
DFFLQNx3	24	17	22	2	22	0	210.8
DFFLQx4	26	18	25	2	25	1	519.0
SDFHx1	32	23	25	5	25	3	1,880.4
SDFHx2	32	23	26	4	26	3	2,327.2
SDFHx3	32	23	27	4	27	3	2,466.5
SDFHx4	32	23	31	3	28	3	2,184.1
SDFLx1	32	23	25	4	25	2	1,511.3
SDFLx2	32	23	26	4	26	2	1,479.5
SDFLx3	32	23	27	4	27	2	1,632.0
SDFLx4	32	23	31	3	28	2	1,824.8
Average	24.9	18.2	22.3	2.7	22.0	1.0	815.0

PARAMETRIC DTCO STUDY (CELL SCALING)

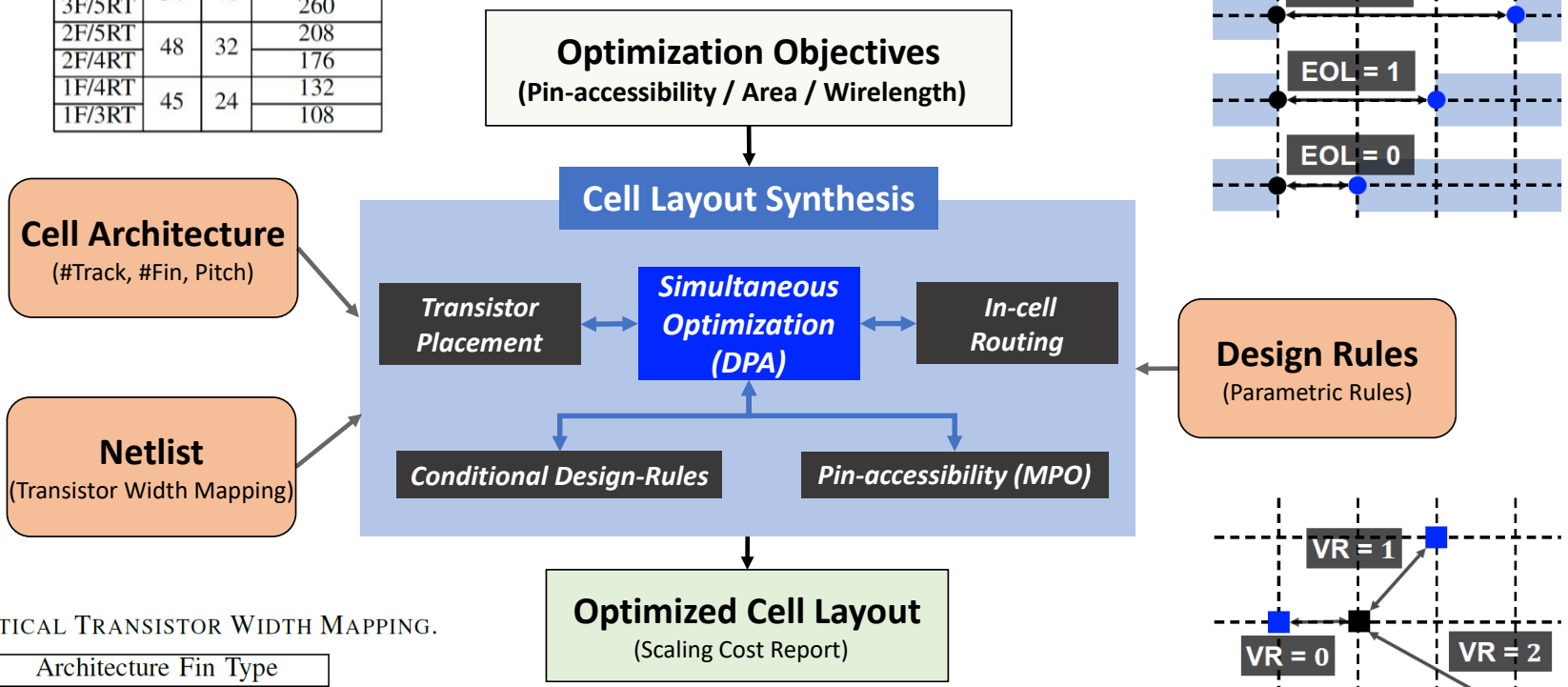
[ISCAS'20]

- Framework can cover possible cell architectures in sub-7nm
- Parametric Study: Estimation of scaling effect w/o real trials



SCALING ARCHITECTURE TYPES: F = FIN, RT = ROUTING TRACK. ALL NUMBERS ARE IN $[nm]$.

Type	CPP	MP	Cell Height
3F/6RT	54	40	300
3F/5RT			260
2F/5RT	48	32	208
2F/4RT			176
1F/4RT	45	24	132
1F/3RT			108

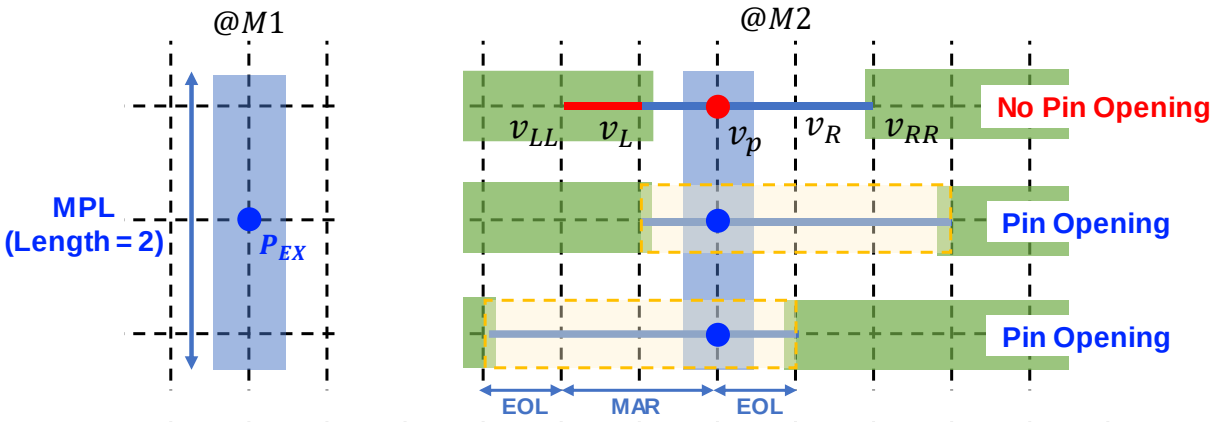


HYPOTHETICAL TRANSISTOR WIDTH MAPPING.

Architecture Fin Type			
7 fins [9]	3 fins	2 fins	1 fin
1/2/3	1		1
4/5	2	2	
6/7	3		

CONSTRAINT-BASED PIN-ACCESSIBILITY IMPROVING [ISCAS'20]

- Strict Constraint-based Ensuring Pin-Accessibility
  - Conventional works improve pin-accessibility through the optimization objective
  - Minimum I/O Pin Length (MPL) , Minimum I/O Pin Opening (MPO)



[MPL Formulation]

$$\mathbf{AL1}(m_{v,v_F}, m_{v,v_B}), \quad \text{if } f_m^n(v, v_D) = 1 \ , \ f_m^n(v, v_U) = 1$$

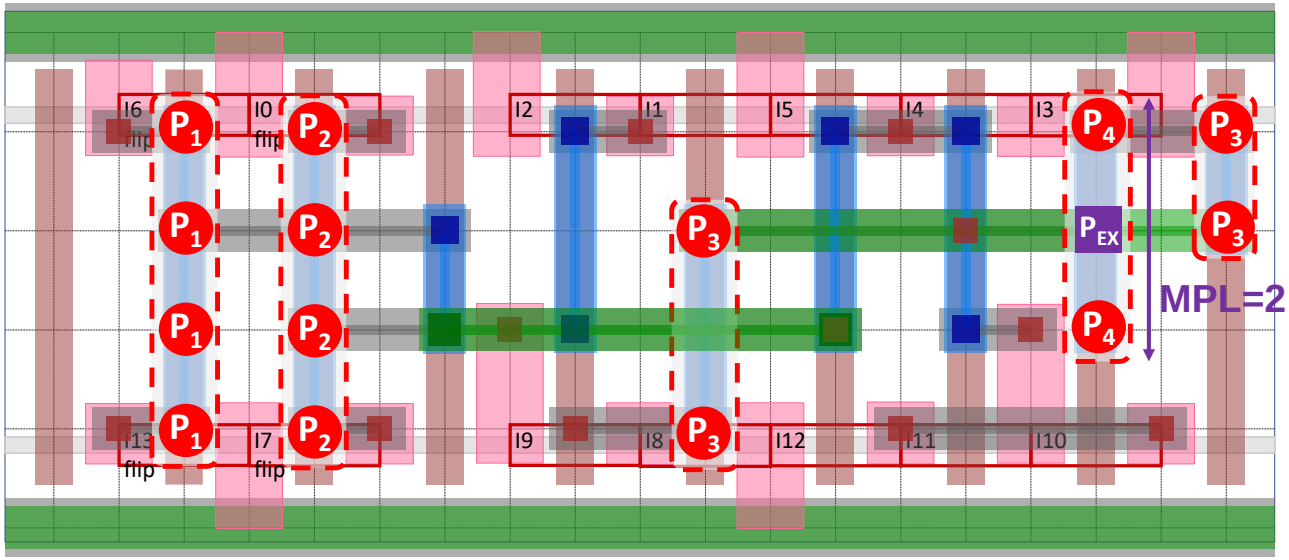
$$\forall v \in V_1, \ m = P_{EX}$$

[MPO Formulation]

$$\mathbf{ALk}(\{O_{v_p} | \ v_p \in Q(p)\}), \quad \text{if } \bigvee_{v \in V_2, u \in V_2} e_{v,u}^{n(p)} = 0$$

$$\overline{O_{v_p}} = \sum_{n \in N, n \neq n(p)} \left((e_{v_{LL},v_L}^n \vee e_{v_L,v_p}^n \vee e_{v_p,v_R}^n) \wedge (e_{v_L,v_p}^n \vee e_{v_p,v_R}^n \vee e_{v_R,v_{RR}}^n) \right),$$

$$\forall v_p \in Q(p), \quad \begin{cases} v \in Q(p), & \text{if } e_{v_D,v_{DF}}^n = 1 \ , \ e_{v_D,v_{DB}}^n = 1 \\ v \notin Q(p), & \text{otherwise} \end{cases}, \forall v \in V_2$$



: Gate
: Source/Drain
: M0
: M0 Signal
: M1
: M1 Signal
: M2
: M2 Signal
: CA
: VIA01
: VIA12
P : Pin Opening on M1

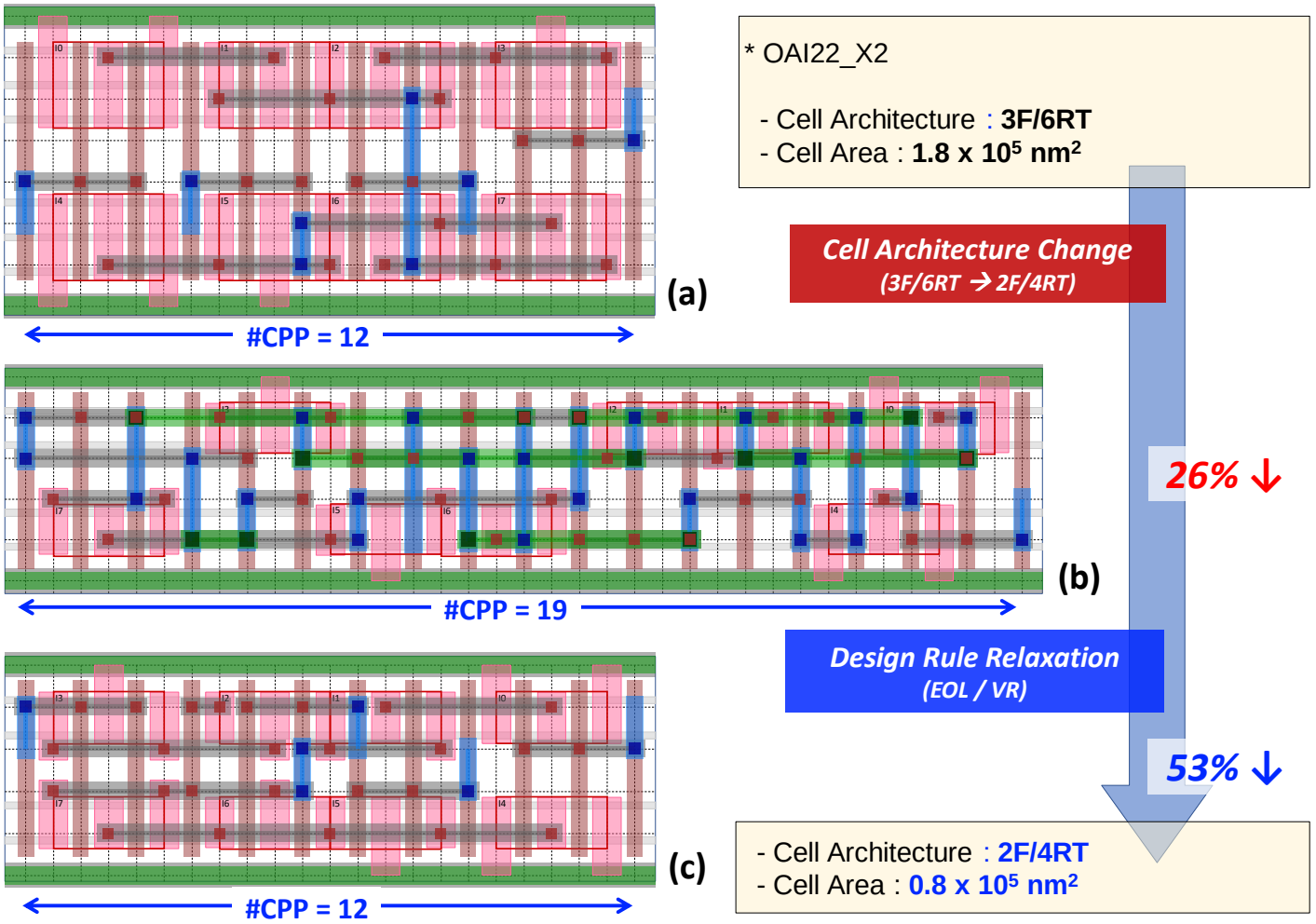
*** HA_X1 :** 4 I/O Pin (P_{EX})
*** Cell Architecture**
: 1 Fin / 4 Routing Track

DTCO THROUGH DESIGN RULE RELAXATION

[ISCAS'20]

*CPP : Contact Poly Pitch

- Identification the specific parameters of design rule involving DTCO
- A Key metric in scaling is maintaining the number of CPP*
  - EOL/VR Relaxation : From 1/1 grid → To 0/0 grid



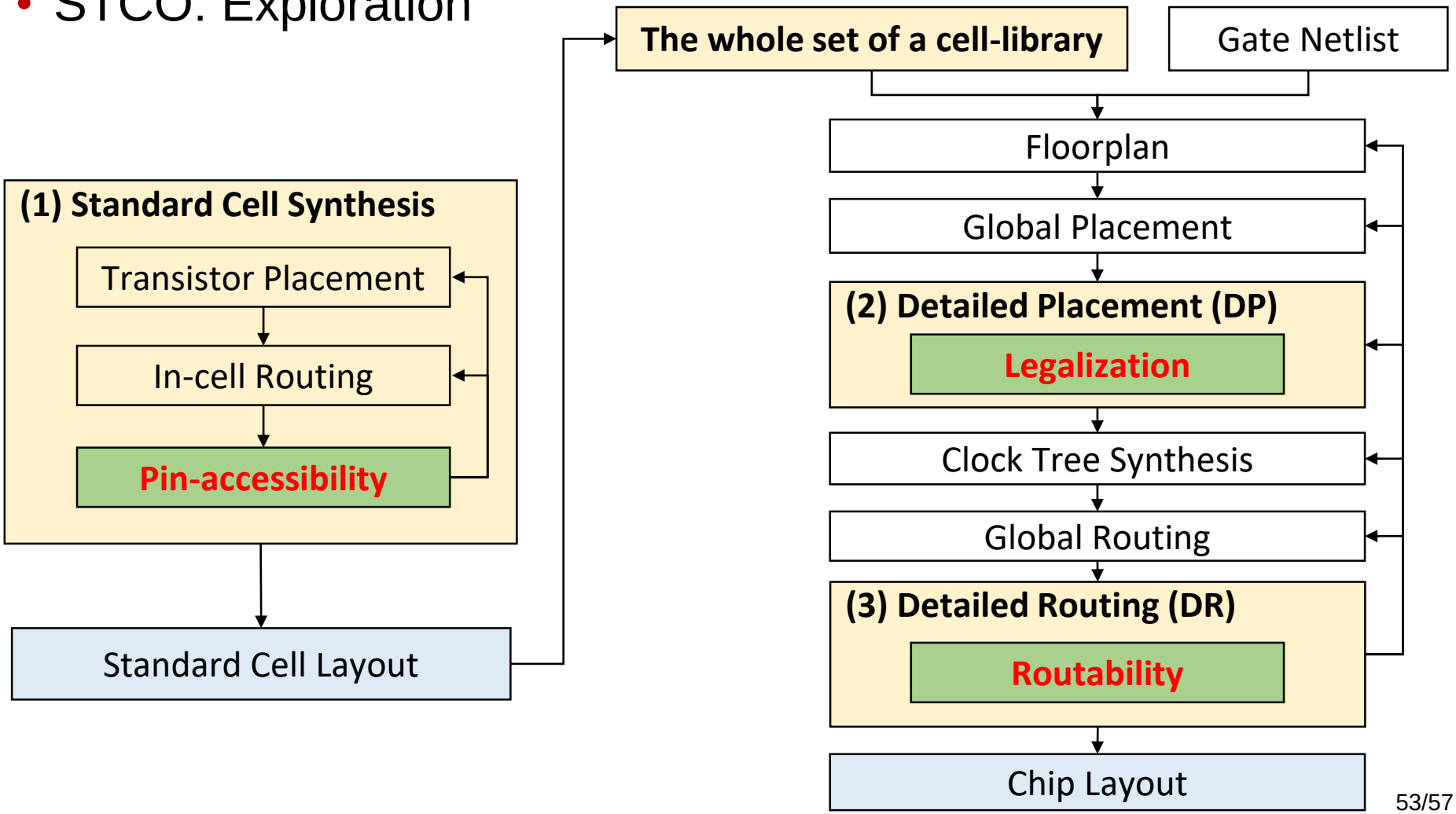
CHAPTER 3 – STANDARD CELL SYNTHESIS

- **SMT-based Simultaneous Place-&-Route Cell Synthesis**
  - Innovative **dynamic pin allocation (DPA)** to integrate P&R
  - SAT's fast reasoning + optimization : **Achieved Better Optimality**
- **Orchestrated Scalability Improvements: up to 36 FET / 27 N**
  - Practical Design Features / Redundancy Removing: Maintained Optimality
  - Practical Search-space Restriction: Tiny Degradation (<0.2%) of ML
- **A whole set of a standard cell library through**
  - Compare to ASAP 7nm library, **Even Better optimality**
  - **1.4%** ↓ of Cell Size (Placement), **63.0%** ↓ of M2 track use (Routability↑)
- **Holistic Exploration for fast-enable DTCO *[ISCAS'20]***
  - With strict constraint-based pin-accessibility improvement: **MPL, MPO**
  - Fast estimation of cell scaling effect: Parametric DTCO study

- *Introduction*
- *Ch.0) Formulation Background*
- *Ch.1) Routability Analysis (ILP/SAT)*
- *Ch.2) Routability Diagnosis (SAT)*
- *Ch.3) Standard Cell Synthesis (SMT)*
- ***Future***

Future Research Plan

- Layout Synthesis: Efficiency and Performance
- DTCO: PDK
- STCO: Exploration



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Pin accessibility Index

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DTCO framework

- K. Jo, S. Ahn, J. Do, T. Song, T. Kim and K. Choi, "Design Rule Evaluation Framework Using Automatic Cell Layout Generator for Design Technology Co-Optimization", IEEE Transactions on Very Large-Scale Integration Systems 27(8) (2019), pp. 1933-1946.

Thank you

SAT FORMULATION

- Flow Feasibility (F)
  - CFC for pins (AMO type) : EO = AMO ∩ ALO (1 clause)

$$\mathbf{F}_{C_1}(v,n,m) = \mathbf{EO}\Big(\{f_m^n(v,p) \mid p \in a(v)\}\Big), \quad \forall v \in V,\ \forall n \in N,\ \forall t_m^n \in T^n$$

  - CFC for grids (non-AMO type)

$$\mathbf{F}_{C_2}(v,n,m) = \bigwedge_{u \in a(v)} \neg f_m^n(v,u) \vee \bigvee_{p,q \in a(v), p \neq q} \Big(f_m^n(v,p) \wedge f_m^n(v,q) \wedge \bigwedge_{u \in a(v), u \neq p, u \neq q} \neg f_m^n(v,u) \Big), \quad \forall v \in V,\ \forall n \in N,\ \forall t_m^n \in T^n$$

  - VE for pins (AMO type)

$$\mathbf{F}_{E_1}(v) = \mathbf{EO}\Big(\{e_{v,u}^n \mid u \in a(v),\ n \in N\}\Big), \quad \forall v \in V,\ v \neq S_o$$

  - VE for grid (AMO type)

$$\mathbf{F}_{E_2}(v) = \mathbf{AMO}\Big(\Big\{ \bigvee_{p \in a(v)} e_{v,p}^n \ \Big|\ n \in N \Big\}\Big), \quad \forall v \in V$$

  - Edge Assignment (EA) : Logical Imply

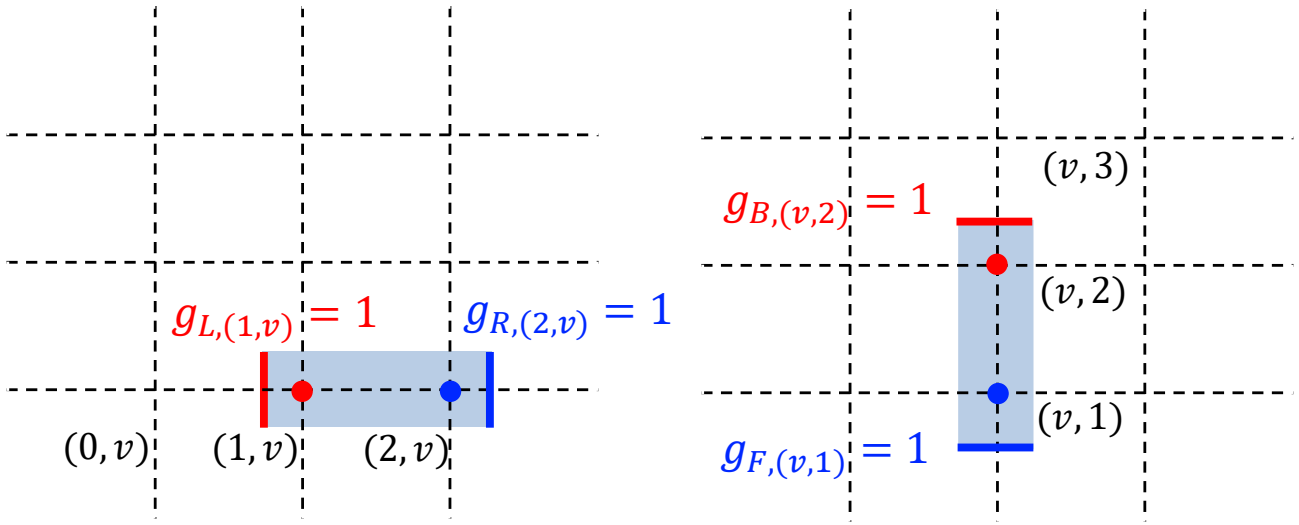
$$\mathbf{F}_{EA}(e_{v,u},n,m) = e_{v,u}^n \vee \neg f_m^n(v,u), \forall e_{v,u} \in E, \forall n \in N, \forall t_m^n \in T^n$$

  - Metal Segment (MS) : AMO type

$$\mathbf{F}_M(e_{v,u}) = \mathbf{EO}\Big(\{\neg m_{v,u}\} \cup \{e_{v,u}^n \mid n \in N\}\Big), \quad \forall e_{v,u} \in E$$

CONDITIONAL DESIGN RULE FORMULATION

- Geometric Variable for BCC
  - End-of-Line indicator of each vertex for design rule constraints



$$g_{L,v} = \neg m_{v_L,v} \wedge m_{v,v_R},$$
$$g_{R,v} = m_{v_L,v} \wedge \neg m_{v,v_R},$$

$$\forall v \in V_2$$

Logical Expression for SAT

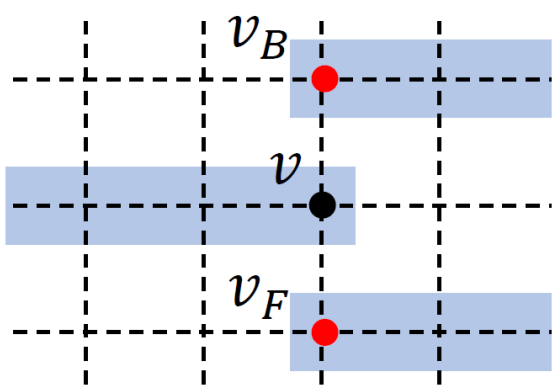
$$g_{L,v} \leq 1 - m_{v_L,v} \; ; \; g_{L,v} \leq m_{v,v_R} \; ; \; g_{L,v} \geq m_{v,v_R} - m_{v_L,v}$$
$$g_{R,v} \leq m_{v_L,v} \; ; \; g_{R,v} \leq 1 - m_{v,v_R} \; ; \; g_{R,v} \geq m_{v_L,v} - m_{v,v_R}$$

Linear Expression for ILP
(Equality or inequality)

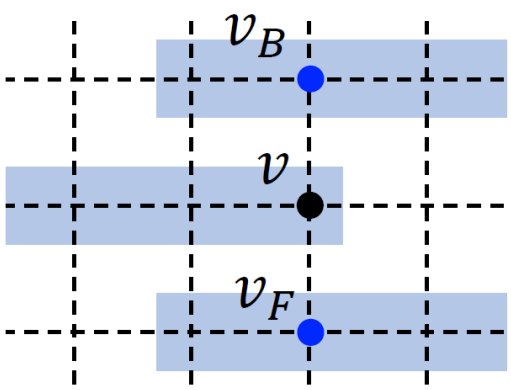
SELF ALIGNED DOUBLE PATTERN-AWARE DESIGN RULES

- Parallel Run Length Rule (PRL)
  - The minimum block space to avoid single point contact mask rule check error
    → The minimum parallel run length(d : PRL param.) between adjacent metal segments

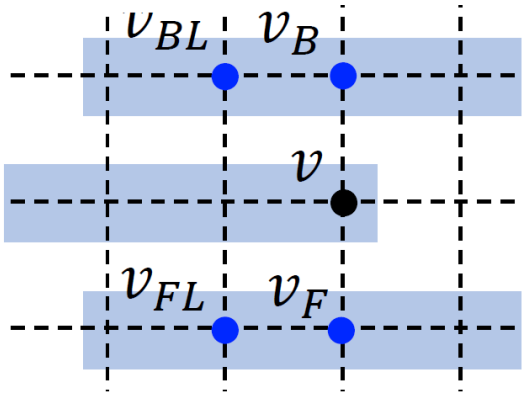
$$if\ d = 2\quad PRL(v) : g_{R,v} + g_{L,v_B} + g_{L,v_{BL}} \leq 1; g_{R,v} + g_{L,v_F} + g_{L,v_{FL}} \leq 1, \forall v \in V_0, V_2$$



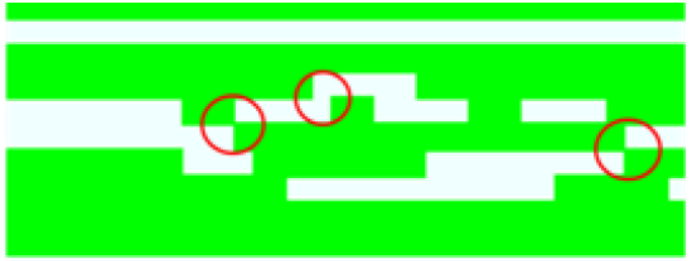
Violation (Single-Point-Contact)

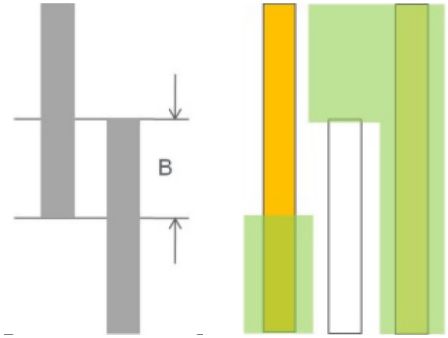


No Violation @ RL = 1



No Violation @ RL = 2





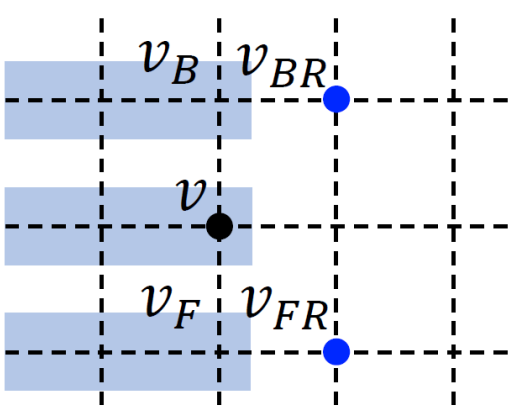
[Figure: Y. Ma et. al, Self-aligned double patterning (SADP) compliant design flow, SPIE 2012]

STEP HEIGHT RULE

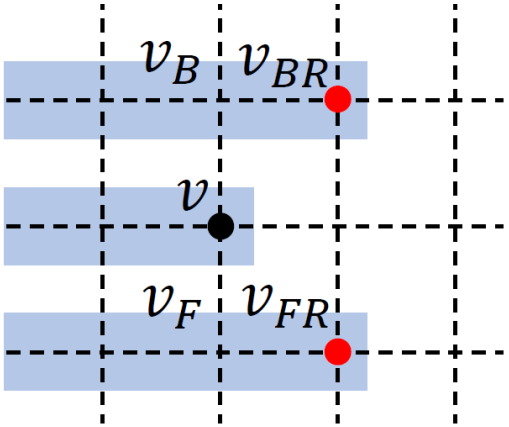
- Step Height Rule (SHR)
  - The minimum block width to avoid small step mask rule check error

    → The minimum step width(d : SHR param.) between adjacent unaligned tips

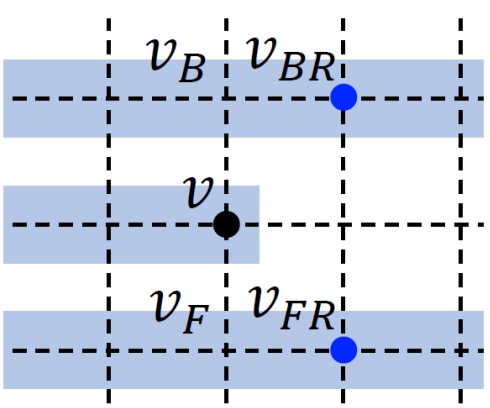
$$if\ d = 2\ \ SHR(v) : g_{R,v} + g_{R,v_{BR}} \leq 1; g_{R,v} + g_{R,v_R} \leq 1, \forall v \in V_0, V_2$$



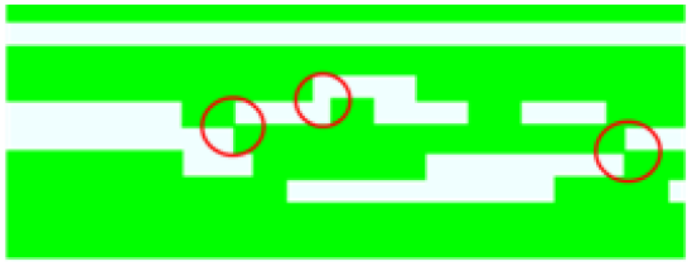
No Violation

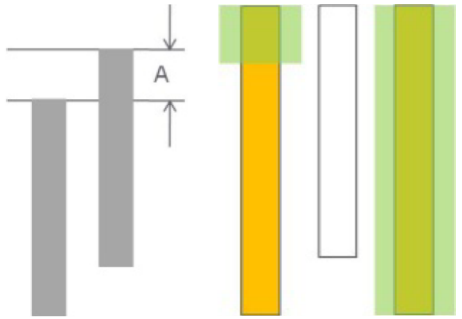


Violation



No Violation





[Figure: Y. Ma et. al, Self-aligned double patterning (SADP) compliant design flow, SPIE 2012]

SAT FORMULATION

- Design Rule Feasibility (D)
  - Geometric Variable (GV) : non-AMO type

$$\mathbf{D}_{GV_L}(v) = (g_{L,v} \wedge \neg m_{v_L,v} \wedge m_{v,v_R}) \vee (\neg g_{L,v} \wedge \neg m_{v,v_R}) \vee (\neg g_{L,v} \wedge m_{v_L,v}), \quad \forall v \in V_2$$

$$\mathbf{D}_{GV_R}(v) = (g_{R,v} \wedge m_{v_L,v} \wedge \neg m_{v,v_R}) \vee (\neg g_{R,v} \wedge \neg m_{v_L,v}) \vee (\neg g_{R,v} \wedge m_{v,v_R}), \quad \forall v \in V_2$$

$$\mathbf{D}_{GV} = \bigwedge_{v \in V} \left(\mathbf{D}_{GV_L}(v) \wedge \mathbf{D}_{GV_R}(v) \wedge \mathbf{D}_{GV_F}(v) \wedge \mathbf{D}_{GV_B}(v) \right)$$

$m_{v_L,v}$	m_{v,v_R}	$g_{L,v}$	D_{GV_L}
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

  - GV-based conditional design rule (AMO type)
    - MAR / EOL / PRL / SHR

$$\mathbf{D}_{M_{LR}}(v) = \mathbf{AMO}(g_{L,v}, g_{R,v}, g_{L,v_R}, g_{R,v_R}), \quad \forall v \in V_2$$

$$\mathbf{D}_{E_R}(v) = \mathbf{AMO}(g_{R,v}, g_{L,v_{FR}}) \wedge \mathbf{AMO}(g_{R,v}, g_{L,v_{BR}}) \wedge \mathbf{AMO}(g_{R,v}, g_{L,v_R}, g_{L,v_{RR}}), \quad \forall v \in V_2$$

$$\mathbf{D}_{P_R}(v) = \mathbf{AMO}(g_{R,v}, g_{L,v_B}, g_{L,v_{BL}}) \wedge \mathbf{AMO}(g_{R,v}, g_{L,v_F}, g_{L,v_{FL}}), \quad \forall v \in V_2$$

$$\mathbf{D}_{S_R}(v) = \mathbf{AMO}(g_{R,v}, g_{R,v_{BR}}) \wedge \mathbf{AMO}(g_{R,v}, g_{R,v_{FR}}), \forall v \in V_2$$

$$\mathbf{D}_M = \bigwedge_{v \in V} \left(\mathbf{D}_{M_{LR}}(v) \wedge \mathbf{D}_{M_{FB}}(v) \right)$$

$$\mathbf{D}_E = \bigwedge_{v \in V} \left(\mathbf{D}_{E_L}(v) \wedge \mathbf{D}_{E_R}(v) \wedge \mathbf{D}_{E_F}(v) \wedge \mathbf{D}_{E_B}(v) \right)$$

$$\mathbf{D}_P = \bigwedge_{v \in V} \left(\mathbf{D}_{P_L}(v) \wedge \mathbf{D}_{P_R}(v) \wedge \mathbf{D}_{P_F}(v) \wedge \mathbf{D}_{P_B}(v) \right)$$

$$\mathbf{D}_S = \bigwedge_{v \in V} \left(\mathbf{D}_{S_L}(v) \wedge \mathbf{D}_{S_R}(v) \wedge \mathbf{D}_{S_F}(v) \wedge \mathbf{D}_{S_B}(v) \right)$$

  - Metal-based design rule (VR)

$$\mathbf{D}_V(v) = \mathbf{AMO}(m_{v,v_U}, m_{v_R,v_{UR}}, m_{v_B,v_{UB}}, m_{v_{BR},v_{UBR}}) \wedge \mathbf{AMO}(m_{v_D,v}, m_{v,v_U}), \quad \forall v \in V$$

COMPLEXITY OF ENCODING TECHNIQUES FOR BCC

- SAT Encodings for At-Most-One (AMO) constraint
  - Commander Encoding: Most efficient in terms of number of clause in AMO

Table 1: A summary of most well-known AMO SAT-encodings, where some encodings come from cardinality constraints noted by CAR

enc	*clauses*	*aux vars*	*UPaAC*	*origin*
pairwise	$\binom{n}{2}$	0	yes	folklore
linear (CAR.)	$8n$	$2n$	no	[44]
totalizer	$O(n^2)$	$O(nlog(n))$	yes	[7]
binary	$nlog_2 n$	$\lceil log_2 n \rceil$	yes	[19]
sequential counter	$3n-4$	$n-1$	yes	[40]
sorting networks (CAR.)	$O(nlog_2^2 n)$	$O(nlog_2^2 n)$	yes	[15]
commander	$\sim 3n$	$\sim \frac{n}{2}$	yes	[26]
product	$2n+4\sqrt{n}+O(\sqrt[4]{n})$	$2\sqrt{n}+O(\sqrt[4]{n})$	yes	[14]
card. networks(CAR.)	$6n-9$	$4n-6$	yes	[5]
PHFs-based (CAR.)	$nlog_2 n$	$\lceil log_2 n \rceil$	yes	[10]
bimander	$\frac{n^2}{2m}+nlog_2 m-\frac{n}{2}$	$log_2 m, 1 \le m \le n$	yes	[24]
bimander ($m=\frac{n}{2}$)	$nlog_2 n-\frac{n}{2}$	$\lceil log_2 n \rceil - 1$	yes	[24]

** Nguyen, Van-Hau, and Son T. Mai. "A new method to encode the at-most-one constraint into SAT." Proceedings of the Sixth International Symposium on Information and Communication Technology. ACM, 2015.*

Pairwise

$pairwise\_AMO\{a, b, c, d, e, f\}$

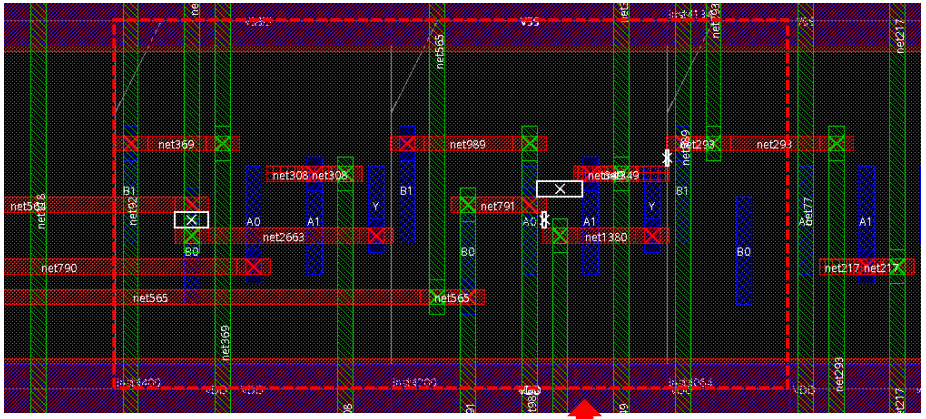
Commander

$pairwise\_AMO\{C_1, C_2\}$

$pairwise\_EO\{\neg C_1, a, b, c\}$

$pairwise\_EO\{\neg C_2, d, e, f\}$

DRV Diagnosis Examples (From Commercial Tool)

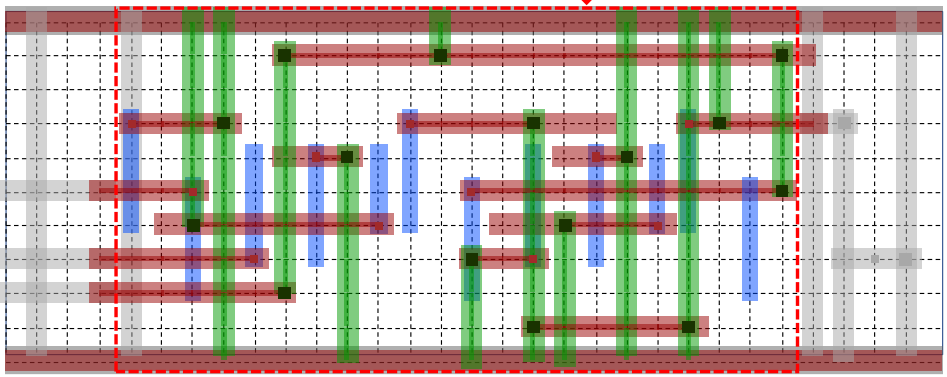


: DRV

Region I

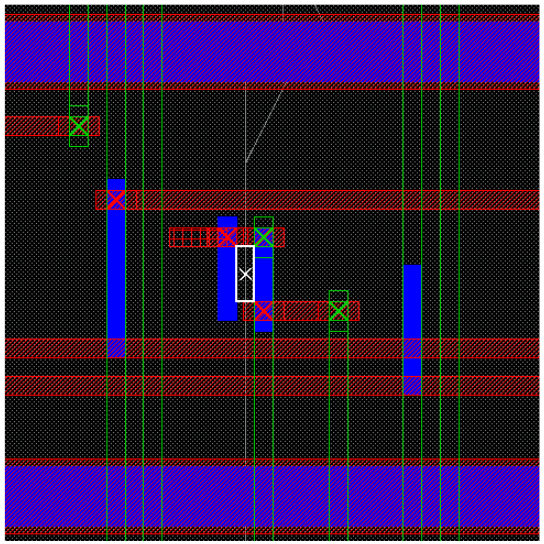
Unroutable
(4 DRVs)

The Same Switchbox



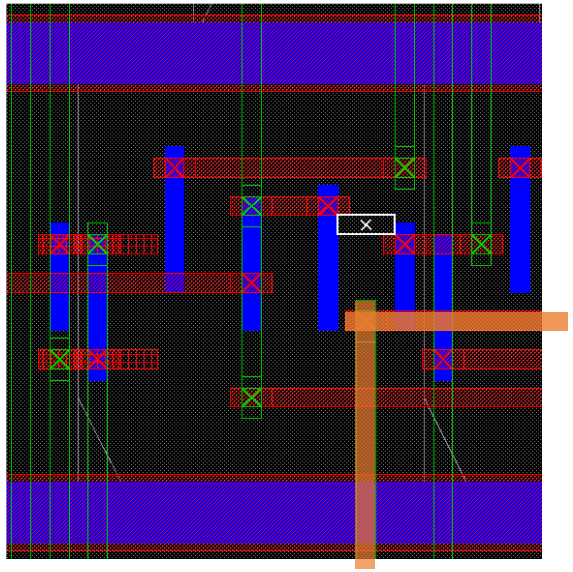
: M1
: M2
: M2 Signal
: M3
: M3 Signal
: VIA12
: VIA23
: Blockage

Routable



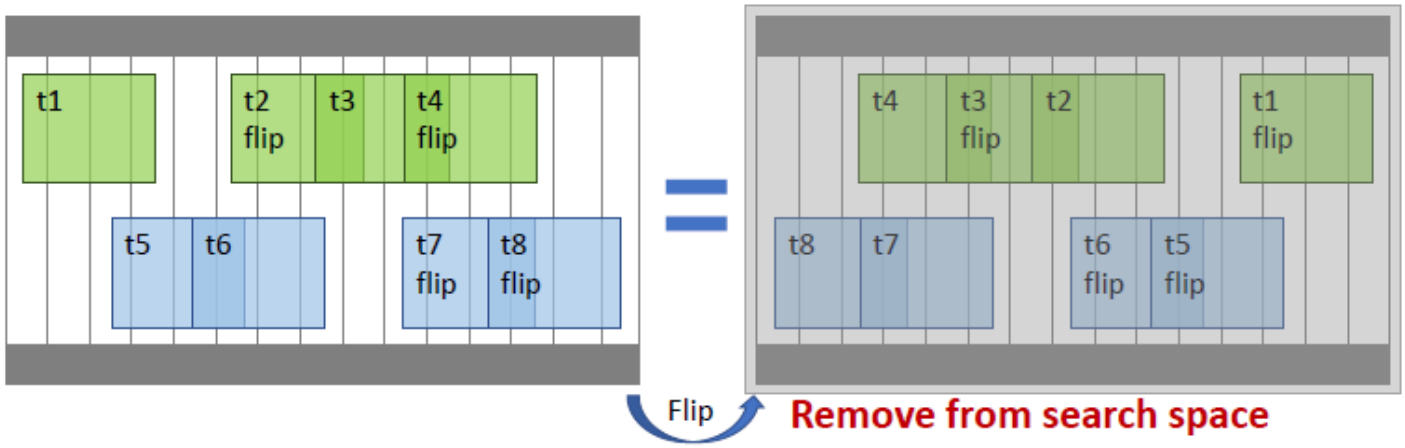
DRV
Obstacle

(a) Intrinsic CP



(b) Obstacle CP

FLIPPING OF WHOLE CELL DESIGN



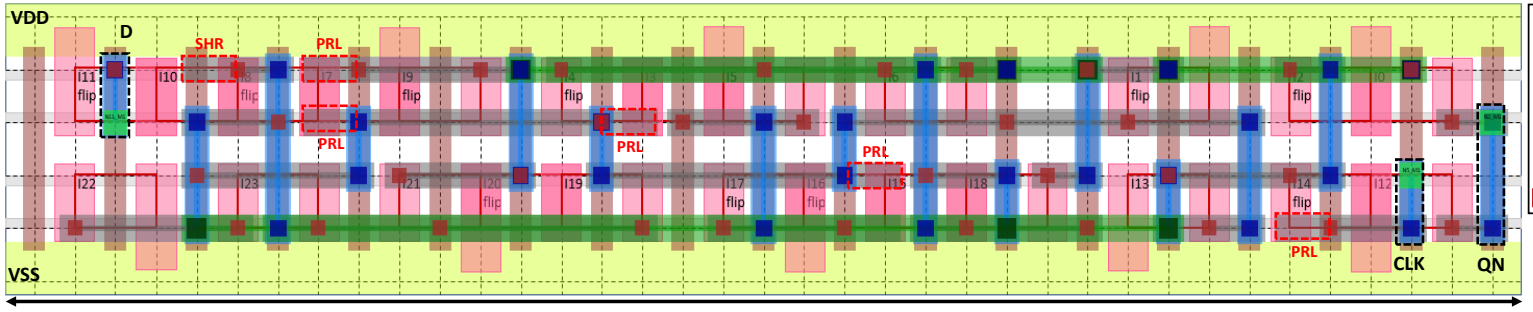
Ex1) Even #P-FET : 1, 2, 3, 4

(1, 2) (3, 4)	(1, 2)<(3, 4)	K=1
(1, 3) (2, 4)	(1, 3)<(2, 4)	K=2
(1, 4) (2, 3)	(1, 4)<(2, 3)	K=3
(2, 3) (1, 4)	~~(2, 3) (1, 4)~~	
(2, 4) (1, 3)	~~(2, 4) (1, 3)~~	
(3, 4) (1, 2)	~~(3, 4) (1, 2)~~	

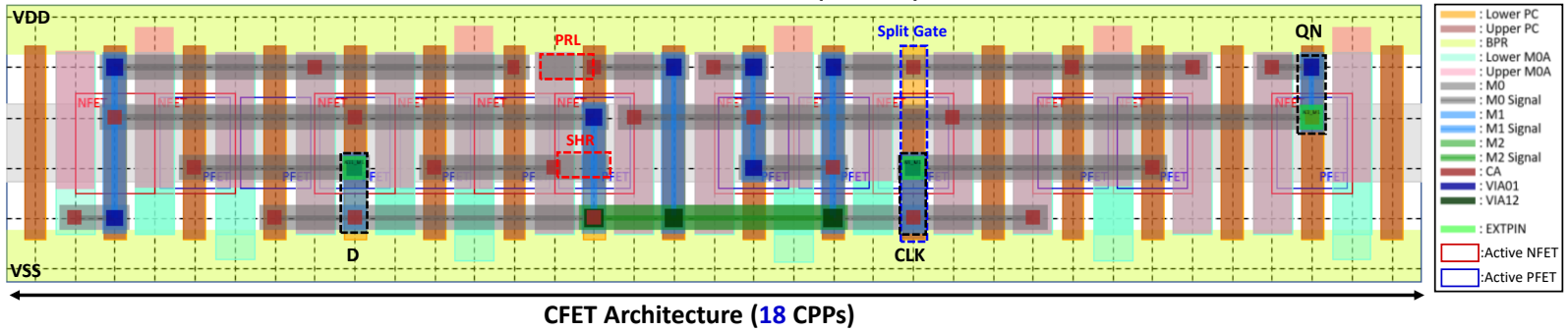
Ex2) Odd #P-FET : 1, 2, 3, 4, 5

(2, 3) (1) (4, 5)	(1, 3) (2) (4, 5)	(1, 2) (3) (4, 5)	(1, 2) (4) (3, 5)	(1, 2) (5) (3, 4)
(2, 4) (1) (3, 5)	(1, 4) (2) (3, 5)	(1, 4) (3) (2, 5)	(1, 3) (4) (2, 5)	(1, 3) (5) (2, 4)
(2, 5) (1) (3, 4)	(1, 5) (2) (3, 4)	(1, 5) (3) (2, 4)	(1, 5) (4) (2, 3)	(1, 4) (5) (2, 3)
~~(3, 4) (1) (2, 5)~~	~~(3, 4) (2) (1, 5)~~	~~(2, 4) (3) (1, 5)~~	~~(2, 3) (4) (1, 5)~~	~~(2, 3) (5) (1, 4)~~
~~(3, 5) (1) (2, 4)~~	~~(3, 5) (2) (1, 4)~~	~~(2, 5) (3) (1, 4)~~	~~(2, 5) (4) (1, 3)~~	~~(2, 4) (5) (1, 5)~~
~~(4, 5) (1) (2, 3)~~	~~(4, 5) (2) (1, 3)~~	~~(4, 5) (3) (1, 2)~~	~~(3, 5) (4) (1, 2)~~	~~(3, 4) (5) (1, 2)~~

CONVENTIONAL FET VS C-FET



Conventional Architecture (19 CPPs)



CFET Architecture (18 CPPs)

***DFFHQN**
#FET=24
#Net=17

***DPA* [15]**

*** Optimized Layout (Conv.)**
Cell Size = **19** CPPs
Metal Length (ML) = **616**
#M_2 Track = **2**

DCPA

*** Optimized Layout (CFET)**
Cell Size = **18** CPPs
Metal Length (ML) = **300 (51.3%)**
#M_2 Track = **1 (50.0%)**