JINGWEI LU

Santa Clara, CA | francesco.ljw@gmail.com | LinkedIn | Google Scholar

PROFESSIONAL SUMMARY

Proven talent at planning, orchestration and execution system covering science, technology and management. Technical strength in high-level & low-level system tech design (HLD & LLD), science strategic design, ambiguity taming, cross-functional collaboration, resources coordination, task planning, etc. Exceptional on aligning application design strategy and objectives with established technology development and research paradigms to achieve maximum operational impacts with minimum obstacles. Growth and innovative mindset over software feature invention and system performance optimization. Skilled professional on keen interpersonal, communicational, organizational and resource allocation expertise. Solid research experience with 15+ publications, 50+ articles review and 400+ citations.

CORE COMPETENCIES

Last Mile Tech & Mgmt	System HLD & LLD	Planning Systems	Orchestration & Execution
Software Engineering	Machine Learning	Algorithm Design	Data Structures
Project Management	Performance Enhancement	Application Design	Process Automation

PROFESSIONAL EXPERIENCE

AMAZON.COM, INC., SANTA CLARA, CA, MARCH 2022 TO PRESENT

SENIOR SOFTWARE DEVELOPMENT ENGINEER (L6, Manager Level), Last Mile Planning (LMP).

- Core technical contributor in Sub Same-Day (SSD) planning team serving world-wide order deliveries within average 6 hours between customer click and promised delivery time. Responsibilities covering a wide scope of planning and optimization services for delivery stations orchestration and on-road transporters execution, including but not limited to, route planning, dispatch planning, sector planning, pick planning, geospatial processing, etc.
- Sole tech lead on the development of the next generation SSD planning system for the combined optimization of Under-The-Roof (UTR i.e. delivery station) orchestration and On-The-Road (OTR i.e. transporter) execution efficiency.
  - High-level design (HLD) of SSD planning system functionality and architecture concerning multiple workflows and services, aligning objectives towards optimal in-station operational efficiency and on-road transiting and servicing performance.
  - Low-level design (LLD) requirements specification for the individual service components creation or evolvement with functionality decomposition, artifacts model definition, storage request formation, race condition handling, etc.
  - Lead collaboration between multiple cross-functional planning, orchestration and execution teams, including customer shopping experience, packages snapshotting, packages picking orchestration, route planning, route dispatching, transporter assignment.
- Strategic and technical contributions to the adaptive sector planning services for SSD delivery stations with algorithm design, system design, tech implementation, shadow testing, station piloting and launching, etc..
  - Develop contraction hierarchy based data structure over station jurisdiction using effective shortcuts insertion and vertices contraction within the road network graph, enforcing one-way search path ordering and reducing the planar graph down to one dimensional.
  - Design, implement and test shortest path search using contraction hierarchy query to support packages clustering, reducing search complexity from $O(N^2)$ down to $O(N)$. The search runtime consumption is shortened by in average 20x and up to 35x over all the road network graph use cases.
  - Develop input fetching component to snapshot the up-to-date SSD station layout and UTR resources status per sector planning demand.

CADENCE DESIGN SYSTEMS, INC., SAN JOSE, CA, JANUARY 2014 TO FEBRUARY 2022

SENIOR PRINCIPAL SOFTWARE ENGINEER (L7, Senior Manager Level), Research and Development (R&D)

- Core R&D team member for Innovus Implementation Systems, the top-2 software product in EDA industry for the back-end flow of digital IC design and signoff, which generated roughly $800M annual revenue for Cadence in 2020.
- Solely incubated the **mixed placer technology**. Lead a **cross-functional R&D team** for the technology prototyping, including literature research, mathematical derivation and modeling, proof of concepts, algorithm development and implementation, empirical validation, etc.
  - Devised and integrated the technology into the automated generation framework of complex floorplans for hundreds of macros instead of utilizing manually designed macro layout.
  - Implemented and verified this technology with significantly improved system performance, power consumption, and chip area (manufacturing cost) each by up to 10%, respectively.

  - Cut down the placement turnaround time from several weeks of manual labor to only a few hours of software automation, which dramatically shortened the time-to-market of IC design products and saved the engineering resources.
  - Received broad recognition from many customers, procured and deployed a **supplemental license** for this new feature of mixed placement technology, producing **significant additional revenue** by this new license every fiscal year.
- Devised and implemented a multi-thread multi-level recursive **partitioner** to support **cross-functional product demands**. This utility minimizes the user specified objective costs (e.g., total amount of network cuts, network levels, etc.), satisfies the user specified partitioning constraints (e.g., partition weight balancing, preassigned partition indexes, predetermined partition capacities), and consumes negligible runtime. It provides a generalized partitioning infrastructure and is being widely applied across multiple different domains of product features.
- Examined, analyzed, and migrated the software product towards **massive parallelism** infrastructure, such as multi-thread and distributed platforms, ensured significant runtime reduction thus good scalability w.r.t. the number of threads and machines. The product performance remains consistent across different platforms, which ensures customer experience. Reformed object-oriented programming design structure to purge coding redundancies and facilitate coding management and maintenance.

Other Projects

Numerical Methods for VLSI Placement, Ph.D. Dissertation[9] and Followup Works, June 2012 to April 2016

- Conceptualized, designed, and delivered three algorithm prototypes, *ePlace*[1,2], *ePlace-MS*[1,3] and *ePlace-3D*[4], for billion-scale numerical VLSI placement of standard-cell, mixed-size and three-dimensional integrated circuits. Remained the finest placement algorithm in the world since published in 2014 with a multitude of applications across over 90% modern research works and products. All the three works are positively commented in Google's recent Nature paper (June 09, 2021) on graph placement.
- Realized an average of 5% (up to 40%) cost (wirelength) reduction and $3\times$ (up to $15\times$) speedup v.s. state-of-the-art placement software and algorithm prototypes. Speech invitations from multiple research and industrial institutions, including *The Chinese University of Hong Kong*, *Intel*, *IBM*, *Cadence Design Systems Inc.*, *Synopsys*, *Xilinx Inc.*, etc.

Machine Learning, Stanford Online Coursework and Followup Works, February 2018 to Present

- Apply robust knowledge and understanding of mathematics with deep experience in machine learning theory and concepts, including bias and variance, measurement criteria, maximum likelihood estimation (MLE) and maximum a posteriori (MAP), principal component analysis (PCA), gradient descent, overfit and underfit, loss function, pre-processing, and regularization.
- Utilize complex machine learning models: regression, classification, clustering, neural network and deep learning, etc.

Selected Publications

[1] **J. Lu**, P. Chen, C.-C. Chang, L. Sha, D. J.-H. Huang, C.-C. Teng and C.-K. Cheng, "ePlace: Electrostatics Based Placement Using Nesterov's Method", *ACM/IEEE DAC* 2014, pp. 1-6 (**best paper nomination**, 12 out of 174 papers, 787 submissions).

[2] **J. Lu** and C.-W. Sham, "LMgr: A Low-Memory Global Router with Dynamic Topology Update and Bending-Aware Optimum Path Search", *IEEE ISQED* 2013, pp. 231-238 (**best paper award**, 3 out of 114 papers).

[3] **J. Lu**, W.-K. Chow, C.-W. Sham and E. F. Y. Young, "A Dual-MST Approach for Clock Network Synthesis", *ACM/IEEE ASP-DAC* 2010, pp. 467-473 (**best paper nomination**, 13 out of 115 papers, 340 submissions).

Awards and Honors

Technical reviewers of *IEEE TCAD*, *ACM TODAES*, *IEEE TVLSI*, *ACM/IEEE DAC*, *ACM/IEEE ICCAD*, etc. 2014 - Present

SHINE (Catalyst, Team Player) Awards at *Cadence Design Systems, Inc.* 05/2017, 06/2017

Cadence Well Done! Awards at *Cadence Design Systems, Inc.* 01/2014, 01/2017, 02/2017

Best paper nomination[1] (1st author) at *ACM/IEEE DAC 2014* (12 out of 174 papers, 787 submissions, top 1.5%) 06/2014

Best paper award[5] (1st author) at *IEEE ISQED 2013* (3 out of 114 papers, top 2.6%) 03/2013

Best paper nomination[6] (1st author) at *ACM/IEEE ASP-DAC 2010* (13 out of 115 papers, 340 submissions, top 3.8%) 01/2010

Jacobs fellowship at *University of California, San Diego* ($\sim$10 out of $400+$ students, $2,200 per month) 09/2010 - 06/2013

Research studentship at *The Hong Kong Polytechnic University* (HK$12,800 per month) 03/2008 - 02/2010

Chu Kochen Honors Program (Mixed Class) at *Zhejiang University* (350 out of $5000+$ students, top 7%) 10/2002 - 06/2006

Education and Credentials

Ph.D. in Computer Science, *University of California, San Diego*, GPA 3.79 09/2010 - 12/2014

M.Phil. in Electronic and Information Engineering, *The Hong Kong Polytechnic University*, GPA 4.00 02/2008 - 02/2010

B.Sc. in Information Engineering, *Zhejiang University*, major course GPA 3.87 10/2002 - 06/2006