International Workshop on Power and Time Modeling, Optimization and Simulation

Clock Network Synthesis with Concurrent Gate Insertion

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Overview of Presentation

- Background Information
  - Clock network synthesis
  - Clock gate insertion
- Our Contributions
  - Topology construction
  - Concurrent gate insertion
  - Slew table construction
- Experimental Results
- Q & A

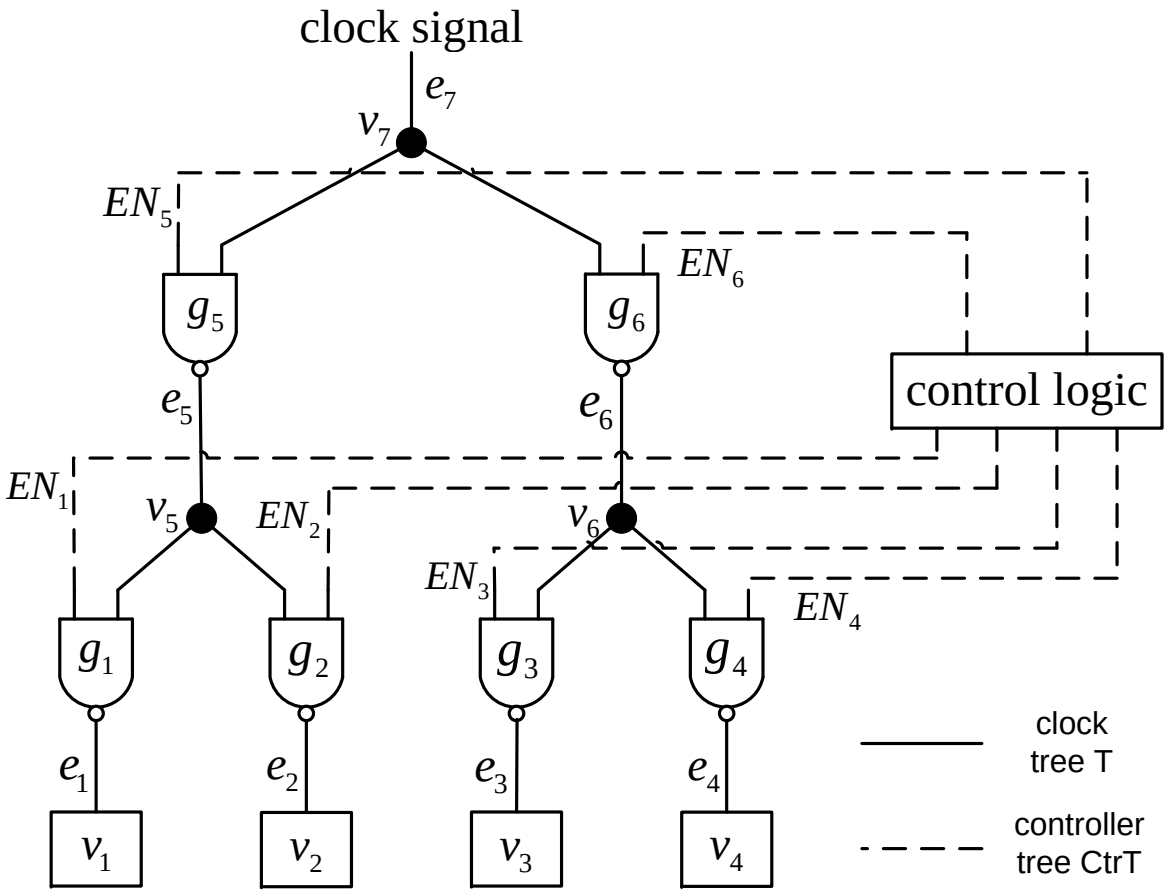
Clock Network Synthesis (CNS)

- Applied before routing for synchronization on the digital circuits
- Connect the clock signal source to all the sinks (flip-flops/memory cells) on the chip
- Customized buffer insertion and wire width
- Four metrics for evaluation
  - Clock Skew
  - Power Consumption
  - Transition Time
  - Variation Tolerance

Clock Gating Design

- An extended work based on clock network synthesis
- Gate insertion instead of buffers to disable the idle clock sections
- Other than the clock tree, an independent controller tree will be built up connecting all the gates to the control logic
- Use activity patterns to manage the active and idle clock periods

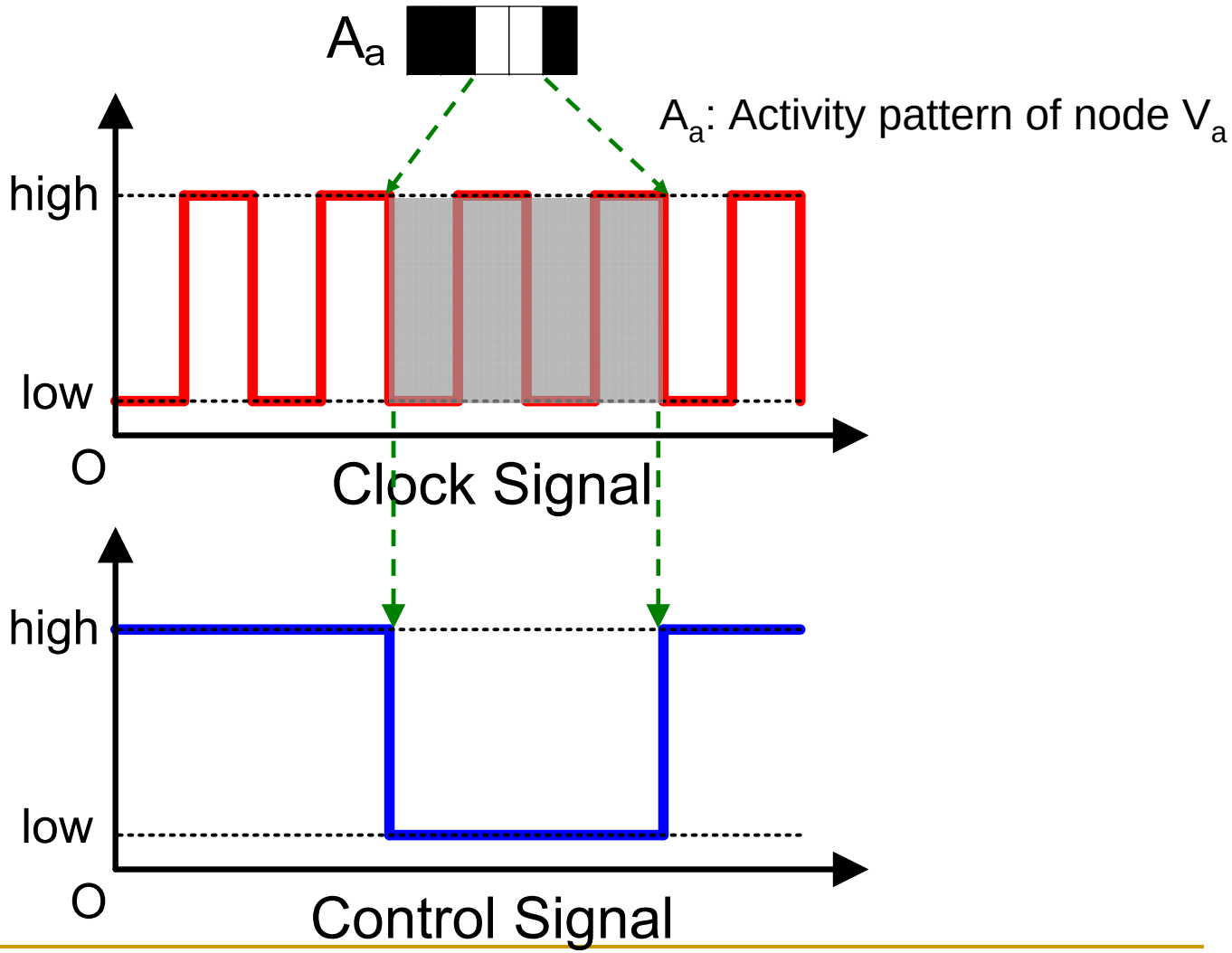
Gated Clock Tree



Activity Pattern

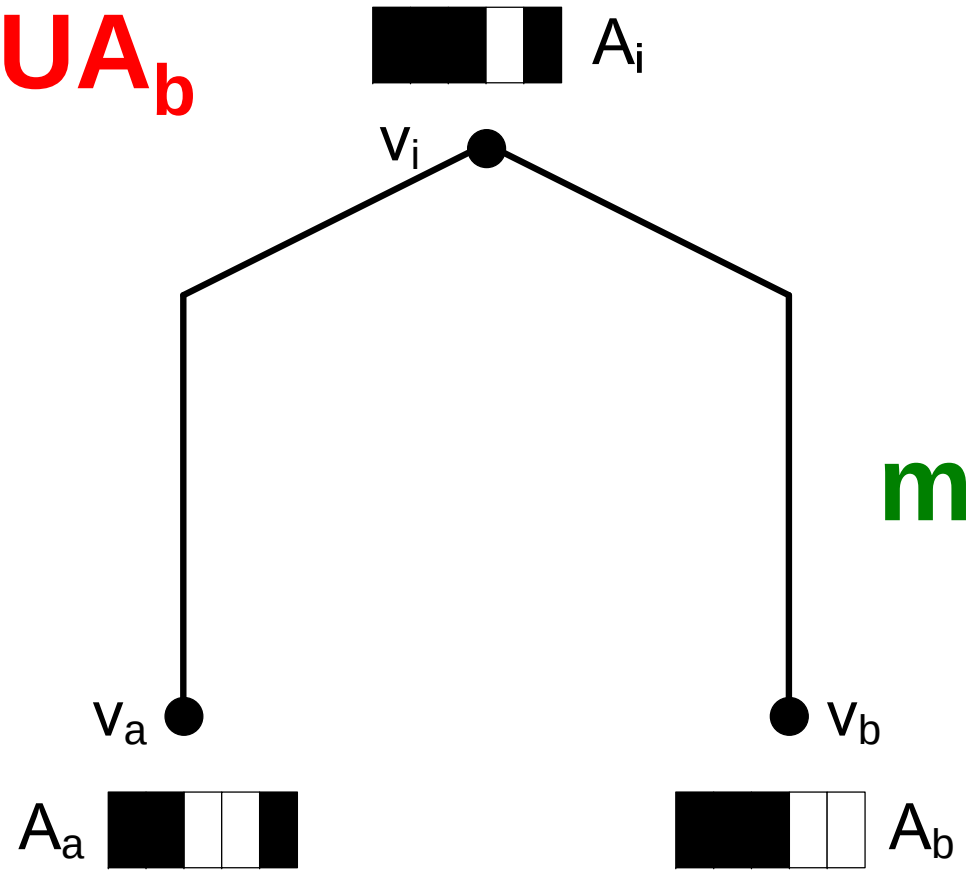
- Active period
  - A proper clock signal should be provided to this clock sink
  - The clock signal consumes dynamic power
- Idle period:
  - No clock signal is needed to be provided to this clock sink
  - No power is consumed for the clock signal

Power Consumption



Activity Pattern of the Clock Tree

$A_i = A_a U A_b$



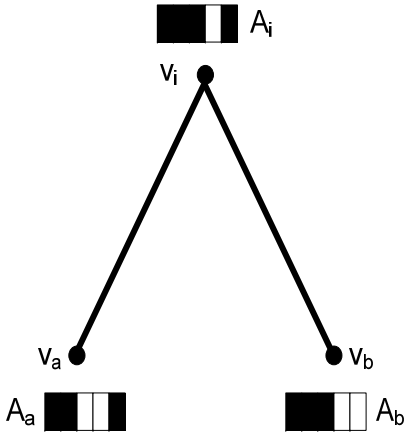
merge

Power Consumption

- Power Consumption
  - $0.5 * a * C_d * f * V_{dd}^2$

C_d: total capacitance
f: clock frequency
V_{dd}: voltage supply

- Switched capacitance (SC)



$$SC_{CLK} = C_{CLK} \times P(A_i)$$

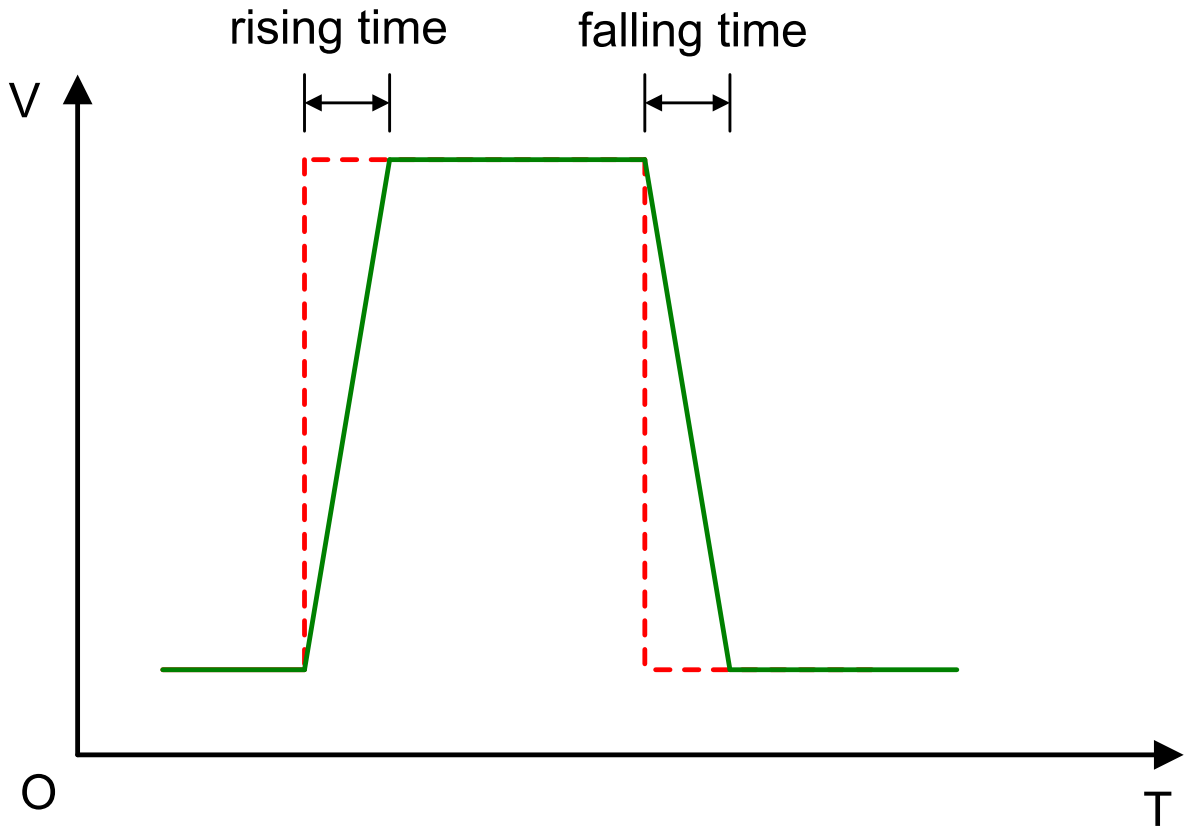
$$SC_{CTR} = C_{CTR} \times P_{tr}(A_i)$$

$$P(A_i) = \frac{AT_{no}(A_i)}{Len(A_i)},\ \text{node activity}$$

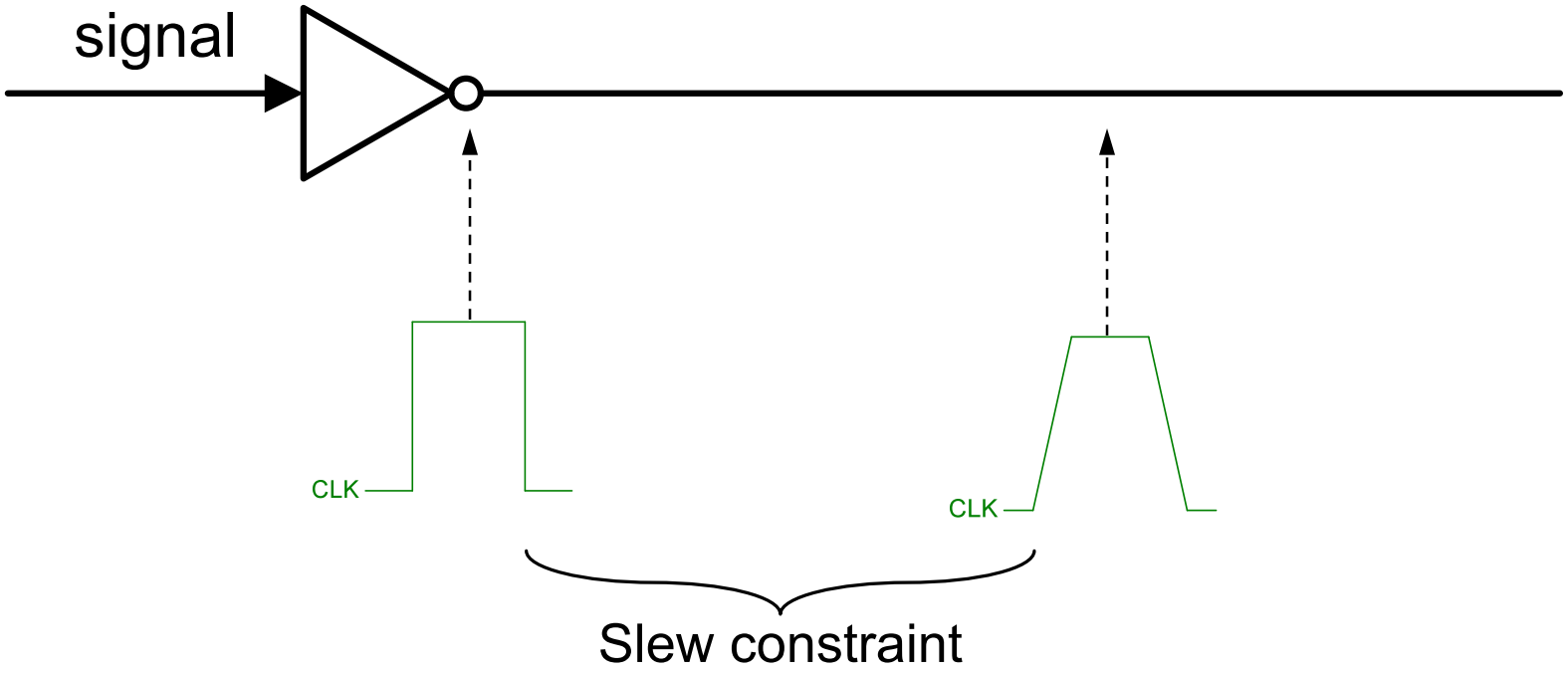
$$P_{tr}(A_i) = \frac{TR_{no}(A_i)}{2 \times (Len(A_i) - 1)},$$

node transitional probability

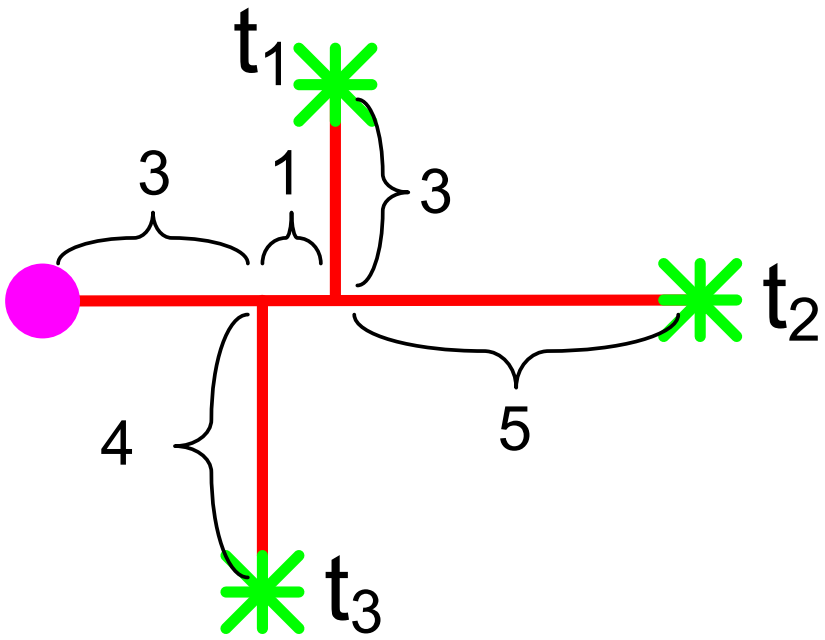
Transition Time



Transition Time Reduction



Clock Skew



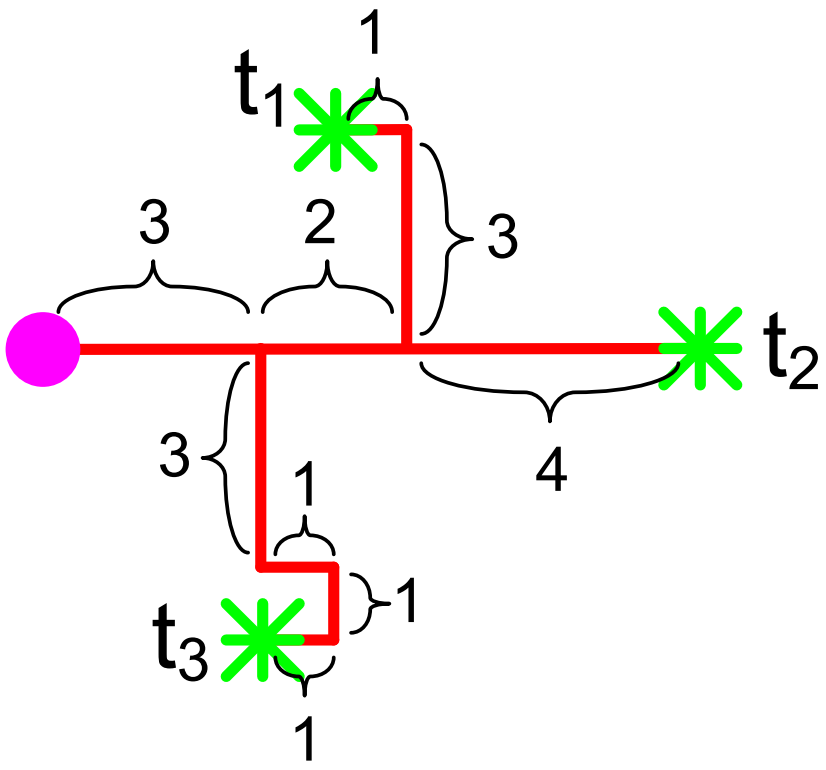
$$d_1 = 3+1+3 = 7$$

$$d_2 = 3+4 = 7$$

$$d_3 = 3+1+5 = 9$$

$$skew = \max\{d_1, d_2, d_3\} - \min\{d_1, d_2, d_3\} = 9 - 7 = 2$$

Clock Skew



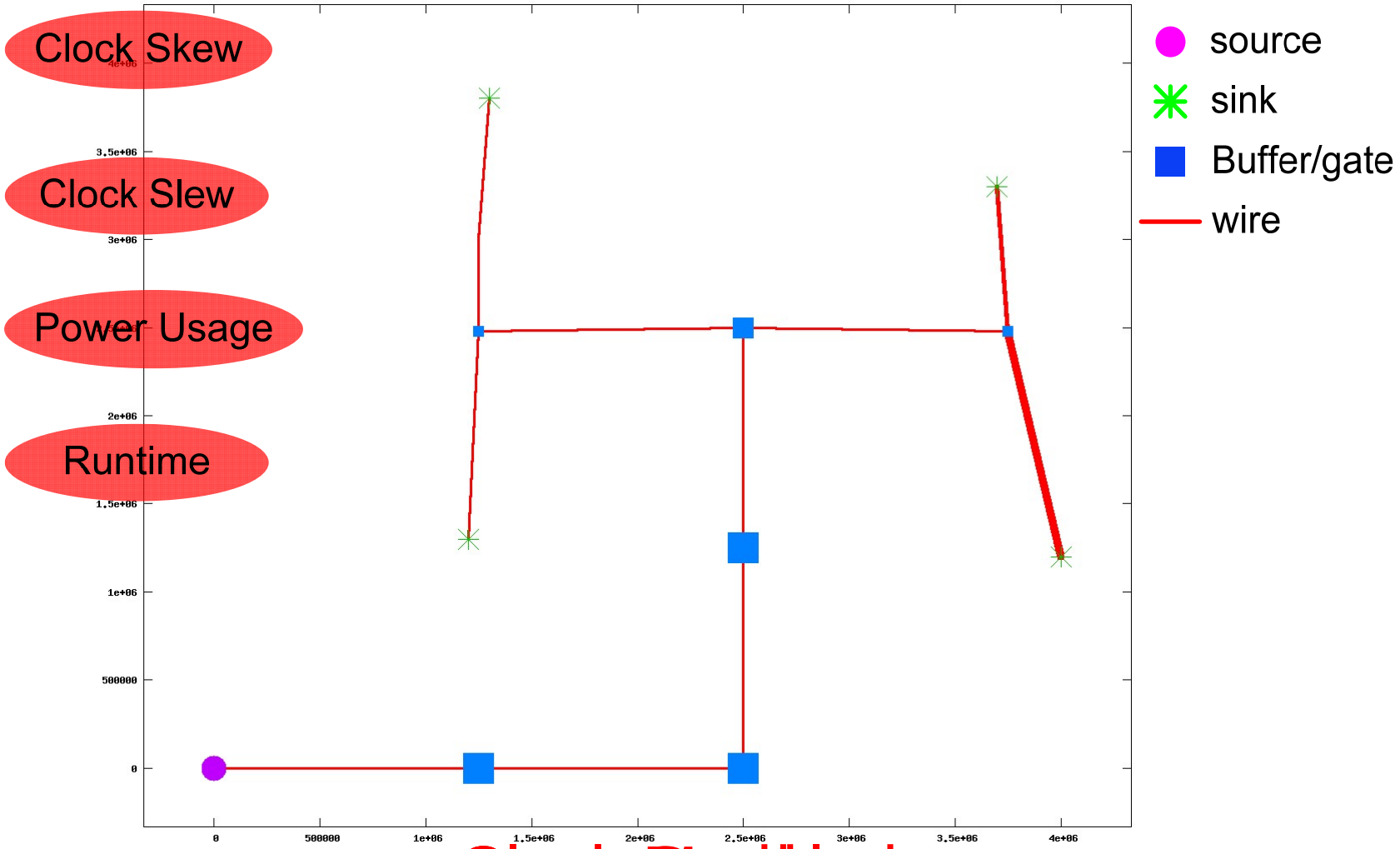
$$d_1 = 3+2+3+1 = 9$$

$$d_2 = 3+2+4 = 9$$

$$d_3 = 3+3+1+1+1 = 9$$

$$skew = \max\{d_1, d_2, d_3\} - \min\{d_1, d_2, d_3\} = 9 - 9 = 0$$

Problem Formulation



Clock Skew Synthesis

Overview of our Gating work

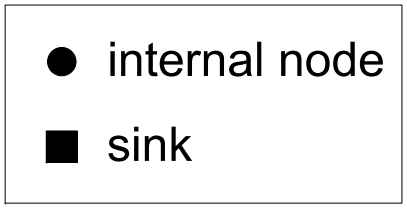
- Dual-MST based perfect matching with improved cost function
- Concurrent gate insertion concerning reduction of power consumption
- Balance the buffer and gate levels for reducing clock skew
- Constraint on slew rate is applied

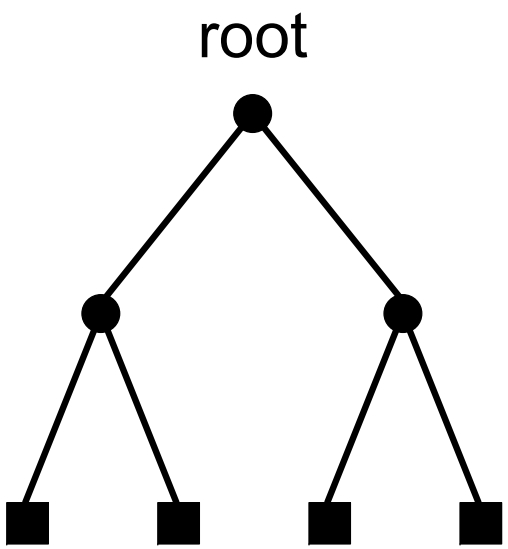
Construction of Clock Tree

- DMST
  - A dual-MST based Perfect Matching
  - Hierarchical Buffer Sizing
  - Iterative Buffer Insertion
  - Dual-MZ Blockage Handling
  - Elmore RC model [1] for delay computation

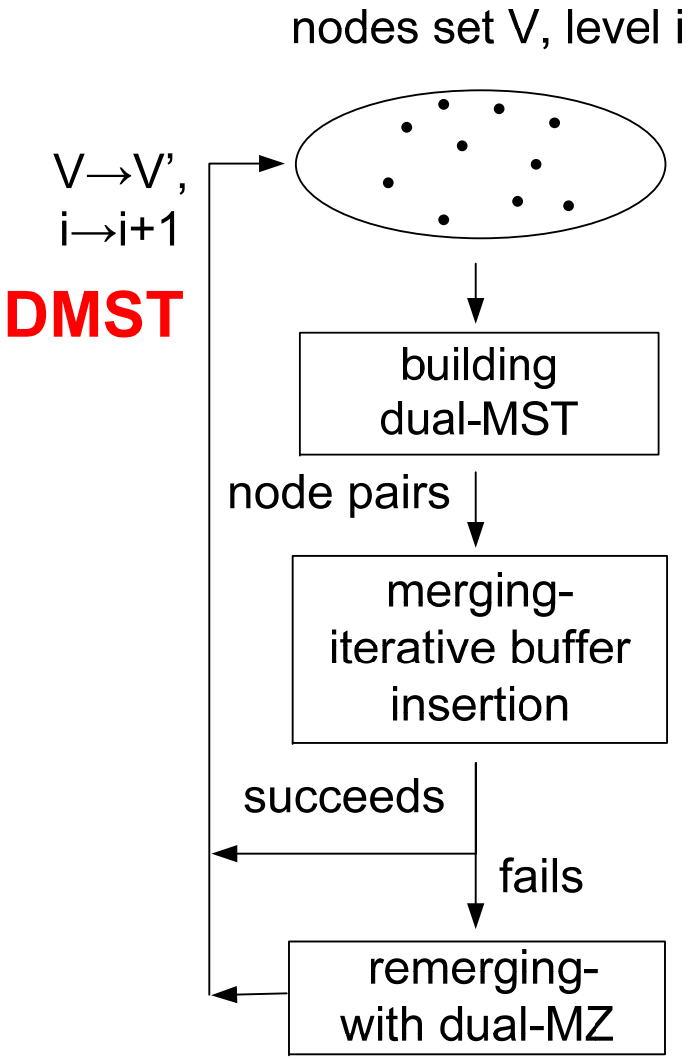
[1] W. C. Elmore. The Transient Response of Damped Linear Networks with Particular Regard to Wide Band Amplifiers. *Journal of Applied Physics*, 19(1):55 – 63, January, 1948.

Bottom-Up Procedure

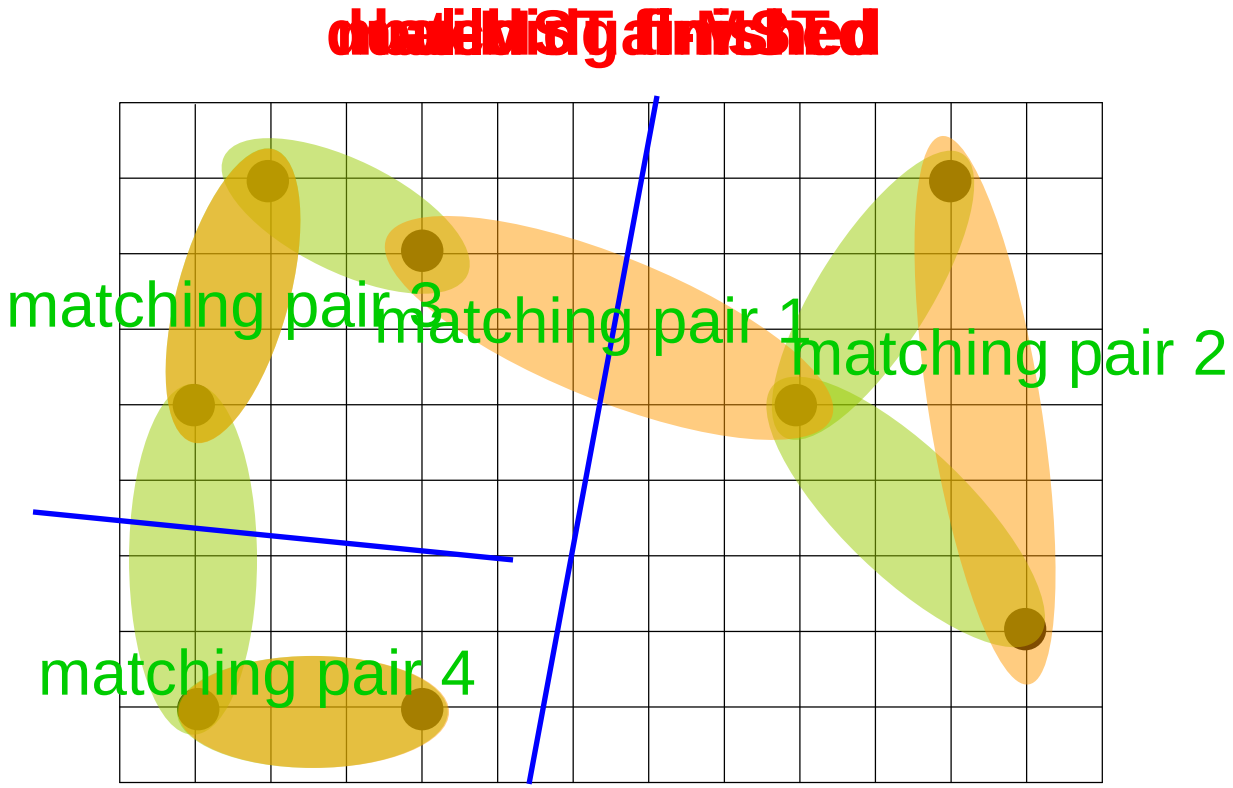




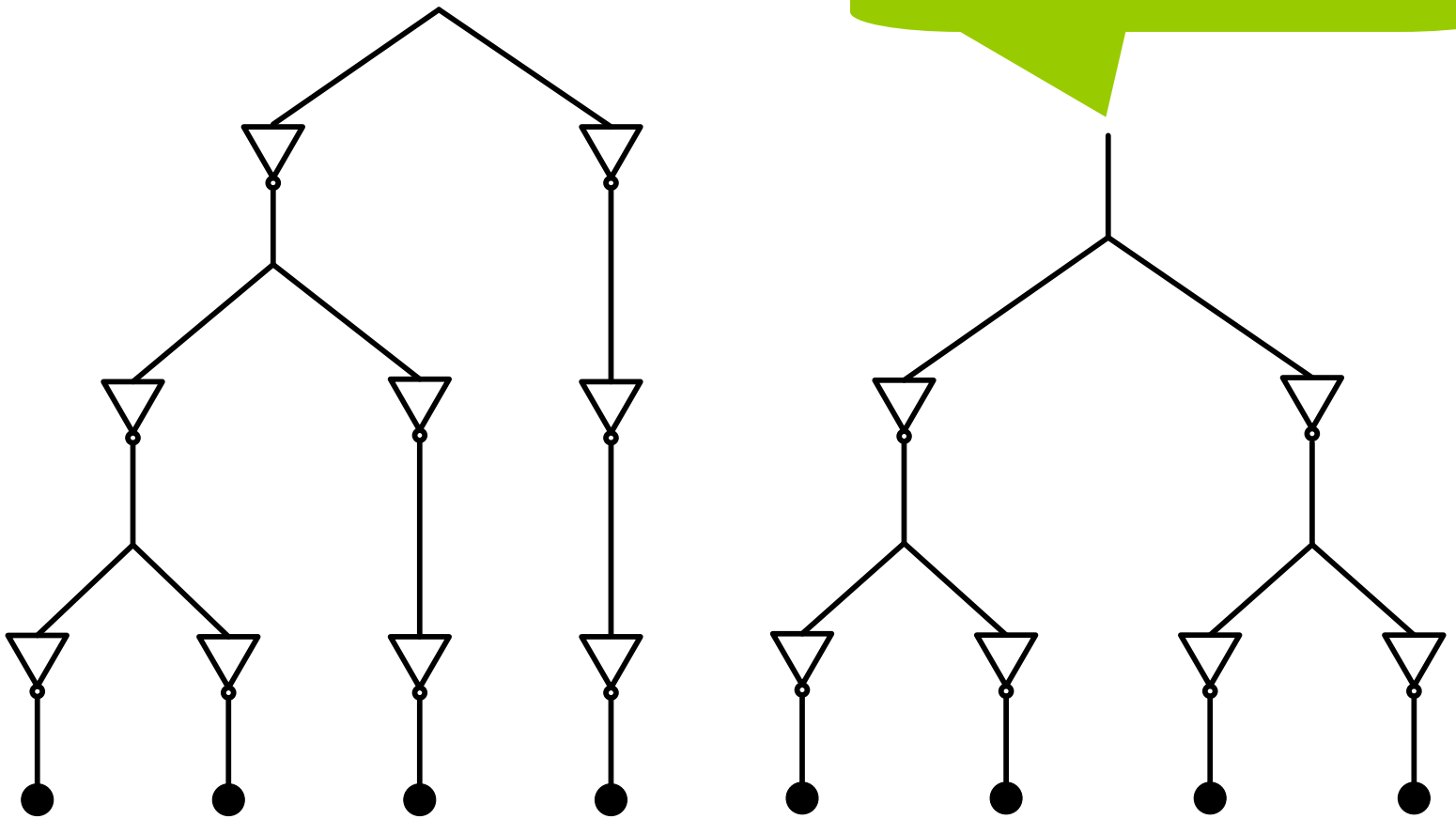
Overview of DMST



Dual-MST


matching pair 3
matching pair 1
matching pair 2
matching pair 4

Topology Comparison



Non-Perfect Matching

dual-MST

Cost Function

- Merging cost estimat
  - non-snaking $Pwr(v_a, v_b) = \rho_P \times D(v_a, v_b) \times P(A_i)$
  - snaking $Pwr(v_a, v_b) = \rho_P \times \frac{DLY(v_a, v_b)}{\rho_D} \times P(A_i)$
- Cost function for dual-MST matchin

unit power

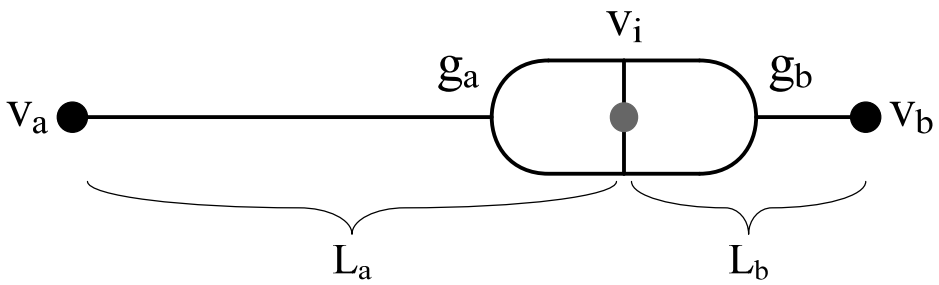
Manhattan distance

unit delay

delay difference

$$f_c(v_a, v_b) = \alpha \times D(v_a, v_b) + \beta \times Pwr(v_a, v_b)$$

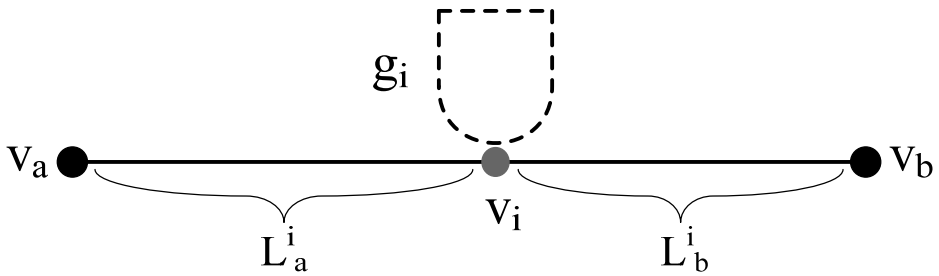
Determination on Gate Insertion



C_a^u : un-gated capacitance for clock tree at v_a

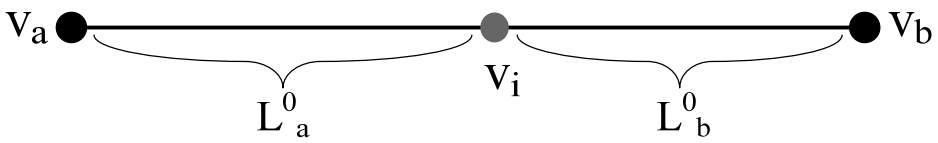
$C_{T_a^{ctr}}^u$: load capacitance for controller tree of v_a

$$SC_{tmp}(v_a, v_b) = \left(C_a^u + \rho_C \times L_a\right) \times P(A_a) + \left(C_b^u + \rho_C \times L_b\right) \times P(A_b) + C_{T_a^{ctr}}^u \times P_{tr}(A_a) + C_{T_b^{ctr}}^u \times P_{tr}(A_b)$$



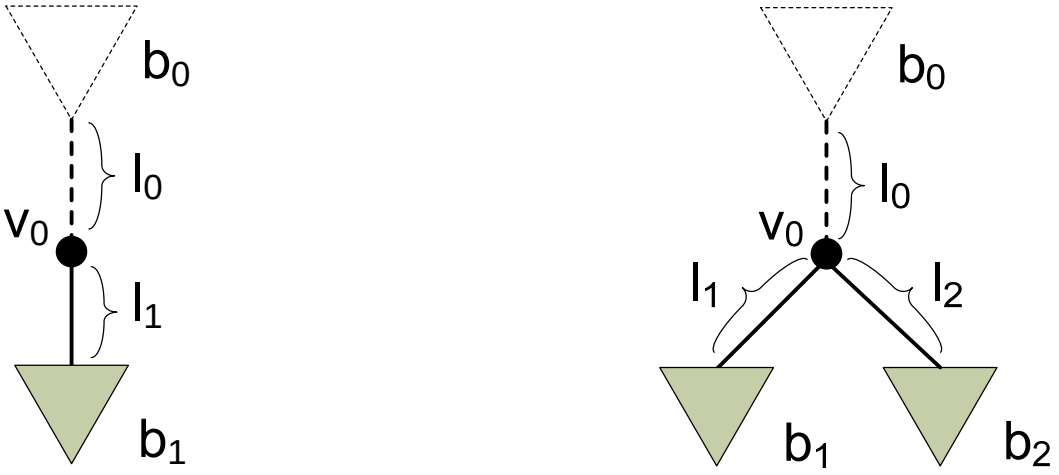
$$SC_{vir}(v_a, v_b) = \left(C_a^u + \rho_C \times L_a^i + C_b^u + \rho_C \times L_b^i\right) \times P(A_i) + C_{T_i^{ctr}}^u \times P_{tr}(A_i)$$

Gate Insertion Determination



$$SC_{non}\left(v_a, v_b\right) = C_a^u + \rho_C \times L_a^0 + C_b^u + \rho_C \times L_b^0$$

Slew Table Construction



Experimental Results

- Applied benchmark suite: ISPD2009 circuits [2]
  - Technology: 45nm model
  - Slew limitation: 100ps
- Metrics for comparison
  - SKEW (clock skew): ps
  - TC (total capacitance of the clock tree and the controller tree): fF
  - OSC (optimal switched capacitance): fF
  - SC (resulted switched capacitance): fF
  - CPU (program runtime): s

[2] C. N. Sze, P. Restle, G.-J. Nam and C. Alpert. ISPD2009 Clock Network Synthesis Contest. In *Proceedings of the International Symposium on Physical Design*, pages 149-150, 2009.

ISPD2009 Circuits Table

Circuits	Chip Size (mm x mm)	No. of Sinks	No. of Blockage (Area %)	CAP limit (fF)
ispd09f11	11.0 x 11.0	121	0 (0%)	118000
ispd09f12	8.1 x 12.6	117	0 (0%)	110000
ispd09f21	12.6 x 11.7	117	0 (0%)	125000
ispd09f22	11.7 x 4.9	91	0 (0%)	80000
ispd09f31	17.1 x 17.1	273	88 (24.38%)	250000
ispd09f32	17.0 x 17.0	190	99 (34.26%)	190000
ispd09f33	15.3 x 15.3	209	80 (27.68%)	195000
ispd09f34	16.0 x 16.0	157	99 (38.67%)	160000
ispd09f35	15.3 x 15.3	193	96 (33.22%)	185000
avg.	**12.1 x 11.6**	**203**	**169 (23.62%)**	**140273**

Experimental Results

Circuits	Our Approach (α=1,β=0)					Our Approach (α=2,β=1)				
	SKEW	TC	OSC	SC	CPU	SKEW	TC	OSC	SC	CPU
ispd09f11	20	103973	61868	78939	0.37	16.7	103851	61422	78261	0.37
ispd09f12	17.2	104874	65539	78970	0.34	16.6	103998	65090	79603	0.35
ispd09f21	20	118028	68813	89140	0.35	25.7	108116	67586	81043	0.35
ispd09f22	15.6	69810	43786	53173	0.32	8.5	69552	43938	53597	0.32
ispd09f31	33.7	221639	136596	179336	3.83	19.3	220522	128744	174024	5.6
ispd09f32	33.4	175122	101850	138156	0.51	21.7	162525	103658	123151	0.5
ispd09f33	20.6	171747	107773	139476	5.44	18.8	155995	100329	128386	6.3
ispd09f34	22.2	144688	92341	118570	0.49	20.3	139518	88924	109183	0.46
ispd09f35	16.9	165546	104232	134708	8.11	21.6	163376	102231	128963	8.13
avg.	**21.6**	125009	77527	**100852**	2.08	**20.6**	121118	76082	**96397**	2.26

Conclusion

- Dual-MST based perfect matching has been engaged
- A new cost function has been developed on power awareness
- Gate insertion technique has been improved to further optimize the performance
- Constraint on signal slew rate is satisfied so that our work can be more practical to be applied in real practice

Q & A

- Thank You