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Research Interests

Computer architecture including core microarchitecture design, transactional memory and memory hierarchy.

Program analysis for designing specialized co-processors.

Algorithmic optimizations for addressing system bottlenecks.

Education

University of California, San Diego: Fall 2004 – Present.
Ph.D. in Computer Science expected in Spring 2011.
M.S. in Computer Science in Spring 2006.
CGPA: 3.81/4.0

Indian Institute of Technology, Madras: Fall 2000 – Spring 2004.
B.Tech. in Computer Science and Engineering.
CGPA: 8.40/10.0

Research Projects

Arsenal Processors: Massively Heterogeneous Multiprocessors. The goal of the Arsenal processor design is to use massive heterogeneity to attack the system performance scaling issues caused by the power wall. To achieve this, the project automatically designed and implemented energy-efficient application-specific circuits, *Conservation Cores* (C-cores). The main challenge here was to ensure the longevity of c-cores by providing them with the capability to support future versions of their target applications via *patching* [1, 2]. To further improve the scalability of this approach of trading area for specialization, the follow-up work designed compound circuits, QASICs, that supported multiple general-purpose applications with similar data/control flow [3].

GreenDroid: A Highly Specialized Mobile Application Processor for Android. Designed GreenDroid mobile application processor, a multicore research prototype that targets the Android mobile software stack and can execute mobile programs with 11× less energy than today's designs [4, 5].

Hardware Support for Transactional Memory. Designed an efficient page-based approach for virtualizing transactional memory. The goal was to make both the transaction commit and abort operations fast and ensure graceful degradation of performance with the increase in the total transactional memory footprint [6].

Computation Reuse to Save Power in Network Processors. Designed a Computation Reuse Cache to reduce the energy consumption in Network Processors without compromising on the worst case throughput guarantees [7].

Partitioning of Large Circuits for Multi-FPGA Architecture. Developed an evolutionary technique to efficiently partition big circuits so that they can be implemented on a Multi-FPGA architecture [8].

Projects

Search engine for Distributed File System Designed and implemented a search engine for distributed file system. The main focus was on distributing the index storage among the nodes of the system efficiently without compromising on the "global correctness" of the search results.

Conference Tool, LoquaCT: Developed a tool for online conferencing. It was a decentralized scalable architecture. Also special care was taken to maintain consistent state at all times and to provide a graceful recovery in case of partial network failures.

Professional Experience

Intern at HP, Palo Alto: Summer 2006. Advisor: Dr. Norm Jouppi.
Worked in the area of transactional memory. The goal of the project was to compare the power efficiency of different transactional memory system implementations. The study also focussed on analyzing power consumption of the different components of a transactional memory system.

Intern at Intel, Santa Clara: Summer 2005. Advisor: Dr. Brad Chen.
Designed and implemented simulator for estimating the possible performance impact of resource contention on multiple independent applications running in parallel on a chip multiprocessor. The focus was mainly the second level shared cache in our experiments.

Intern at Fiorano Inc, New Delhi: Summer 2003.
Designed and implemented a JMS IN Adapter used for sending the data to a JMS destination server. It had support for message buffering and resending in case of network failures and connection to the destination server was re routed in case present one fails.

Publications

[1] Ganesh Venkatesh, Jack Sampson, Nathan Goulding, Saturnino Garcia, Vladyslav Bryskin, Jose Lugo-Martinez, Steve Swanson, and Michael Bedford Taylor. Conservation cores: Reducing the energy of mature computations. In *International Conference on Architectural Support for Programming Language and Operating Systems(ASPLOS)*, March 2010.

[2] Jack Sampson, Ganesh Venkatesh, Nathan Goulding, Saturnino Garcia, Steven Swanson, and Michael Bedford Taylor. Efficient complex operators for irreuglar code. In *International Symposium on High-Performance Computer Architecture (HPCA)*, February 2011.

[3] Ganesh Venkatesh, Jack Sampson, Nathan Goulding, Steven Swanson, and Michael Taylor. Quasi-asics: Trading area for energy by exploiting similarity in synthesized cores for irregular code. In *In Submission*.

[4] Nathan Goulding, Jack Sampson, Ganesh Venkatesh, Michael Bedford Taylor, and Steven Swanson. Greendroid: A mobile application processor for a future of dark silicon. In *Symposium for High Performance Chips(HotChips)*, August 2010.

[5] Nathan Goulding, Jack Sampson, Ganesh Venkatesh, Saturnino Garcia, Joe Auricchio, Po-Chao Huang, Manish Arora, Siddharth Nath, Jonathan Babb, Steven Swanson, and Michael Bedford Taylor. The greendroid mobile application processor: An architecture for silicon's dark future. In *To Appear in IEEE Micro*, March 2011.

[6] Weihaw Chuang, Satish Narayasamy, Ganesh Venkatesh, Jack Sampson, Michael Van Biesbrouck, Gilles Pokam, Osvaldo Colavin, and Brad Calder. Unbounded page-based transactional memory. In *International Conference on Architectural Support for Programming Language and Operating Systems(ASPLOS)*, October 2006.

[7] Bengu Li, Ganesh Venkatesh, Brad Calder, and Rajiv Gupta. Exploiting a computation reuse cache to reduce energy in network processors. In *High-Performance Embedded Architecture and Compilation(HiPEAC)*, November 2005.

[8] Pratibha P, Siva NageswaraRao Borra, A Muthukaruppan, S Suresh, Ganesh V, and V. Kamakoti. A parallel evolutionary approach to spatial partitioning in reconfigurable environments. In *Indian International Conference on Artificial Intelligence(IICAI)*, December 2003.

Talks Given

Exploiting a Computation Reuse Cache to Reduce Energy in Network Processors. *High-Performance Embedded Architecture and Compilation(HiPEAC)*, November 2005

A Parallel Evolutionary Approach to Spatial Partitioning in Reconfigurable Environments. *Indian International Conference on Artificial Intelligence (IICAI)*, December 2003

iRain: Data Water Cycle for Raining User with Information. *Wild and Crazy Ideas Session at ASPLOS (WACI)*, March 2010

Teaching Experience

University of California San Diego - Teaching Assistant
CS100 - Advanced Data Structures

Indian Institute Of Technology, Madras - Teaching Assistant
CS110 - Computational Engineering

References

Prof. Steve Swanson.
Website: `www.cse.ucsd.edu/users/swanson`
Email: swanson@cs.ucsd.edu

Prof. Michael B. Taylor.
Website: `www.cse.ucsd.edu/users/mbtaylor`
Email: mbtaylor@cs.ucsd.edu

Dr. Brad Calder.
Website: `www.cse.ucsd.edu/users/calder`
Email: bcalder@microsoft.com