Voltage Adaptation under Temperature Variation

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***Abstract*—The maximum delay of a processor is subject to both temperature (T) and voltage (V) *jointly*. Therefore, there is the prospect of reducing V at runtime whenever T is below the worst-case temperature without violating the predetermined timing constraints, instead of employing throughout a conservative V that corresponds to T_{worst}. Hence, the efficiency can be maximized, while still accounting for temperature variation at runtime, without sacrificing reliability. In this work, we focus on the key challenge of how the *small, yet sufficient voltage* can be accurately, at design time, obtained in which timing constraints at runtime are assuredly fulfilled. To achieve that, we model the delay of processor under the joint effects of T and V through creating cell libraries that contain the detailed delay information of cells at a wide variety of T and V cases. Libraries are compatible with commercial EDA tools. Hence, standard tool flows, even though they were not designed for that purpose, can be employed to seamlessly obtain the correlation between T and V in any circuit regardless its complexity. After modeling of the correlation between T and V from the physical level to circuit level, we implement at the system level a temperature-guided voltage adaptation technique that tunes the voltage at runtime following temperature variations leading to a considerable reduction in power.**

I. Introduction

Unsustainable temperatures, caused by high on-chip power densities [1], [2], have become one of the major obstacles that challenges designers in the current technology nodes. To overcome the effects of temperature increase on prolonging the circuit's delay, a timing guardband that corresponds to the worst-case temperature (T_{worst}), is typically employed on top of the critical path (CP) delay of circuit [3], [4]. This guarantees that the circuit will be always clocked at a sustainable frequency regardless temperature changes at runtime. Even though such an approach is safe, it is, in fact, inefficient as the temperature may, most of the operation time, stay below T_{worst} due to dynamics in running workloads. On the other hand, voltage has an opposite impact to temperature on delay (i.e. when V decreases, the circuit's delay increases). Hence, there is the prospect of reducing V at runtime whenever $T < T_{worst}$ without violating timing constraints. In this work, we introduce a novel technique that continuously tunes the voltage based on the operation temperature of processor. *It continuously eliminates any excess in voltage margin (i.e. avoiding wasted energy) following temperature dynamics at runtime towards maximizing the efficiency.* We call our technique *voltage adaptation* to differentiate it from conventional voltage scaling techniques (e.g., [5]) in which a controller predicts the performance requirement of the next task and accordingly scales V to save energy. Such techniques often necessitate having the maximum temperature that will be generated by the next task a prior, which might not be possible in some (e.g., real time) embedded systems.

Temperature and Voltage Correlation: When the temperature rises, lattice vibrations in silicon increase leading to increasing the probability of an electron being scattered [6]. Thus, the carrier mobility (μ), which is the drift velocity of a particle in an electric field, decreases. In turn, a lower μ leads to a lower I_{ON} in transistors [6] and hence larger delay (i.e. transistors become slower) [7], demonstrates. Therefore, a temperature increase results in increasing the CP's delay of circuit and vice versa. To ensure clocking the circuit with a sustainable frequency at runtime, a timing guardband needs to be typically included. Opposite to temperature, voltage has a contrary impact on transistor delay. When V decreases, the CP's delay becomes larger as the delay of its individual transistors increases. *Therefore, a delay improvement due to a temperature reduction can be equivalently translated into a lower voltage without violating timing constraints.*

The focus of this work is to accurately model the correlation between T and V with respect to the timing behavior of complex circuits like processors. This enables us to *adaptively* employ an equivalent voltage ($V_{adapted} < V_{nominal}$) whenever ($T_{operation} < T_{worst}$) in which the efficiency is maximized while timing constraints are still fulfilled. Reducing V results in less dynamic and leakage power. Therefore, energy and temperature can be optimized as well as reliability because reductions in T and V decelerate the underlying mechanisms of aging [8]. Note that the focus of our work is minimizing the efficiency loss akin to temperature guardband that inevitably required to overcome temperature variations at runtime. Other kinds for runtime variation like aging [9] are out of the scope and they necessitate their own guardbands to be employed.

II. Key Challenges in Modeling Temperature and Voltage Effects on Processor's Delay

Temperature and voltage effects originate from the physical level and then propagate all the way up to the system level where they finally cause timing violations. In the following we briefly summaries these effects:

(a) Physical and Transistor Levels: T and V dependencies in MOSFETs are very complex as they *differently* impact its key parameters like energy band gap, velocity saturation, carrier mobility, threshold voltage, leakage current, etc. [6]. A higher T reduces μ, but it concurrently reduces V_{th}, which has a contradictory impact compared to μ (i.e. it increases I_{ON}). Therefore, the overall impact of T and V changes on transistor delay inevitably necessitates employing physics-based modeling. To account for that, the industrial compact model of MOSFET BSIM [7] is typically employed as it accurately

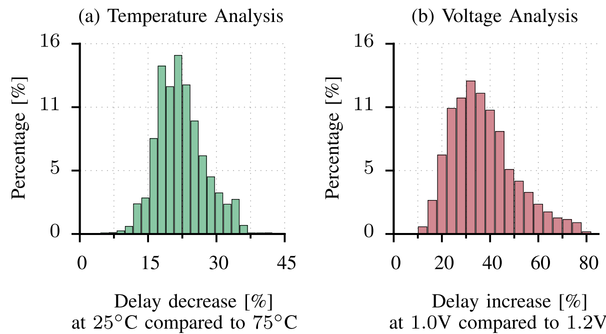

Fig. 1. The delay of gates within a standard cell library can be *non-uniformly* shifted under the same temperature (a) or voltage (b) change.

captures the effects that T and V have on all of the MOSFETs parameters along with the existing interdependencies.

(b) Gate Level: Even if the impact of T and V changes on pMOS/nMOS transistors is accurately estimated, the corresponding impact on the delay of gates will still be ambiguous because gates can be unevenly affected. Furthermore, the delay of the same gate itself may also be differently influenced based on the existing operating conditions ($OPCs$) in that gate (i.e. its input signal slews and output load capacitance). To demonstrate that, we analyze the impact of T reduction from 75°C to 25°C on the gates of a 45nm standard cell library [10]. As shown in Fig. 1(a), the same T reduction (i.e. 50°C) *non-uniformly* impacts the delay of gates. The delay improvement (i.e. decrease) can vary from merely 0.6% to 49%. Analogously, we also analyze the impact of V decrease from 1.2V to 1.0V. As shown in Fig. 1(b), the same V reduction of 200mV also *non-uniformly* impacts the delay of gates with a large variance between 2.5% and 81%.

(c) Circuit Level: Since the same change in T or V *non-uniformly* shifts the delay of gates, the prospect that the path which was formerly (i.e. before the T, V change) non-critical to become critical needs to indeed be considered.

In summary: Analyzing *accurately* the processor's delay under T and V effects, towards implementing a reliable temperature-guided voltage adaptation, is challenging as it necessitates involving all of the physical, transistor and circuit levels jointly. Considering the fact that the paths of a processor may switch their role w.r.t criticality necessitates, additionally, studying the entire processor's netlist. Hence, it is indispensable to perform the required timing analysis by means of existing commercial tool flows. Including their optimized and verified algorithms therein can effectively and correctly handle the large complexity in such sophisticated designs.

III. Our Temperature-Guided Voltage Adaptation

Our implementation of the proposed temperature-guided voltage adaptation consists of the following key steps:

- Creating cell libraries for the operational ranges of T, V.
- Measuring the processor's delay under T and V effects.
- Modeling the timing of processor correlating temperature reductions to the corresponding equivalent voltages.
- Implementing a runtime technique that adapts voltage based on the processor's temperature without violating timings.

Linking the physical and system levels: step 1 covers the physical, transistor and gate levels. Then, steps (2 and 3) cover the circuit level. Finally, step 4 covers the system level where our technique is implemented. Note that because our cell libraries created in step 1 are compatible with standard tool flows, we are able to employ in step 2 a commercial Static Timing Analysis tool (STA) in which its mature algorithms automatically handle the challenge of CP switching when T or V changes (details in Section II).

Cell Libraries Creation under T and V Effects: Similar to the presented steps in [4], [11], [12], which showed how degradation-aware cell libraries can be created to analyze degradation effects (e.g., aging and temperature), we create in the following cell libraries that consider T and V effects. We employ SPICE netlists of the combinational and sequential gates within the Nangate 45nm open-cell library [10]. Every netlist includes the parasitics information extracted from the gate's layout. The Predictive Technology Modeling (PTM) [13] for the high-performance 45nm technology together with the BSIM4 model [7] is employed. BSIM4 enables us to model the complex dependencies of MOSFET's parameters. Thus, the effects of T and V, at the physical and transistor levels, can be properly considered. Then, we employ the HSPICE circuit simulator to accurately measure the delay and power (leakage and dynamic) of every gate. To take the impact of $OPCs$ into account, we consider 7×7 input signal slews and output load capacitances. The measured 49 values of delay and power of each gate are then stored using the standard "*liberty*" format. This ensures that our libraries are compatible with existing commercial tool flows, e.g., Synopsys.

Based on the aforementioned process, we create a cell library for every 1°C for the range of $T \in [25, 85]$°C under the voltage of 1.2V. Likewise, we also create a cell library for every 10mV for the range of $V \in [0.9, 1.2]$V under the temperature of 25°C. As a result, we create 91 cell libraries. Both T and V ranges are typical for processors in the 45nm and the selected fine granularity provides us with a high certainty when we later analyze the processor's delay. Note that selecting a smaller T step would not be helpful as the accuracy of on-chip temperature sensors (which we later rely on to perform the online adaptation of V) is typically >1°C. Similarly, performing V adaptation at less than 10mV would also not be beneficial due to voltage fluctuation induced uncertainty. We select T_{worst} as 85°C, which is normal for commercial processors. Other T_{worst} can be easily considered.

IV. Modeling the Temperature-Voltage Correlation in Processors

To model the T-V correlation, we study four kinds of processors to take various architectures and complexities into account: The state-of-the-art industry-competitive out-of-order processor from Berkeley [14] and three processors (RISC with 5 and 6 pipelines and VLIW CPU) generated from the Synopsys Processor Designer tool. In the following, we take the BOOM CPU as an example and later summarize the analysis of others. First, we synthesize the RTL using the Synopsys Design Compiler based on the baseline library (1.2V, 25°C). Then, we estimate the maximum delay in the entire processor's netlist for the whole range of $T_{operation} \in [25, 85]$°C with

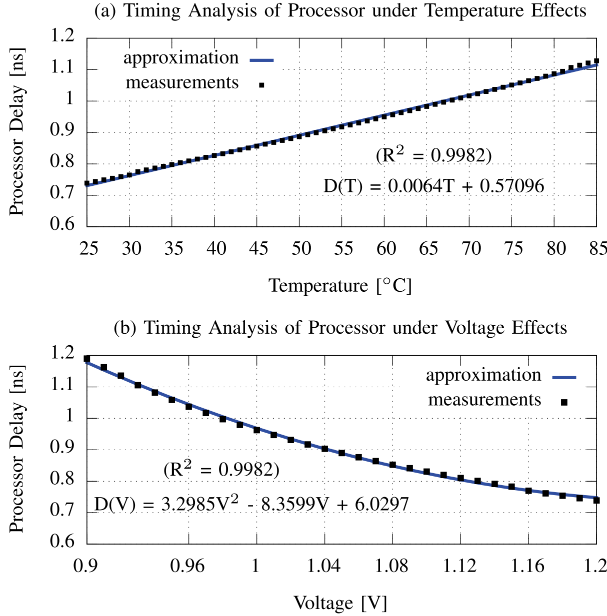

Fig. 2. Modeling the delay of BOOM processor under T and V effects.

a 1°C step using the Synopsys STA tool and our created libraries. Any switch in the CP due to T, V effects will be automatically captured by the STA tool. Based on the obtained data, we model the impact of T on the processor's delay $D(T)$. As Fig. 2 (a) shows, the linear approximation exhibits a good agreement with data. The average error is merely 0.42% and the root-mean-square error (RMSE) is 0.0048. Analogously, we perform timing analysis of processor's netlist for whole range of $V \in [0.9, 1.2]$V with a 10mV step to model the impact of V on the processor's delay $D(V)$. As shown in Fig. 2(b), a second-order polynomial approximation exhibits a good agreement with obtained data and the average error is 0.54% along with an RMSE of 0.0056. Finally, T variation ($\Delta T = T_{worst} - T_{operation}$) is correlated to the corresponding equivalent voltage as Eqs.(1, 2, 3) demonstrate. Fig. 3 shows $V_{adapted}$ for every $T_{operation}$. All curve's points result in a delay that does not violate the timing constraint (i.e., the processor's delay at $T_{worst} = 85$°C and $V_{nominal} = 1.2$V). Note that only the slope of T and V curves (see Fig. 2(a, b)) contribute in modeling the T-V correlation (see Eq. 2). Thus, the initial values (i.e. α_1 and β_2) are not important. The fitting parameters vary for different processors, as Table I summarizes (all errors are within 0.55%). Thus, the processor's architecture plays a role in how the T and V affect the maximum delay.

$$D(T) = \alpha_0 T + \alpha_1 \ , \ D(V) = \beta_0 V^2 + \beta_1 V + \beta_2 \qquad (1)$$

$$\Delta D(T) = D(T_{worst}) - D(T_{operation}) = \alpha_0 \Delta T > 0$$

$$\Delta D(V) = D(V_{nominal}) - D(V_{adapted}) < 0$$

$$\Delta D(V) = \beta_0(-\Delta V^2 + 2V\Delta V) + \beta_1 \Delta V = \Delta D(T) \Rightarrow$$

$$\Delta V = \frac{(2\beta_0 V + \beta_1) + \sqrt{(2\beta_0 V + \beta_1)^2 - 4\beta_0 \Delta D}}{2\beta_0} \ ; \ \beta_0 \neq 0$$

$$\Delta V = \frac{(2\beta_0 V + \beta_1) + \sqrt{(2\beta_0 V + \beta_1)^2 + 4\beta_0 \alpha_0 \Delta T}}{2\beta_0} \qquad (2)$$

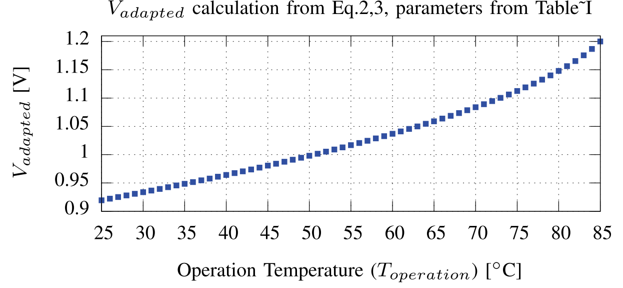

Fig. 3. The corresponding equivalent voltage for every operation temperature in which the timing constraint is not violated.

$$V_{adapted} = V_{nominal} - \Delta V \qquad (3)$$

V. Voltage Adaptation at Runtime using the T-V Correlation

Once the T-V correlation for the targeted processor is modeled at design time, a look-up table (LUT) that links each operation temperature with its corresponding equivalent voltage (see Fig. 3) can be built. Then, the LUT is employed at runtime to adapt the V based on current T. To achieve that, the processor's temperature is periodically read at every t_{read} from an on-chip sensor, which is often available in most of processor chips to provide the maximum T of processor at runtime. V adaptation can be rapidly performed as recent on-chip voltage regulators switches V within $< 1\mu$s like Intel on-the-fly regulators [15]. To sustain reliability, the V adaptation must take into account the maximum potential increase in T until the next sensor reading arrives based on its sampling rate. Otherwise, timing violations might occur due to applying a smaller V than what can be tolerated leading to unsustainable frequency. To this end, we add a safety margin (SM) on top of the read temperatures. The SM can be estimated at design time from analyzing the maximum possible T increase when the maximum power rise occurs. Such a SM means that the selected $V_{adapted}$ is always higher than what is actually needed. This additionally ensures that any small uncertainty in modeling (reported in Table I) will be compensated.

VI. Evaluation and Comparisons

State of the art (e.g., [16]) typically employs a ring oscillator (RO) as a sensor to predict the effects of T and V on delay. Therefore, we first evaluate whether such an approach could be alternatively used instead of creating cell libraries under T and V effects, as we propose. As demonstrated in Section II and Fig. 1, the same T, V change can *differently* impact the gates' delay. This brings up the critical question of "*how good is the RO in predicting the impact that T or V change actually*

TABLE I
Required parameters in Eq. 2 for different processors

Processor	α_0	β_0	β_1	$D(T)$ Err.	$D(V)$ Err.
BOOM	0.0064	3.2985	-8.3599	0.42%	0.54%
RISC-5P	0.0057	2.5167	-6.5215	0.36%	0.34%
RISC-6P	0.0065	3.1048	-7.9779	0.39%	0.39%
VLIW	0.0063	3.0396	-7.7905	0.39%	0.40%

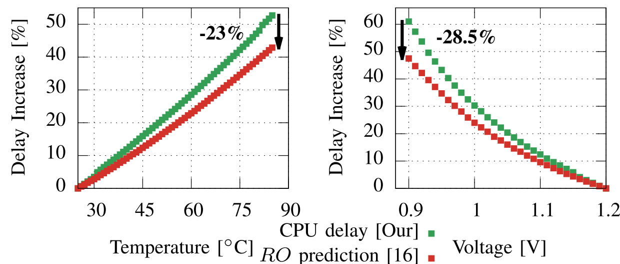

Fig. 4. Evaluating how accurate a RO-based approach in predicting the impact of temperature and voltage changes.

has on the processor's delay?". To investigate that, we study a typical RO of 15 stages [17]. We compare its predictions against the actual delay increase of the BOOM processor. The latter is accurately obtained by the Synopsys STA. As shown in Fig. 4, in both T and V scenarios there is a noticeable error in RO-based predictions reaching 23% and 28.5%, respectively. Such large errors demonstrate why one cannot rely on RO-based predictions to *reliably* perform temperature-guided voltage adaptation. The RO fails in representing how T and V affect the processor's delay because T and V *non-uniformly* impact the delays of gates (see Fig. 1).

To evaluate the effectiveness of our technique comapred to employing throughout a non-adaptive voltage, we build the following simulation toolchain: The cycle-accurate simulator gem5 [18] of an out-of-order processor extracts the activities of varied applications towards estimating the resulting temperature trace of each application using the Hotspot thermal simulator [19] together with the McPAT power simulator [20]. Afterwards, we integrate our technique proposed in Section V to perform the voltage adaptation based on the T-V correlation modeling. For a proper compatibility with the simulated architecture in gem5, we employ the BOOM processor in our evaluation since it is an out-of-order processor. In our implementation we consider $t_{read} = 1$ms and we select SM as 2°C to be added on top of the read temperature. The SM is obtained after analyzing the transient temperature traces of all studied applications to determine the maximum possible T increase within the selected t_{read} (i.e. max ΔT within 1ms). We employ diverse benchmarks from the PARSEC [21] and SPEC2006 [22] benchmark suites. Each benchmark is simulated on top of Linux kernel for realistic analysis.

The obtained results showed that our technique reduces the consumed power by 21%, on average, and up to 24%. This is because that it enables the processor to operate during the majority of operation time at lower voltages than the nominal (1.2V). On average, the applied $V_{adapted}$ is around 0.97V. Reductions in power directly lead to a lower power densities and thus less generated heat. On average, the temperature is reduced by 12% and up to 14%. Fig. 5 demonstrates the dynamics in T and $V_{adapted}$ for the "dedup" benchmark as an example. As shown, our technique reacts to the changes in temperature and accordingly adapts the voltage. This leads to employing lower V most of the time and thereby generating lower temperatures, compared to employing throughout a constant voltage of 1.2V. Note that reductions in T due to lower V may allow further reduction in V until T converges.

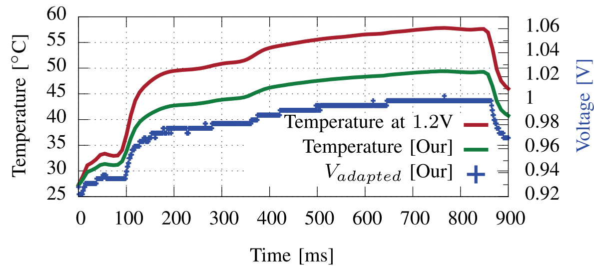

Fig. 5. Demonstration of the thermal behaviour of "dedup" benchmark when employing our temperature-guided voltage adaptation.

VII. Conclusion and Summary

In this work, we investigated how the effects of temperature and voltage on the delay of processor can be modeled towards implementing a temperature-guided voltage adaptation technique. The proposed technique adapts the voltage during the operation of processor in which the minimum, yet sufficient voltage is selected under the effects that temperature variation has, leading to a more efficient computing.

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