

Atieh Lotfi

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Education

Ph.D., Computer Science (Computer Engineering)

Department of Computer Science and Engineering, UC San Diego (GPA: 3.87/4)

San Diego, CA

Dec.2018

- Advisor: Professor Rajesh Gupta
- Thesis: Fault-susceptibility mitigation and efficient use of resources in programmable accelerators

M.Sc., Computer Engineering – Computer Architecture

School of Computer Science and Engineering, University of Tehran (GPA: 18.91/20)

Tehran, Iran

Aug. 2012

- Advisors: Professor Saeed Safari, Professor Zain Navabi
- Thesis: Efficient checkpointing techniques in multiprocessor architectures

B.Sc., Computer Engineering

School of Computer Science and Engineering, University of Tehran

Tehran, Iran

July 2008

- Advisors: Professor Saeed Safari, Professor Zain Navabi
- Project: Error resiliency of multimedia applications in the event of transient errors

Research and Work Experience

Senior Compute Architect NVIDIA *Jan 2019– Present*

GPU Architecture Intern NVIDIA *July 2017– Dec. 2017*

- GPU resiliency

Research Assistant UC San Diego *Sept. 2013–Dec 2018*

- Compiler-assisted hardware resource optimization for FPGA and GPU accelerators, Software level fault mitigation for GPU and FPGA accelerators, High-level synthesis, Approximate computing,

Research Assistant University of Tehran *Sept. 2009–Apr. 2013*

- Fault tolerant techniques for multicore architectures
- Distortion and complexity aware parameter tuning model for the H.264/AVC encoder
- Multi-level test package, Memory Testing, HDL-based Test Evaluation Tool Set

Publications

1. [Atieh Lotfi](#), Saurabh Hukerikar, Keshav Balasubramanian, Paul Racunas, Nirmal Saxena, Richard Bramley, Yanxiang Huang, “Resiliency of automotive detection networks on GPU architectures,” International Test Conference (ITC), Nov. 2019. (**Distinguished paper*)
2. Jeng-Hau Lin*, [Atieh Lotfi](#)*, Vahideh Akhlaghi, Zhuowen Tu, Rajesh K. Gupta, “Accelerating Local Binary Pattern Networks with Software Programmable FPGAs”, Design Automation and Test in Europe (DATE), 2019. (**Equal contributions*)
3. [Atieh Lotfi](#), Nirmal Saxena, Richard Bramley, Paul Racunas, Philip Shirvani, “Low Overhead Tag Error Mitigation for GPU Architectures,” *IEEE/IFIP International Conference on Dependable Systems and Networks (DSN)*, June 2018.
4. [Atieh Lotfi](#), Rajesh K. Gupta, “ReHLS: Resource-aware Program Transformation Workflow for High-level Synthesis,” *International conference on computer design (ICCD)*, Nov. 2017.
5. “Celerity: An Open-Source RISC-V Tiered Accelerator Fabric,” 29th ACM/IEEE Symposium on High-Performance Chips (*HOTCHIPS*), Aug. 2017.
6. [Atieh Lotfi](#), Rajesh K. Gupta, “RxRE: Throughput Optimization for High-Level Synthesis using Resource-Aware Regularity Extraction,”(poster) *FPGA’17*, Feb. 2017.
7. [Atieh Lotfi](#), Abbas Rahimi, Amir Yazdanbakhsh, Hadi Esmaeilzadeh, Rajesh K. Gupta, “GRATER: An Approximation Workflow for Exploiting Data-Level Parallelism in FPGA Acceleration,” Design Automation and Test in Europe (*DATE*), 2016.

8. Atieh Lotfi, Abbas Rahimi, Luca Benini, Rajesh K. Gupta, "Aging-Aware Compilation for GP-GPUs," ACM Transactions on Architecture and Code Optimization (*TACO*), vol. 12, issue 2, 2015.
9. Atieh Lotfi, Abbas Rahimi, Hadi Esmaeilzadeh, Rajesh K. Gupta, "SqueezeCL: Squeezing OpenCL Kernels for Approximate Computing on Contemporary GPUs," Approximate Computing Workshop, Oct. 2015.
10. Mehdi Semsarzadeh, Atieh Lotfi, Mahmoud Reza Hashemi, Shervin Shirmohammadi, "A fine-grain distortion and complexity aware parameter tuning model for the H.264/AVC encoder," Signal Processing: Image Communication, vol. 28, issue 5, pp. 441-457, 2013.
11. Atieh Lotfi, Arash Bayat, Saeed Safari, "Architectural Vulnerability Aware Checkpoint Placement in a Multicore Processor," *18th IEEE International On-Line Testing Symposium(IOLTS'12)*, Spain, June 2012.
12. Atieh Lotfi, Saeed Safari, "A Genetic-based Optimal Checkpoint Placement Strategy for Multicore Processors," *The 16th CSI International Symposium on Computer Architecture and Digital Systems*, 2012.
13. Atieh Lotfi, Parisa Kabiri, Zainalabedin Navabi, "Configurable Architecture for Memory BIST," *In Proc. Of 8th East West Design and Test International Symposium (EWDTS'11)*, Sep. 2011.

Book Contributions:

- "Digital System Test and Testable Design with HDLs", Z. Navabi, ISBN 978-1-4419-7547-8, Springer, January 2011, developed material and helped writing, Chapter 11 (Memory Testing).

Teaching Experience

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| Teaching Assistant CSE Department, UC San Diego, USA | Jan. 2017 - March 2017 |
| - <i>Advanced Microarchitectures - Accelerator for Machine Learning</i> | |
| Teaching Assistant CSE Department, UC San Diego, USA | Jan. 2015 - March 2015 |
| - <i>Computer Architecture Course</i> | |
| Lab Instructor ECE Department, University of Tehran, Iran | Sep. 2010 - Oct. 2012 (5 semesters) |
| - <i>Digital Logic Design Laboratory</i> | |
| Teaching Assistant ECE Department, Worcester Polytechnic Institute, USA | June. 2012 - Sep 2012 |
| - <i>Computer Architecture Course</i> | |
| Teaching Assistant ECE Department, University of Tehran, Iran | Sep. 2011 - Dec. 2011 (3 semesters) |
| - <i>Computer Architecture Course</i> | |

Technical Skills

Programming Languages: C/ C++, Python, CUDA, OpenCL

Hardware Description Languages: Verilog, VHDL

Technical Tools: Xilinx Vivado HLS, Altera SDK for OpenCL, Altera Quartus, ModelSim, Matlab

Compilers: LLVM Compiler Infrastructure

Computer Architecture Simulator and Emulators: SimpleScalar, Multi2sim

Honors and Awards

- Distinguished paper for ITC 2019 paper (Resiliency of automotive detection networks on GPU architectures)
- Travel grant for ICCD conference, 2017; Travel grant for CRA-Women Grad Cohort Workshop, 2015
- Fellowship Award, UCSD Department of Computer Science and Engineering, 2013-2014
- Ranked 3rd among MSc computer architecture students, 2012
- Ranked 4th/16,000 in the Iranian nationwide graduate entrance exam in Computer Engineering, 2009

Selected Graduate Coursework

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| - Advanced computer architecture | - Hardware security for embedded systems |
| - Advanced compilers | - Validation and prototyping of embedded systems |
| - Parallel computation | - Design of digital systems with HDLs |
| - Design and analysis of algorithms | - Database Systems |
| - Digital system testing and testable design | - Machine learning |
| - Fault tolerant computing | - Low-power VLSI design |