CSE 243 (Section Id: 339066)

VLSI Computer-Aided Design

Synthesis Methodologies in VLSI Design & Test

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As VLSI designs become increasingly large, ever increasing levels of Computer-Aided Design tools, starting from ever higher levels of specification abstraction are being used. While *logic synthesis* tools have already been established as an integral part of the VLSI Design flow, *high level synthesis* methodologies are making increasing inroads. The size and complexity of systems-on-a-chip, composed of embedded ASICs and processors, necessitates research in *hardware-software codesign* methodologies. This course will provide an introduction to the main synthesis methodologies in VLSI CAD, namely, *logic synthesis*, *high level synthesis* and *hardware-software codesign.* A brief introduction to classical physical design automation will be provided.

Additionally, the increasing size and complexity of VLSI chips is necessitating a solution to the highly costly problem of chip and system reliability. Ever higher levels of fault coverage are necessitated in VLSI designs, while the increasing penetration of electronic solutions in everyday life is necessitating higher levels of fault resilience. An introduction to the issues and fundamental approaches in *VLSI Test & Fault Tolerance* will be additionally provided in this course.

No textbook is required; all course material will be provided by the instructor. The following books are recommended:

- *Synthesis and Optimization of Digital Circuits*, by G. De Micheli, McGraw-Hill, 1994.
- *High-Level Synthesis: Introduction to Chip and System Design*, by D.D. Gajski, N. Dutt, A. Wu, and S. Lin, Kluwer Academic Publishers, 1992.
- *Specification and Design of Embedded Systems*, by D.D. Gajski, F. Vahid, S. Narayan, and J. Gong, Prentice-Hall, 1994.
- *Digital Systems Testing and Testable Design*, by M. Abramovici, M.A. Breuer and A.D. Friedman, IEEE Press, 1990.
- *Design and Analysis of Fault-Tolerant Digital Systems*, by B.W. Johnson, Addison-Wesley, 1987.

The course will meet twice a week on Tuesdays and Thursdays, 11:10 AM to 12:30 PM. The material will be covered in a manner to promote an understanding of the fundamentals of technology and algorithms used in VLSI CAD. A midterm and a final will be given. Students are additionally expected to complete a project, in an appropriate area of VLSI CAD, to be decided in consultation with the instructor.