

CSE 240A (Section Id: 995173)
Principles of Computer Architecture
MoWe 6:30 - 7:50 PM; EBU3B 2154

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Course Contents

Fundamentals of Computer Design Technology Trends. Power, Cost, Dependability. Measuring Performance. Quantitative Principles of Computer Design.

Instruction Set Principles Memory Addressing. Operands. Operations. Control Flow Instructions. Instruction Set Encoding.

Basic Pipeline Concepts Pipeline Hazards. Multicycle Operations in Pipelines. Interrupts, Precise Exceptions in Pipelines. Dynamically Scheduled Pipelines; Scoreboards.

Exploiting Instruction Level Parallelism Instruction Level Parallelism. Data, Control Dependences. Compiler Techniques for ILP. Loop Unrolling. Branch Prediction. Dynamic Scheduling. Dynamically Scheduled Pipelines; Tomasulo's Approach. Hardware-based Speculation. Multiple Issue Superscalar Processors. Advanced Instruction Delivery Techniques.

Limits on Instruction Level Parallelism Studies on Limitations of ILP. Multithreading.

Memory-Hierarchy Design Basics of Cache Performance. Reducing Cache Miss Penalty, Miss Rate, Hit Time.