Problem 1 – Petri Nets

Assume you have a Petri Net \( N \), with \( P \) places, \( T \) transitions and \( F \) flows:

\[ P = \{ P_1, P_2, P_3, P_4, P_5 \} \]
\[ T = \{ T_1, T_2, T_3, T_4 \} \]
\[ F = \{(P_1, T_1), (P_1, T_2), (P_2, T_2), (P_3, T_3), (P_4, T_3), (P_5, T_4), (T_1, P_3), (T_2, P_4), (T_3, P_5), (T_4, P_1), (T_4, P_2)\} \]

a) Assume an initial marking \( M_0 = [4, 3, 0, 0, 0] \).
   i) Is \( N \) pure?
   ii) What degree of liveness does \( N \) have?
   iii) Consider the markings \([0, 1, 1, 1, 1]\) and \([1, 0, 1, 1, 1]\). Are they reachable given the initial state? If the markings are reachable show them by simulating the Petri Net. If they are not reachable, show it by listing all the possible states and transitions.

b) Assume an initial marking \([4, 2, 0, 0, 0]\), we change the weight of \((T_4, P_1)\) from 1 to 2.
   i) List all the possible states and transitions for the given initial marking.
   ii) Is \( N \) pure?
   iii) What degree of liveness does \( N \) have?

Problem 2 – Synchronous Data Flow (SDF)

Given the following SDF graph with nodes A, B and C and edges a, b, c, d, e, f.

\[ \text{a)} \quad \text{Write the incidence matrix for the graph, with the columns corresponding to the nodes and the rows corresponding to the edges.} \]
\[ \text{b)} \quad \text{What values of } k_1 \text{ and } k_2 \text{ allow a PASS schedule?} \]
\[ \text{c)} \quad \text{Provide the PASS schedule such that A precedes B, which in turn precedes C.} \]
\[ \text{d)} \quad \text{In SDF graphs, each edge is associated with a buffer. For your PASS schedule in c), give the minimum size of each buffer.} \]
**Problem 3 – Esterel**

Draw the FSM that accurately represents the functionality of the following Esterel code:

```
module homework3:
    input S, A, E;
    output O;

    loop
        await S;
        abort
            present A else
            await A
        end;
    emit O when E
end
end module
```

**Problem 4 – Verilog**

Consider the following Verilog snippet and its corresponding circuit, at the moment of transition from 1 → 0 of the input to A. Notice that the assignments to a, b, and c are done in parallel.

```
input in1, in2;
output c;
...
initial begin:
    a <= ~in1;
    b <= ~(in1 ^ a);
    c <= a ^ b;
end;
```

![Circuit Diagram](image)

IN: 1 → 0

a) If there are no delta delays implemented, identify the two conflicting scenarios that can occur? Show them by labeling the sequence of transitions to A, B, and C (e.g. A: 0 → 1)

b) Assume a delta delay enforced for each gate. Does this remove ambiguity? If so, what is the new sequence of transitions?
Problem 5 – Petri Nets

Consider the Petri net defined by:

\[ P = \{ p_1, p_2, p_3 \} \]

\[ T = \{ t_1, t_2, t_3 \} \]

\[ A = \{ (p_1 t_1) (p_1 t_3) (p_2 t_1) (p_2 t_2) (p_3 t_3) (t_1 p_2) (t_1 p_3) (t_2 p_3) (t_3 p_1) (t_3 p_2) \} \]

With all weights being 1 except \( w(p_1 t_1) = 2 \)

a) Draw the Petri net

b) Let \( M_0 = [1 \ 0 \ 1] \). Show why transition \( t_1 \) can’t be enabled in any subsequent operations of the Petri net

c) Let \( M_0 = [2 \ 1 \ 1] \). What happens in the subsequent operations of the Petri net?