

# CSE140 - HW #5

Due Thursday March 3, 11:59PM

For the first two problems, we analyze the timing of sequential machines to practice the concept of clock period, skew and retiming. For the rest three problems, we practice the usage of standard interconnect components.

1. Given the circuit in Figure 1, each two-input XOR gate has a propagation delay of 60 ps and a contamination delay of 40 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q propagation delay of 70 ps, and a clock-to-Q contamination delay of 50 ps.

- (a) If there is no clock skew, what is the maximum operating frequency of the circuit?
- (b) How much clock skew can the circuit tolerate before it might experience a hold time violation?

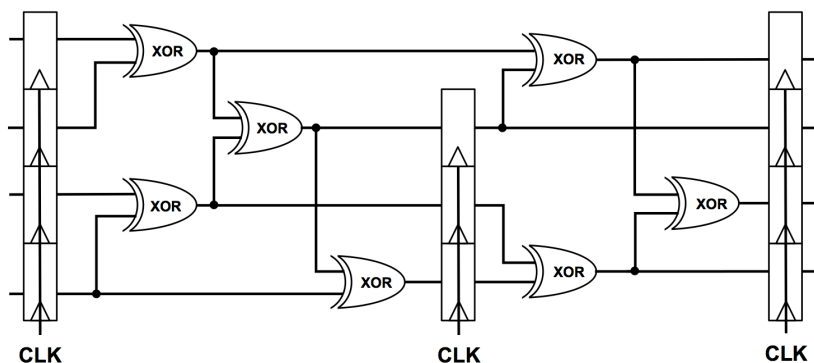


Figure 1: a sequential circuit with 11 Flip-Flops and 7 XOR gates

2. A four-bit addition machine is built with four full adders such that the carry out of the first adder is the carry in to the second adder, and the carry out of the second is the carry in to the third, and so on as shown in Figure 2. The machine has input and output registers and must complete the addition in one clock cycle. Each full adder has the following propagation delays: 20 ps from  $C_{in}$  to  $C_{out}$  or to  $Sum(S)$ , 25 ps from  $A$  or  $B$  to  $C_{out}$ , and 30 ps from  $A$  or  $B$  to  $S$ . The adder has a contamination delay of 15 ps from  $C_{in}$  to either output and 22 ps from  $A$  or  $B$  to either output. Each flip-flop has a setup time of 30 ps, a hold time of 10 ps, a clock-to-Q propagation delay of 35 ps, and a clock-to-Q contamination delay of 25 ps.

- (a) If there is no clock skew, what is the maximum operating frequency of the circuit?

(b) If there is retiming using designated skew, what is the maximum operating frequency of the circuit?

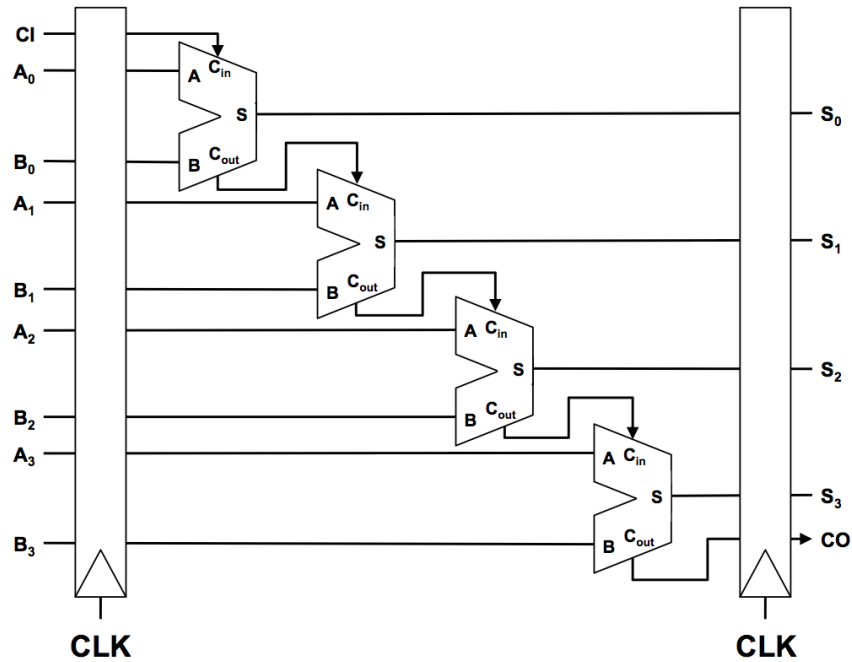


Figure 2: A four-bit addition machine.

3. (Decoders) Given three four-input Boolean functions

$$f_1(a, b, c, d) = \sum m(1, 2, 3, 10, 12) + \sum d(5, 8),$$

$$f_2(a, b, c, d) = \sum m(0, 3, 6, 15) + \sum d(2, 10),$$

$$f_3(a, b, c, d) = \sum m(2, 8, 9, 14) + \sum d(11, 12, 13).$$

- 3.1. Implement the functions using a minimal network of 4:16 decoders and OR gates.
- 3.2. Implement the functions using a minimal network of 3:8 decoders and OR gates.
- 3.3. Implement the functions using a minimal network of 2:4 decoders and OR gates.

4. (Multiplexers) Assume a dual-railed system, where you have access to any variable and its complement. Implement the following four-input Boolean function as indicated in each of the following subproblems.

$$f(a, b, c, d) = \sum m(3, 4, 7, 10, 14, 15) + \sum d(0, 1, 6, 8, 13).$$

- 4.1. Implement the function using a minimal network of 8:1 multiplexers.
- 4.2. Implement the function using a minimal network of 4:1 multiplexers.
- 4.3. Implement the function using a minimal network of 2:1 multiplexers.

5. Assume a dual-railed system, where you have access to any variable and its complement. Given a four-input Boolean function

$$f(a, b, c, d) = \sum m(1, 3, 4, 5, 7, 9, 13) + \sum d(10, 15).$$

- 5.1. Implement the function using a minimal network of 2:4 decoders and OR gates.

- 5.2. Implement the function using a minimal network of 4:1 multiplexers.
- 5.3. Implement the function using a minimal network of 2:1 multiplexers.