CSE140 - HW #3

Due Thurday February 4, 11:59PM

1 Introduction

The purpose of this assignment is to get a better understanding of universal gates and basic memory elements of sequential circuits. For the first problem, we clarify the concept of universal set. For the second problem, we practice the operations of exclusive gates. In the last problem, we learn to analyze circuits with feedback loops.

2 Universal Gates

Check if the set of gates or functions in the following list are universal. Justify your answer. Assume that constants 0 and 1 are available as inputs.

1. {XOR, NOT}
2. {NAND, NOT}
3. {XNOR} (Exclusive NOR gate)
4. $\{f(a,b)\}$, where $f(a,b) = a' + b'$.
5. $\{f(a,b,c)\}$, where $f(a,b,c) = (a+b)(b+c)(a'+b'+c')$.
6. $\{f(a,b,c)\}$, where $f(a,b,c) = ab + ac + bc$.

3 Other types of gates

I. Simplify the expression in a minimal sum of products form.

1. $f(a, b) = a \oplus (a + b') \oplus ab \oplus a'b$.
2. $f(a, b, c) = abc \oplus (a + b' + c) \oplus (b + c)b \oplus a'b \oplus (b + c')$.

II. Prove or disprove the following equalities.

1. $a \oplus bc = (a \oplus b)(a \oplus c)$.
2. $a(b \oplus c) = ab \oplus ac$.

4 Latch

I. Given a SR latch of 2 NOR gates (slide 12 of Lecture Note 7: Sequential Network), replace the NOR gate on top with a NAND gate. Analyze the revised circuit.
1. Write the truth table at times t_1, t_2 and t_3 as the table in slide 20.
2. Draw the state diagram.
3. Describe the state table and characteristic expression.

II. Repeat Problem I. However, replace the two NOR gates of the SR latch with two NAND gates.