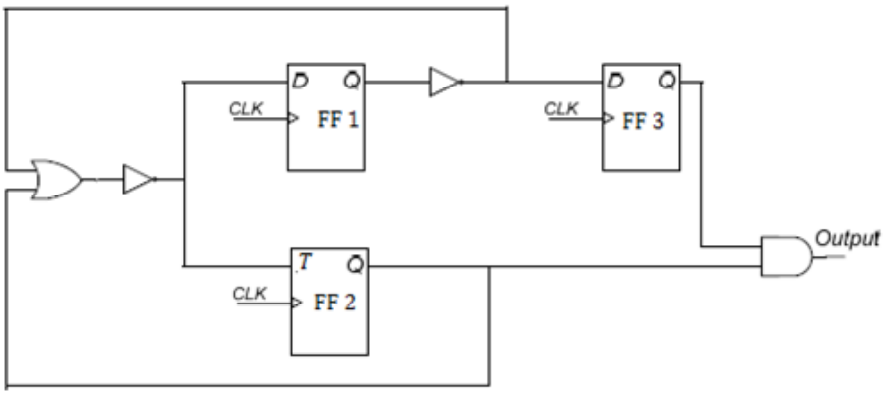
**CSE140 Exercise, No due date**

(I) (Timing and Retiming) For the following circuit, the timing characteristics of the components are summarized below.

- Flip-flop: clock-to-Q maximum delay $t_{pcq} = 40$ps, clock-to-Q minimum delay $t_{ccq} = 30$ps, setup time $t_{setup} = 50$ps, hold time $t_{hold} = 60$ps
- Logic gate (each AND, OR, Inverter): propagation delay $t_{pd} = 35$ps, contamination delay $t_{cd} = 25$ps.




I.1. Suppose that there is no clock skew. What is the maximum clock frequency of this circuit?
I.2. How much clock skew can the circuit tolerate before it might experience a hold time violation?
(II) (Decoders) Given three four-input Boolean functions
$f_1(a,b,c,d) = \sum m(1,2,4,7) + \sum d(3)$, $f_2(a,b,c,d) = \sum m(0,3,14) + \sum d(15)$, $f_3(a,b,c,d) = \sum m(12,15)$.
II.1. Implement the functions using a minimal network of 4:16 decoders and OR gates.
II.2. Implement the functions using a minimal network of 3:8 decoders and OR gates.
II.3. Implement the functions using a minimal network of 2:4 decoders and OR gates.
(III) (Multiplexers) Given a three-input Boolean function
$f(a,b,c) = \sum m(0,3,5,7) + \sum d(6)$,
implement the function using a minimal network of 2:1 multiplexers. Describe the design with a logic diagram.

(IV). (System Designs) Implement the following algorithm:

Alg(X,Y,Z,start,U,done);
Input X[7:0], Y[7:0], start;
Output U[7:0], done;
Local-object A[7:0], B[7:0], C[7:0];
S1: If start' goto S1;
S2: A $\Leftarrow$ X $\|$ B $\Leftarrow$ Y $\|$ C $\Leftarrow$ (00000000) $\|$ done $\Leftarrow$ 0;
S3: A $\Leftarrow$ Add(A, B) $\|$ C $\Leftarrow$ Inc(C);
S4: If A'[7] goto S3;
S5: U $\Leftarrow$ C $\|$ done $\Leftarrow$ 1 $\|$ goto S1;
End Alg

IV.1. Design a data subsystem that is adequate to execute the algorithm.
IV.1.1. Use a table to list the instructions and corresponding components for data path subsystem.
IV.1.2. Draw the schematic diagram to show the data path subsystem. Label the inputs, outputs, and control signals of all components.
IV.2. Design the control subsystem.
IV.2.1. Use a table to list the value of control signals for every state.
IV.2.2. Draw the state diagram.
IV.2.3. Implement the control subsystem with a one hot encoding design. Draw the logic diagram.