CSE140 Midterm2 Solutions

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1. Universal Set of Gates:

1.1. Define a universal set of gates (8 points).

A set of gates that can used to implement any switching function.

or

A set of gates that can used to derive AND, OR, NOT.

1.2. Check if the set in the following list is universal and explain your decision. Assuming constants 0 and 1 are available as inputs (12 points).

1.2.1. {AND, OR}

NOT UNIVERSAL

Cannot implement NOT

1.2.2. {AND, NOT}

UNIVERSAL

We can derive OR using DeMorgan's rule $a + b = \overline{\overline{a + b}} = \overline{\overline{a}.\overline{b}}$

1.2.3. {f(x,y)}, where f(x,y)= x+y'

UNIVERSAL

To get NOT $\rightarrow$ Set $x = 0$

To get OR $\rightarrow$ Invert second input before feeding it to $f(x, y)$ OR $f(x, y')$

To get AND $\rightarrow$ Use DeMorgan's law

1.2.4. {f(x,y,z)}, where f(x,y,z)= (xy+z)(x'y'+z')

UNIVERSAL

To get NOT $\rightarrow$ Set $x = 0, y = 1$ *i.e.,* $f(0, y, 1) = y'$

To get AND $\rightarrow$ Set $z = 0$ *i.e.,* $f(x, y, 0) = (xy + 0)(x'y' + 1) = x.y$

To get OR $\rightarrow$ Use DeMorgan's law (similar to part 2)

2. Other Types of Gates: Consider the function f(x,y) where $\oplus$ is an Exclusive OR operator:

f(x,y)= (xy) $\oplus$ (x' + y) $\oplus$ (x+ y') $\oplus$ (xy') $\oplus$ x' + y')

2.1) Evaluate $f(1, y)$ and $f(0, y)$. (6 points)

(a)
$$\begin{aligned} f(1,y) &= y \oplus y \oplus 1 \oplus y' \oplus y' \\ &= 0 \oplus 1 \oplus y' \oplus y' \\ &= 1 \oplus y' \oplus y' \\ &= y \oplus y' \\ &= 1 \end{aligned}$$

(b)
$$\begin{aligned} f(0,y) &= 0 \oplus 1 \oplus y' \oplus 0 \oplus 1 \\ &= 1 \oplus y' \oplus 0 \oplus 1 \\ &= y \oplus 0 \oplus 1 \\ &= y \oplus 1 \\ &= y' \end{aligned}$$

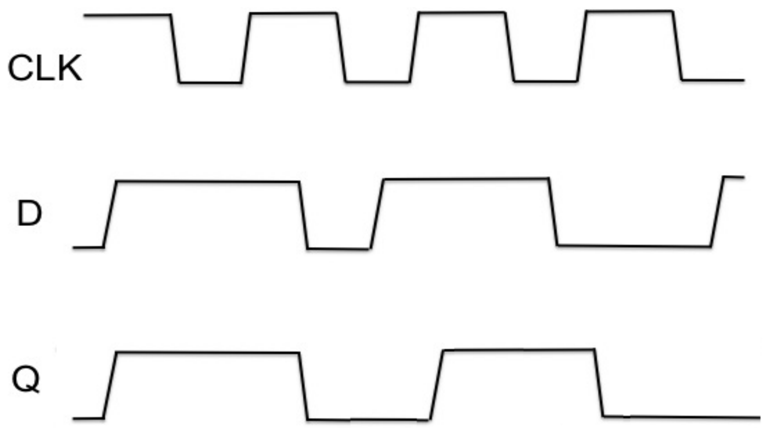
2.2) Simplifyf(x,y) to minimal sum of products expression, No restriction on the method. However, you must explain your approach. (15 points).

Possible ways - {Shannon's, Truth table, Boolean Algebra}

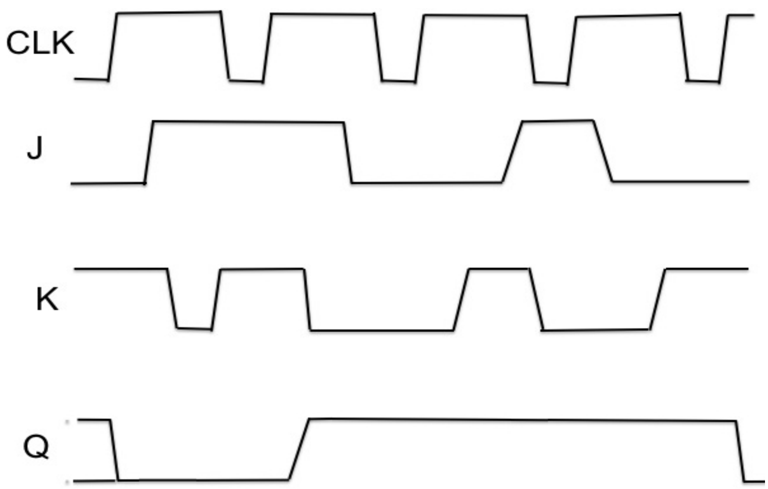
If Shannon's expansion was used -

$$\begin{aligned} f(x,y) &= x' f(0,y) + x f(1,y) \\ &= x'y' + x1 \\ &= x'y' + x \\ &= (x + x')(x + y') \quad \text{[Distributive Law]} \\ &= x + y' \end{aligned}$$

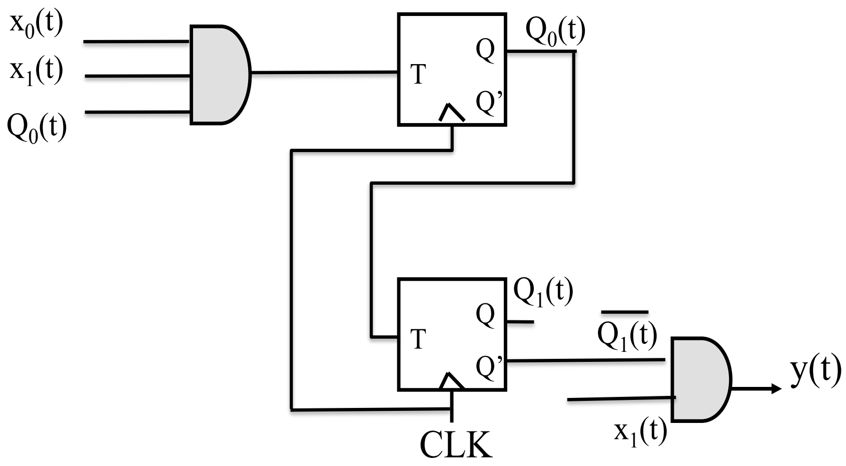
3. Timing Diagram of Latch and Flip-Flop:
3.1 Given the input waveforms shown below, sketch the output, Q, of a D latch (10 points).



3.2 Given the input waveforms shown below, sketch the output, Q, of a JK flip-flop. The flip flop is triggered at the rising edge of the clock. (10 points).



4. (Finite State Machine Specification) Consider the following circuit.



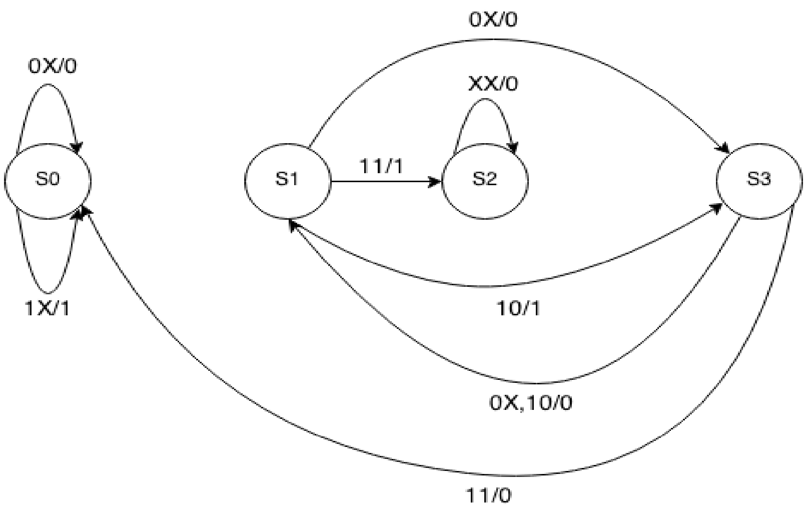
4.1 Write the state transition table (8 points).

$x_1(t)$	$x_0(t)$	$Q_1(t)$	$Q_0(t)$	$T_1(t)$	$T_0(t)$	$Q_1(t+1)$	$Q_0(t+1)$	$y(t)$	$S(t)$	$S(t+1)$
0	0	0	0	0	0	0	0	0	S_0	S_0
0	0	0	1	1	0	1	1	0	S_1	S_3
0	0	1	0	0	0	1	0	0	S_2	S_2
0	0	1	1	1	0	0	1	0	S_3	S_1
0	1	0	0	0	0	0	0	0	S_0	S_0
0	1	0	1	1	0	1	1	0	S_1	S_3
0	1	1	0	0	0	1	0	0	S_2	S_2
0	1	1	1	1	0	0	1	0	S_3	S_1
1	0	0	0	0	0	0	0	1	S_0	S_0
1	0	0	1	1	0	1	1	1	S_1	S_3
1	0	1	0	0	0	1	0	0	S_2	S_2
1	0	1	1	1	0	0	1	0	S_3	S_1
1	1	0	0	0	0	0	0	1	S_0	S_0
1	1	0	1	1	1	1	0	1	S_1	S_2
1	1	1	0	0	0	1	0	0	S_2	S_2
1	1	1	1	1	1	0	0	0	S_3	S_0

<u>State Assignment:</u>

$S_0 = 00, S_1 = 01, S_2 = 10, S_3 = 11$

4.2 Sketch the state diagram (7 points).



4.3 Is the circuit a Moore or a Mealy machine? (5 points).

It's a mealy !

5. A state machine has one input $x(t)$ and two-bit state $(Q_1(t), Q_0(t))$. The machine is described by the following state equations.

$Q_1(t+1) \;=\; Q_1'(t) + \; x'(t)Q_0(t),$

$Q_0(t+1) \;=\; x'(t)Q_1'(t) \; + \; x'(t)Q_0'(t).$

(i). Write the state transition table and draw state diagram (10 points).

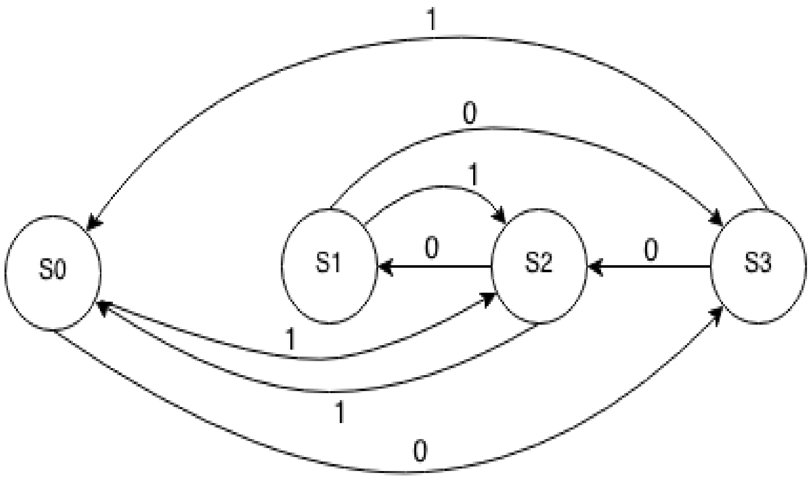
State Transition Table:

id	$x(t)$	$Q_1(t)$	$Q_0(t)$	$Q_1(t+1)$	$Q_0(t+1)$	$s(t)$	$s(t+1)$
0	0	0	0	1	1	S_0	S_3
1	0	0	1	1	1	S_1	S_3
2	0	1	0	0	1	S_2	S_1
3	0	1	1	1	0	S_3	S_2
4	1	0	0	1	0	S_0	S_2
5	1	0	1	1	0	S_1	S_2
6	1	1	0	0	0	S_2	S_0
7	1	1	1	0	0	S_3	S_0

State Assignment:

$S_0 = 00, S_1 = 01, S_2 = 10, S_3 = 11$

State Diagram:



(ii). Use two JK flip-flops and a minimal AND-OR-NOT network to implement the machine. Show your derivation (K maps) and draw the logic diagram (15 points).

Excitation Table:

id	$x(t)$	$Q_1(t)$	$Q_0(t)$	$J_0(t)\ K_0(t)$	$J_1(t)\ K_1(t)$	$Q_1(t+1)$	$Q_0(t+1)$
0	0	0	0	$1\ X$	$1\ X$	1	1
1	0	0	1	$X\ 0$	$1\ X$	1	1
2	0	1	0	$1\ X$	$X\ 1$	0	1
3	0	1	1	$X\ 1$	$X\ 0$	1	0
4	1	0	0	$0\ X$	$1\ X$	1	0
5	1	0	1	$X\ 1$	$1\ X$	1	0
6	1	1	0	$0\ X$	$X\ 1$	0	0
7	1	1	1	$X\ 1$	$X\ 1$	0	0

K-Maps:

$J_0(t) \quad = \quad x'(t)$

$x(t)$ \ $Q_1(t), Q_0(t)$	00	01	11	10
0	1	X	X	1
1	0	X	X	0

$K_0(t) \quad = \quad Q_1(t) \quad + \quad x(t)$

$x(t)$ \ $Q_1(t), Q_0(t)$	00	01	11	10
0	X	0	1	X
1	X	1	1	X

$J_1(t) \quad = \quad 1$

$x(t)$ \ $Q_1(t), Q_0(t)$	00	01	11	10
0	1	1	X	X
1	1	1	X	X

$K_1(t) \quad = \quad x(t) \quad + \quad Q_0'(t)$

$x(t)$ \ $Q_1(t), Q_0(t)$	00	01	11	10
0	X	X	0	1
1	X	X	1	1

Logic Diagram: