Discussion

Mrinmayee Hingolikar

Outline

- Midterm 2 Solutions
- Timing Review

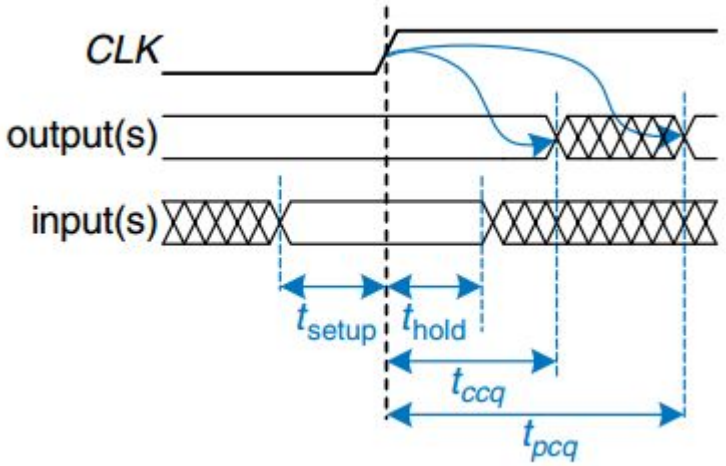
Timing constraints

A sequential element has an *aperture time* around the clock edge, during which input must be stable for the flip-flop to produce a well-defined output.

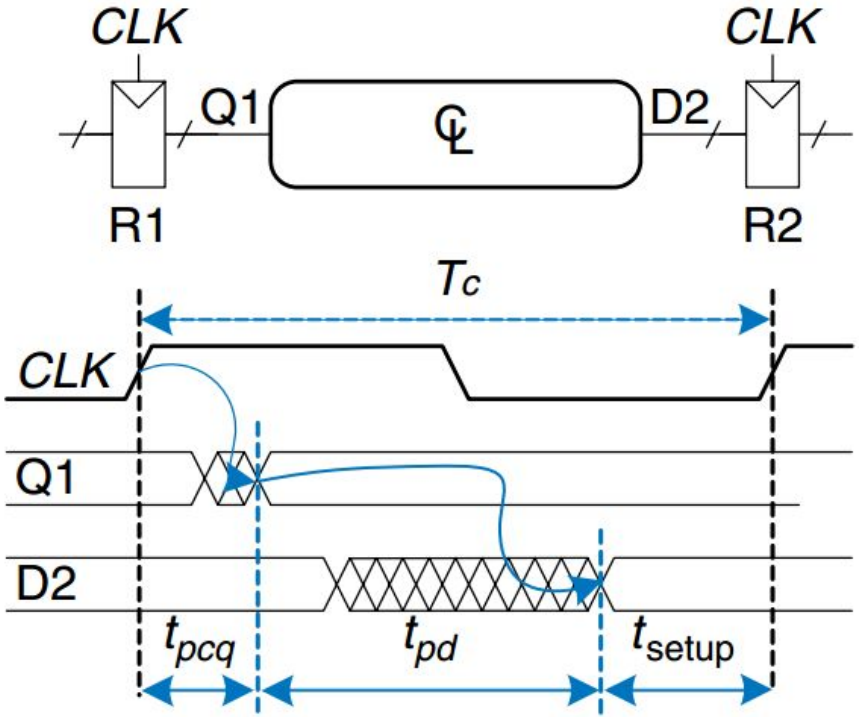
The aperture is defined by a *setup time* (t_{setup}) and *hold time* (t_{hold}), before and after the clock edge respectively.

Output may start to change after *contamination delay* (t_{ccq})

Output must settle to the final value within *propagation delay* (t_{pcq})

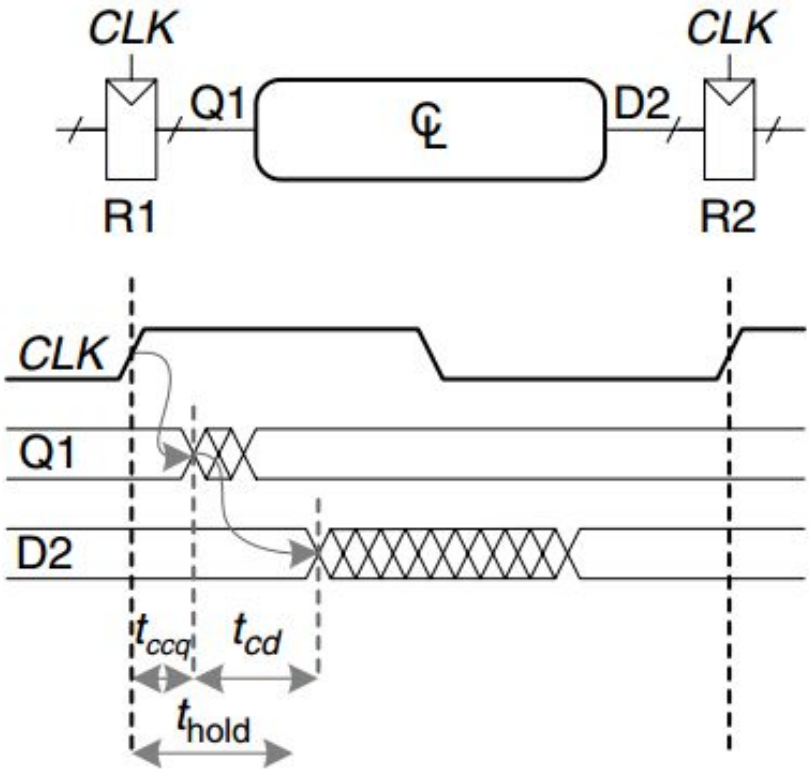


Timing constraints



$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

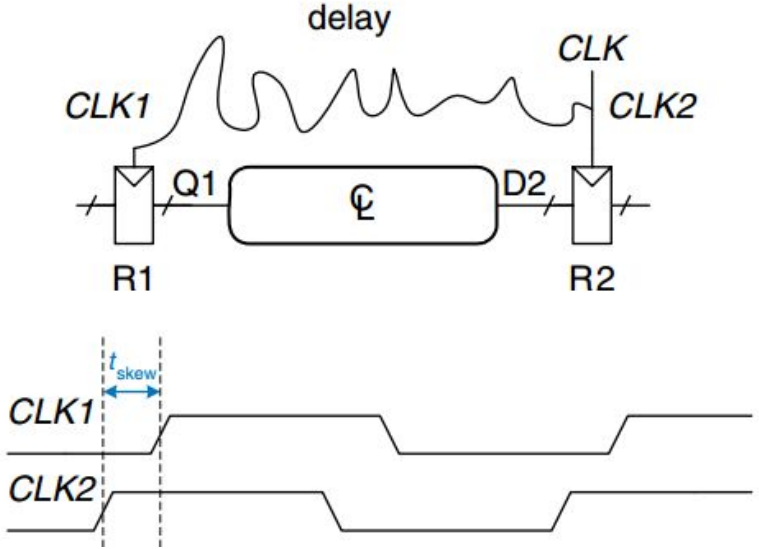
Timing constraints



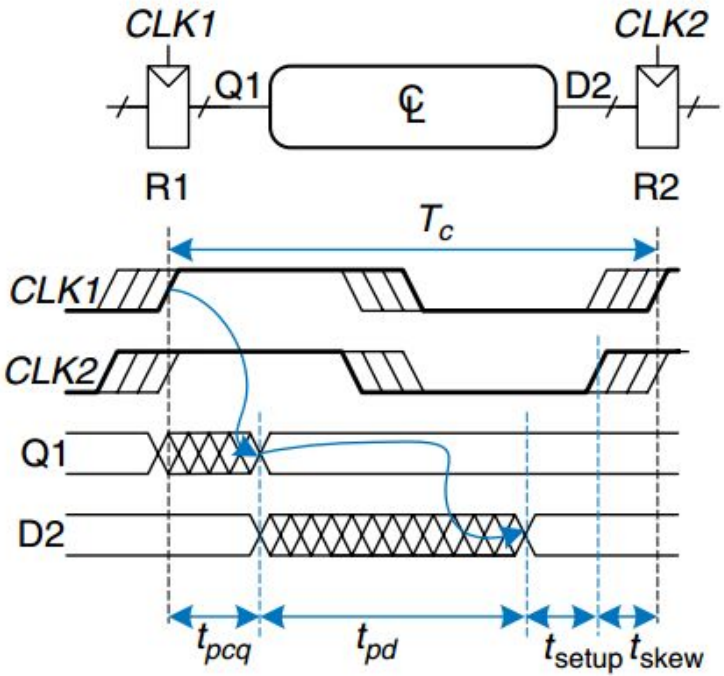
$$t_{ccq} + t_{cd} \geq t_{\text{hold}}$$

Timing constraints

We assumed that the clock reaches all components at exactly same time. In reality, wires from clock source to different components may be of different lengths resulting in a slight variation in clock edges. This is called *clock skew.*



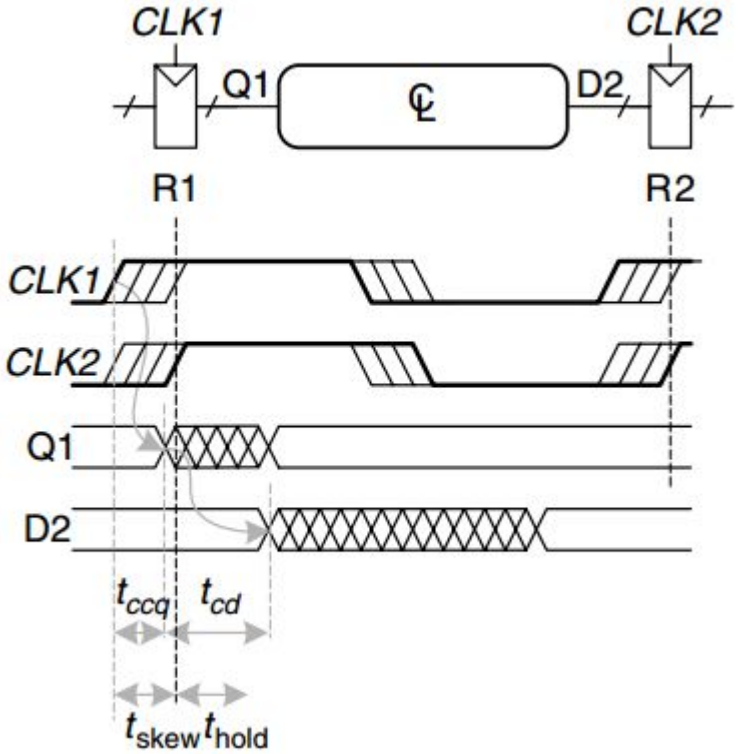
Timing constraints



In the worst case, R1 receives the latest skewed clock and R2 receives the earliest skewed clock, leaving as little time as possible for data to propagate between the registers.

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} + t_{\text{skew}}$$

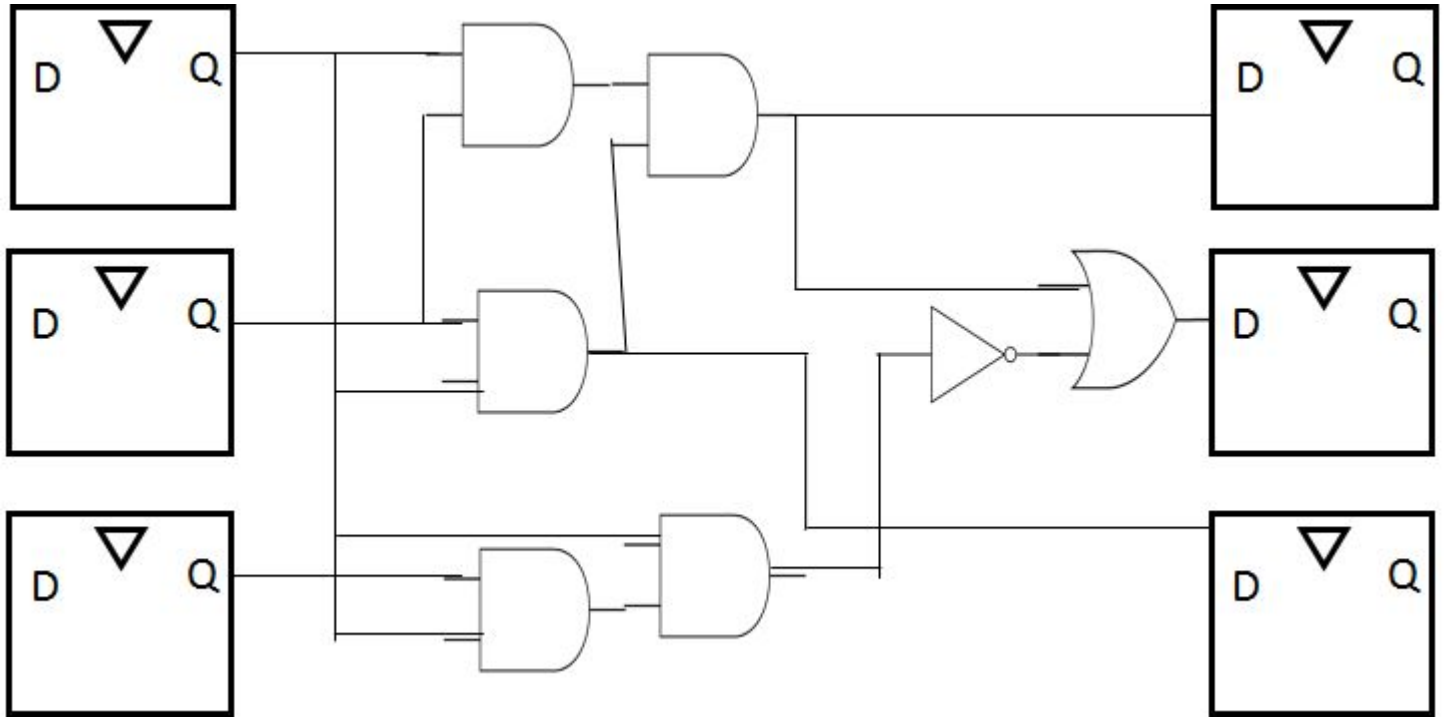
Timing constraints



In the worst case, R1 receives an early skewed clock, *CLK*1, and R2 receives a late skewed clock, *CLK*2. The data zips through the register and combinational logic but must not arrive until a hold time after the late clock.

$$t_{ccq} + t_{cd} \geq t_{\text{hold}} + t_{\text{skew}}$$

Timing constraints example



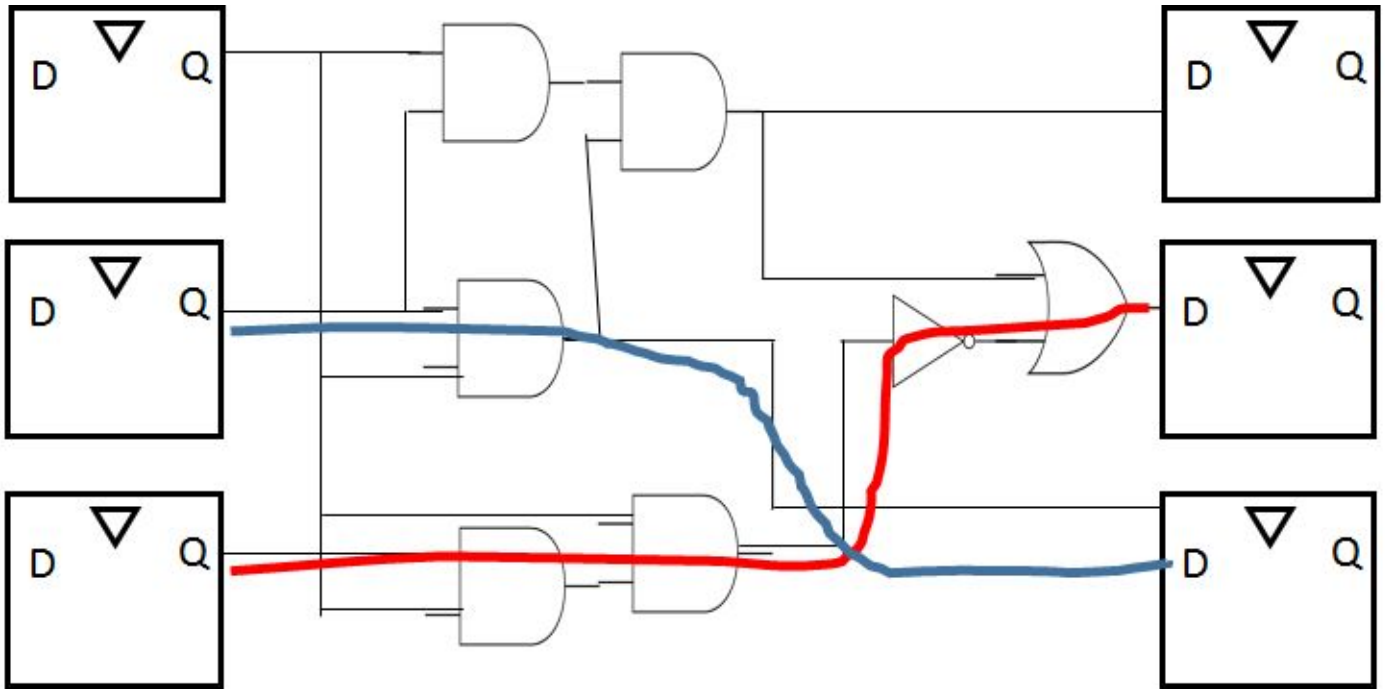
D-FF:
- t_ccq = 40
- t_pcq = 60
- t_setup = 70
- t_hold = 80

Gates:
AND:
- t_pd = 40
- t_cd = 30

OR:
- t_pd = 40
- t_cd = 30

NOT:
- t_pd = 30
- t_cd = 20

Timing constraints example



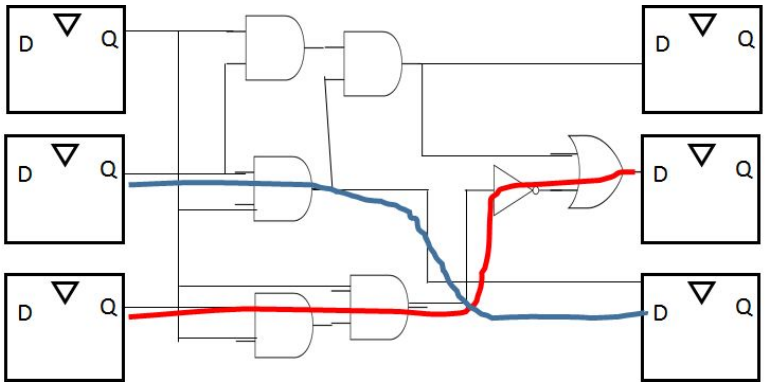
D-FF:
- t_ccq = 40
- t_pcq = 60
- t_setup = 70
- t_hold = 80

Gates:
AND:
- t_pd = 40
- t_cd = 30

OR:
- t_pd = 40
- t_cd = 30

NOT:
- t_pd = 30
- t_cd = 20

Timing constraints example



Setup time constraints:

$T_c \geq t_{pcq} + t_{pd} + t_{setup}$

$T_c \geq (60) + (3*40 + 30) + 70$

$T_c \geq 280ps$

Hold time constraints:

$t_{hold} < t_{ccq} + t_{cd}$

$80 < 40 + 30$ ----> NO !!

----> add buffer !

Thank you!