

Lecture 1:

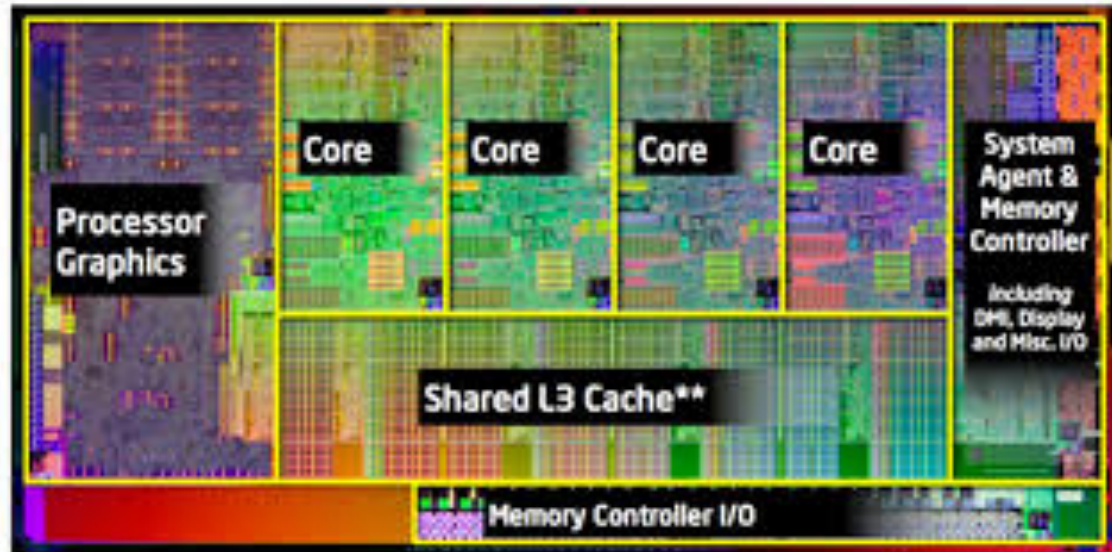
Introduction to Digital Logic Design

CSE 140: Components and Design Techniques for Digital Systems

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University of California, San Diego

What is inside your processor?



Logistics: Resources

Class **website**: <http://cseweb.ucsd.edu/classes/wi15/cse140-ab/index.html>

- *Approx. Syllabus*
- Detailed schedule
- Readings
- Assignments
- Grading policy
- HW submissions (TED)
- Content/announcements through Piazza
- Grades will be posted on Grade Source

Logistics: Course Components

Grading (grade on style, completeness and correctness)

- 10% Homework
- 30% Midterm (Best 1 of 2)
- 20% Quiz, iclicker based (Best 4 of 5) (Dates will be announced in advance via Piazza)
- 40% Final Exam
- If more than 60% of the class fill out CAPE evaluations, lowest homework and quiz score will be dropped
- Standard scale for assigning letter grades: 90-100 = A-/A/A+; 80-89.9=B-/B/B+, 50-79.9=C-/C/C+, 40-49.9=D, less than 40=F. Plusses and minuses will be given at the instructor's discretion.

Logistics: Textbooks

Required text:

- **[Harris]** Digital Design and Computer Architecture, D.M. Harris and S.L. Harris, Morgan Kaufmann, 2013 (2nd Edition).

Other references:

- **[Lang]**: “Digital Systems and Hardware/Firmware Algorithms” by Milos D. Ercegovac and Tomas Lang

In class we will use Clickers!



- Lets you vote on multiple choice questions in real time.

Information about TAs

***TAs and tutors shared between sections A and B**

1. Vineel Pratap Konduru
2. Anup Chenthamarakshan
3. Pallavi Agarwal
4. Anand Anand
5. Michael Chin
6. Jennifer He
7. Ben Martin
8. Ryan McClure
9. Alvin See
10. Nan Shu
11. Harvey Yu

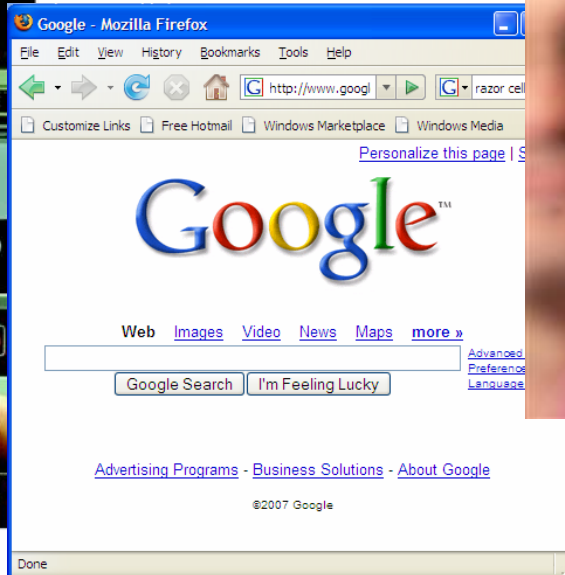
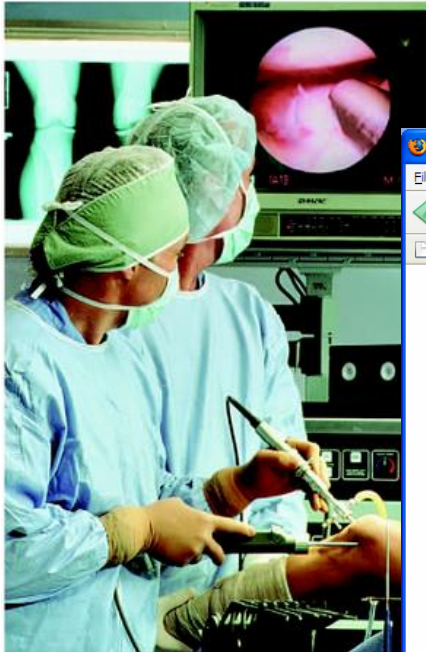
Office hours and emails available
on the course website (Check
weekly)

Course Problems...Cheating

- What is cheating?
 - Studying together in groups is encouraged
 - Turned-in work must be *completely* your own.
 - Copying someone else's solution on a HW or exam is cheating
 - Both “giver” and “receiver” are equally culpable
- Cheating on HW/ exams: in most cases, F in the course.
- Any instance of cheating will be referred to Academic Integrity Office

Motivation

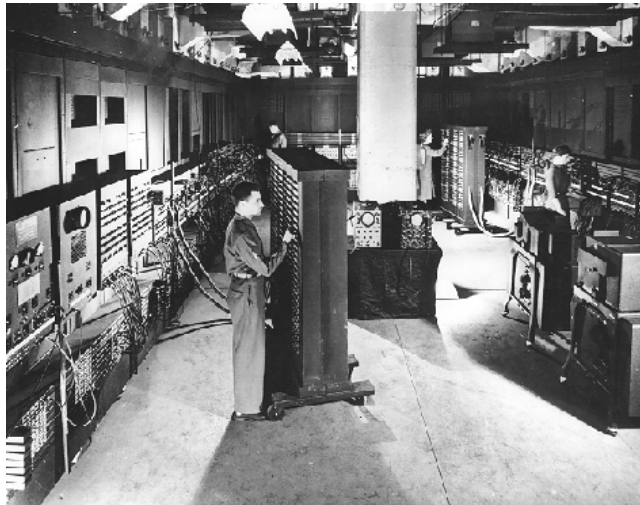
- Microelectronic technologies have revolutionized our world: cell phones, internet, rapid advances in medicine, etc.
- The semiconductor industry has grown from \$21 billion in 1985 to \$268 billion in 2007.



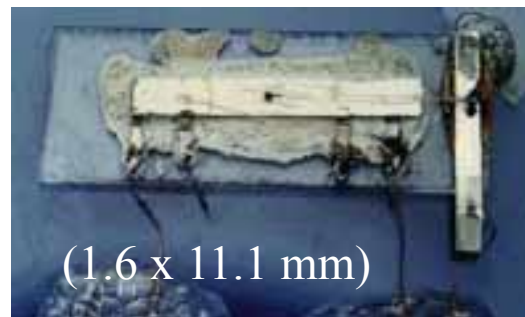
The Digital Revolution

Integrated Circuit: Many digital operations on the same material

Vacuum tubes

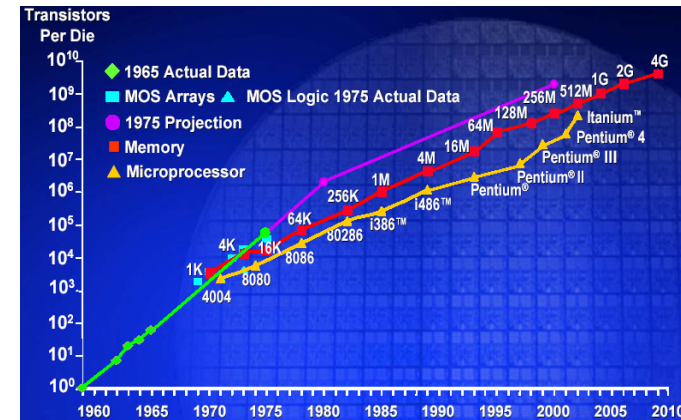


ENIAC



Integrated Circuit

Exponential Growth of Computation



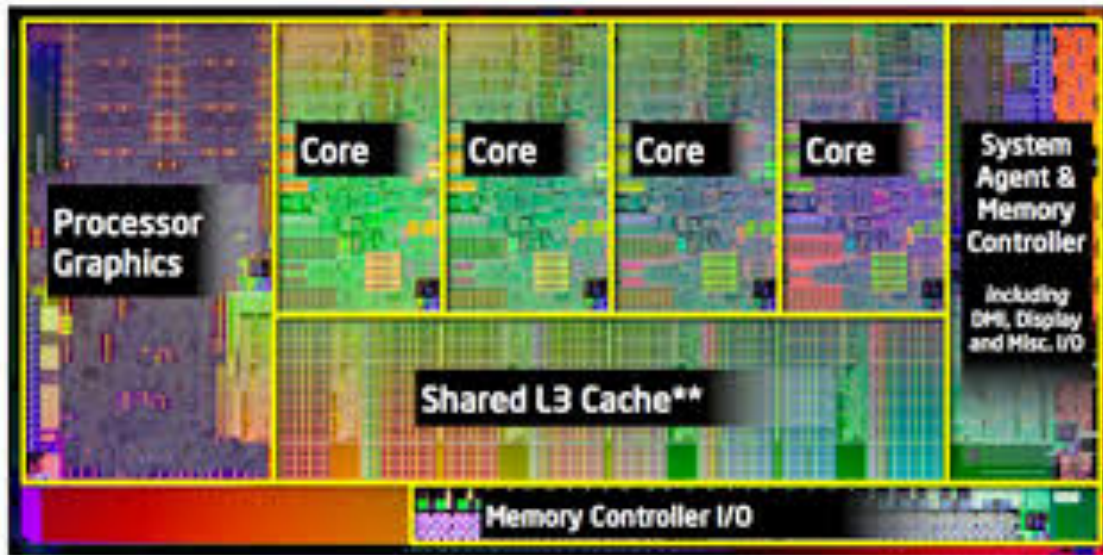
Moore's Law

WWII Stored Program Model

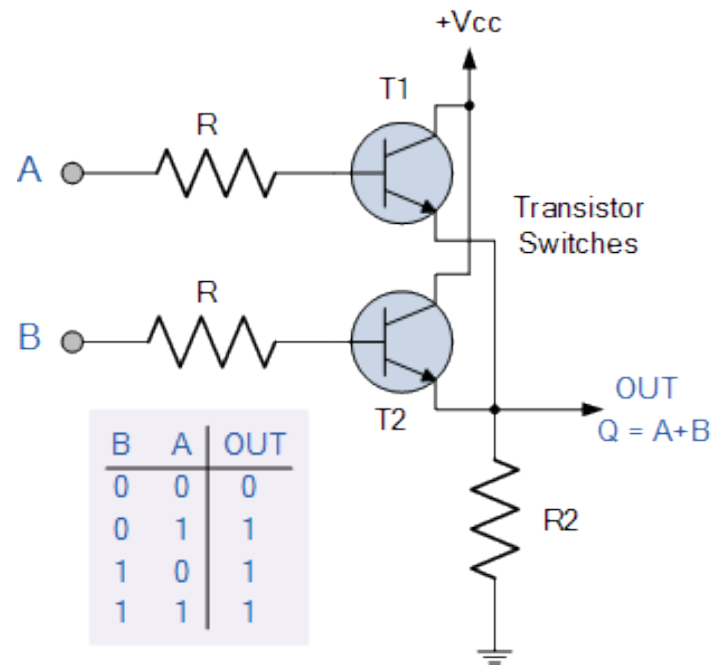
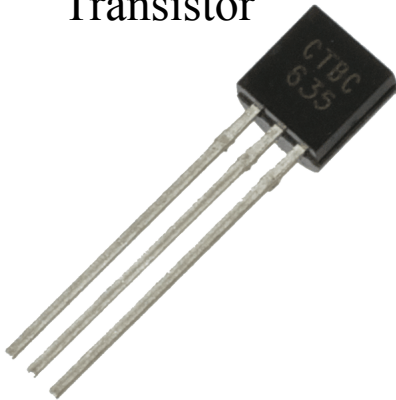
1949

1965

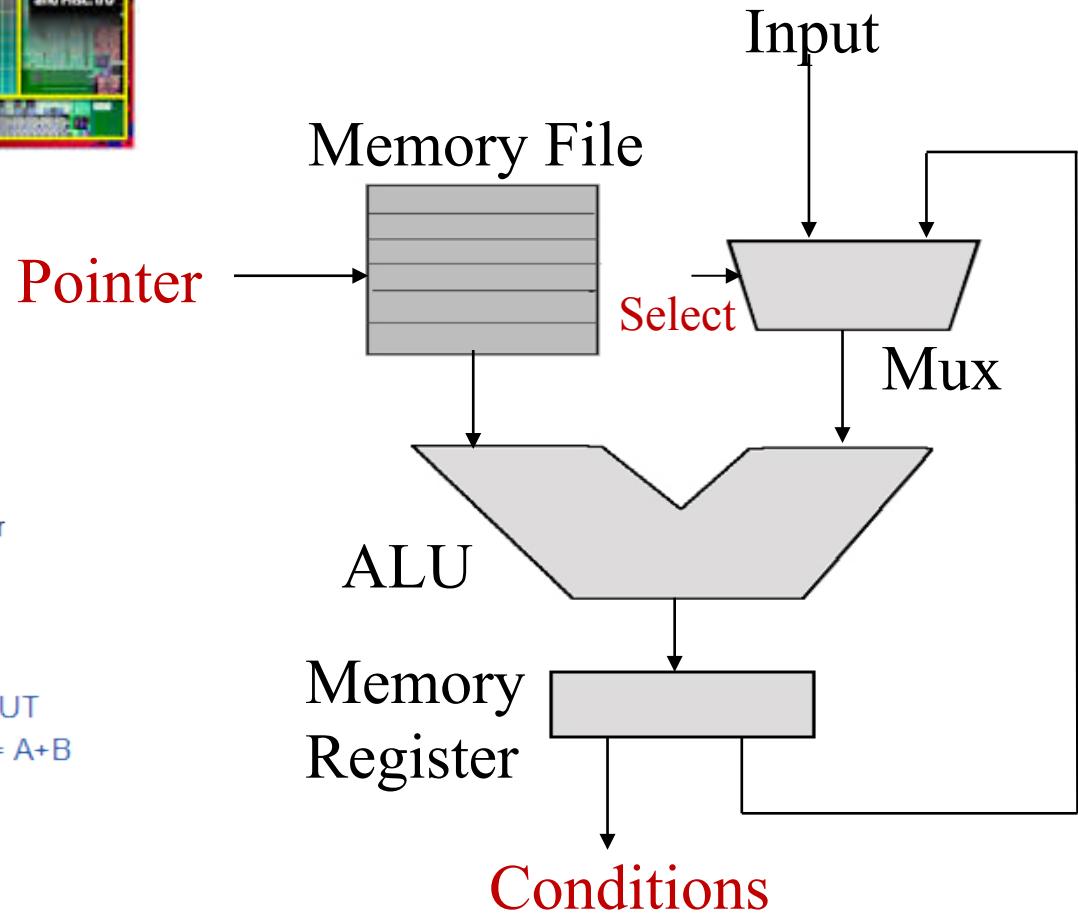
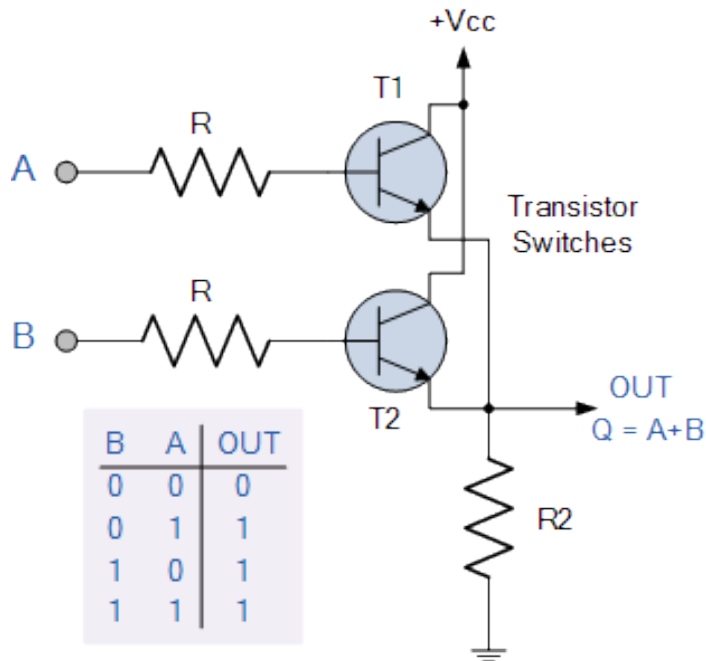
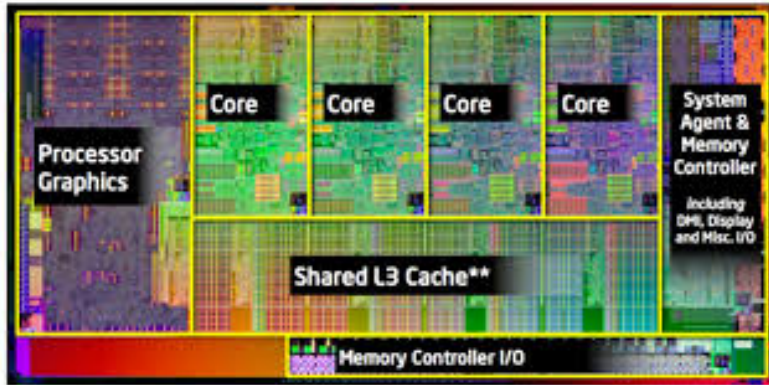
Building complex circuits



Transistor

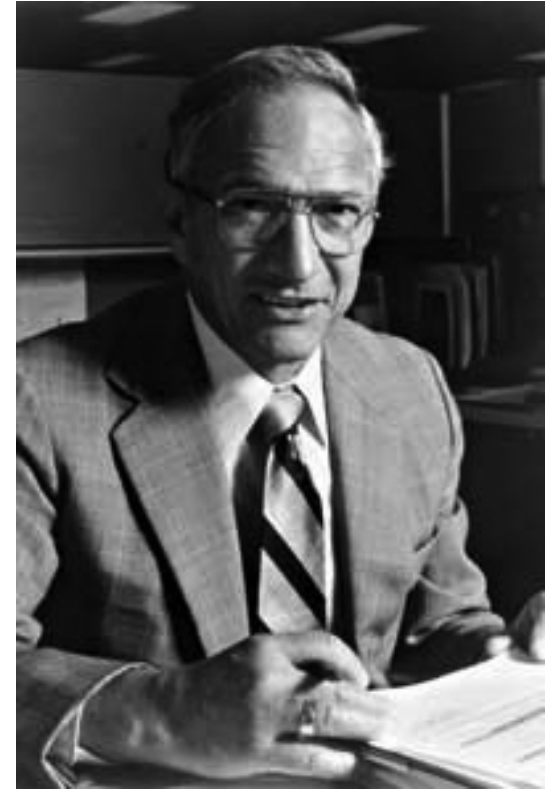


Building complex circuits



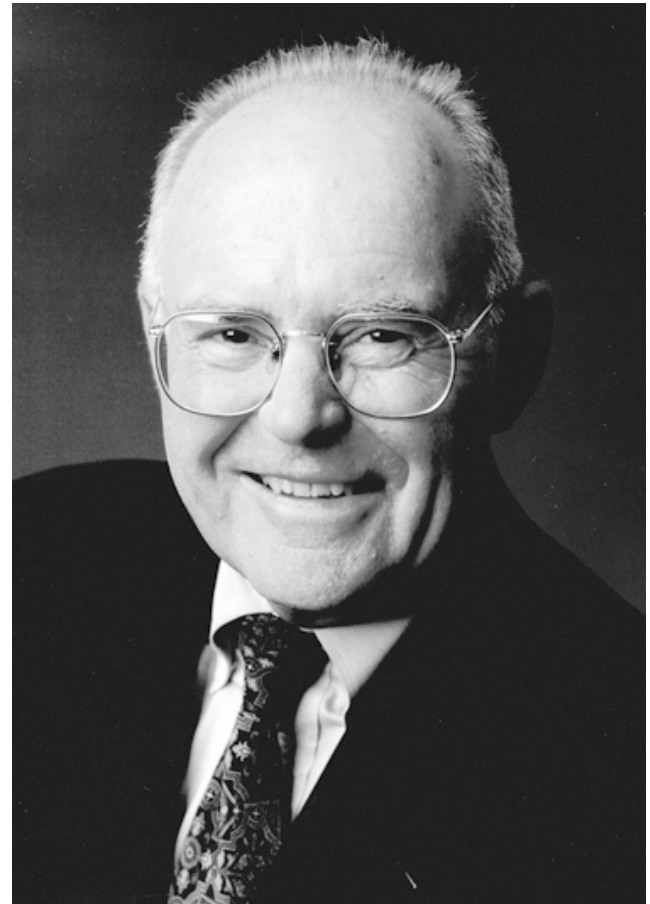
Robert Noyce, 1927 - 1990

- Nicknamed “Mayor of Silicon Valley”
- Co-founded Fairchild Semiconductor in 1957
- Co-founded Intel in 1968
- Co-invented the integrated circuit



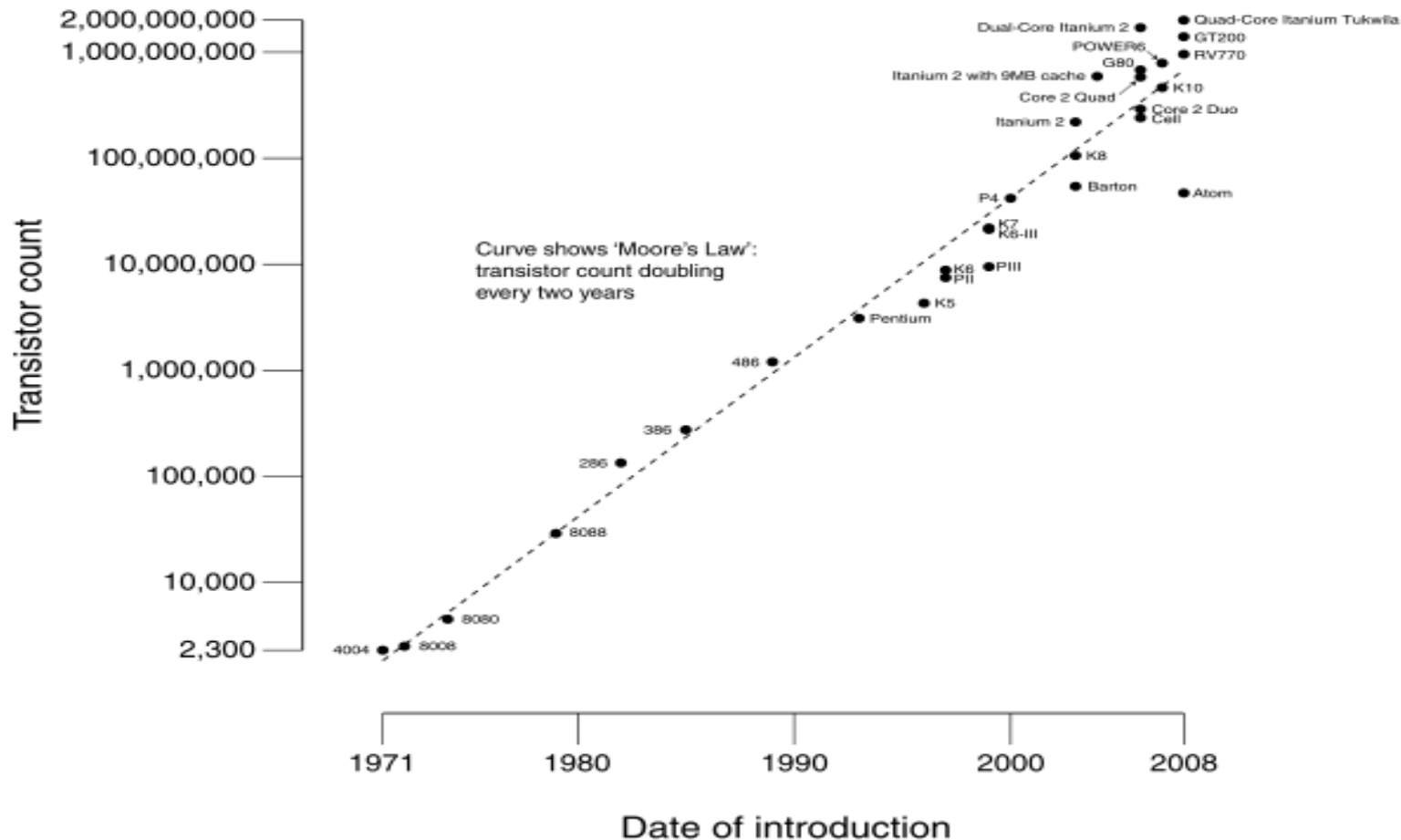
Gordon Moore

- Cofounded Intel in 1968 with Robert Noyce.
- **Moore's Law:** the number of transistors on a computer chip doubles every 1.5 years (observed in 1965)



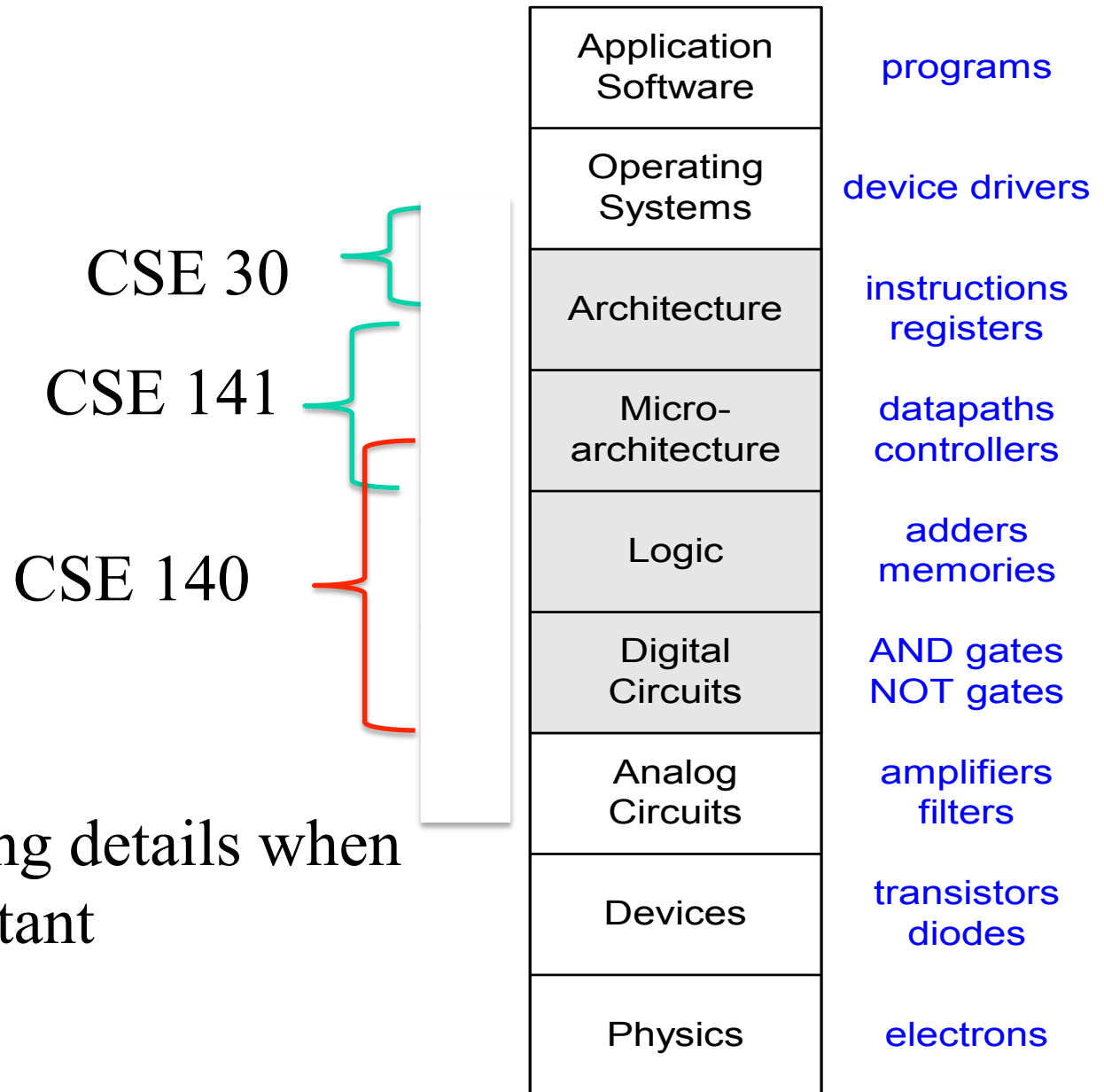
Technology Trends: Moore's Law

CPU Transistor Counts 1971-2008 & Moore's Law



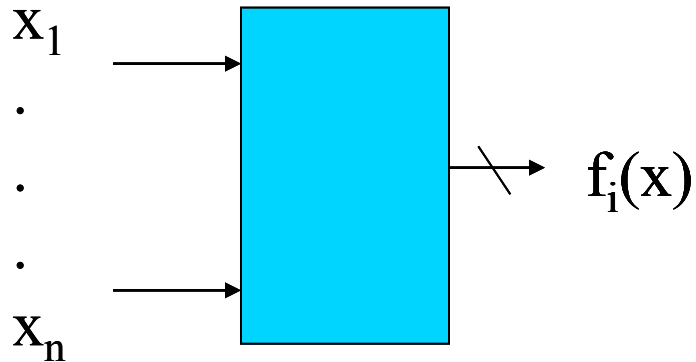
- Since 1975, transistor counts have doubled every two years.

Principle of Abstraction



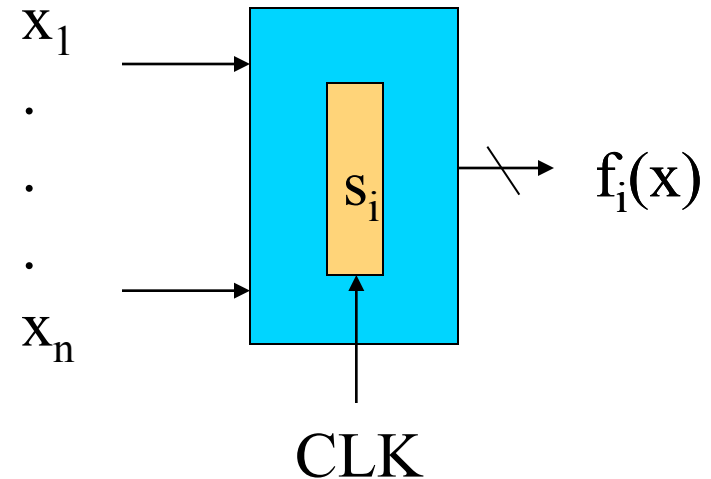
Abstraction: Hiding details when they aren't important

Combinational Logic vs Sequential Network



Combinational logic:

$$y_i = f_i(x_1, \dots, x_n)$$



Sequential Networks

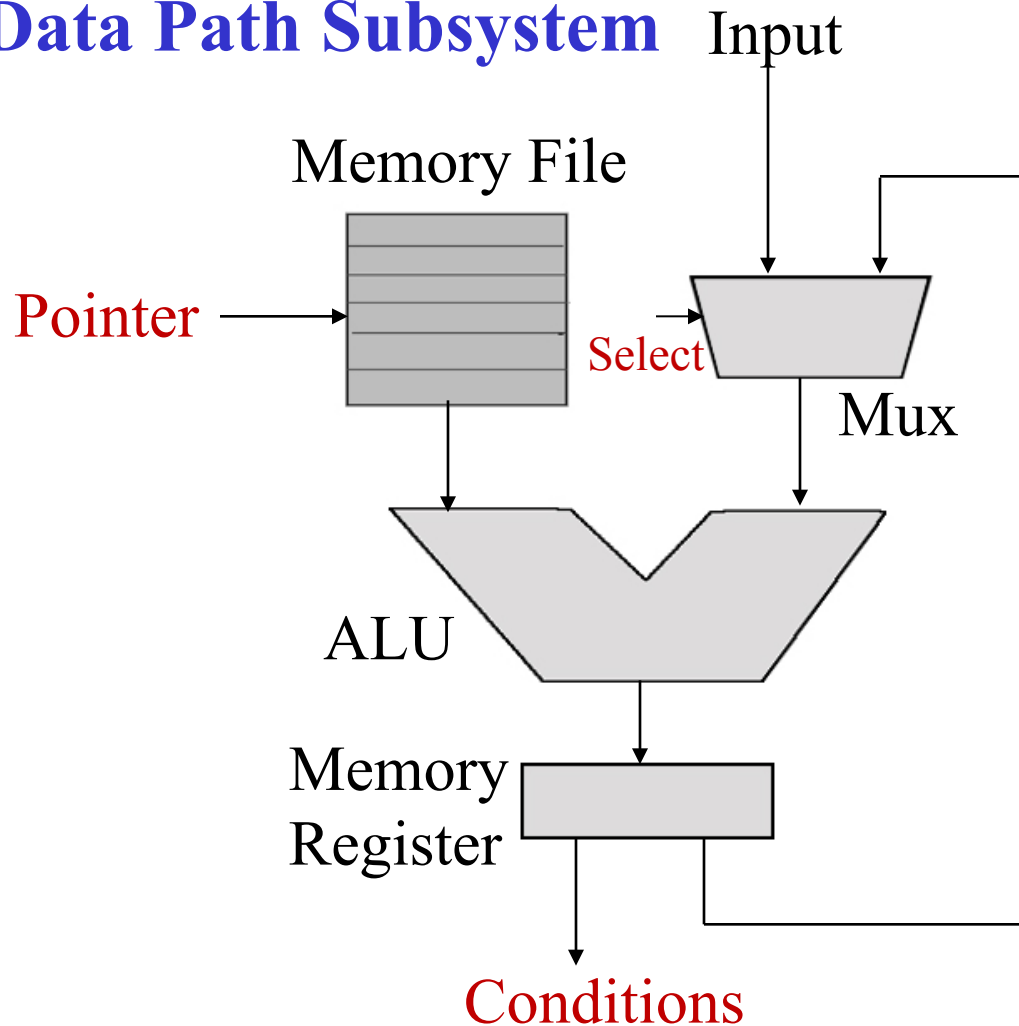
1. Memory
2. Time Steps (Clock)

$$y_i^t = f_i(x_1^t, \dots, x_n^t, s_1^t, \dots, s_m^t)$$

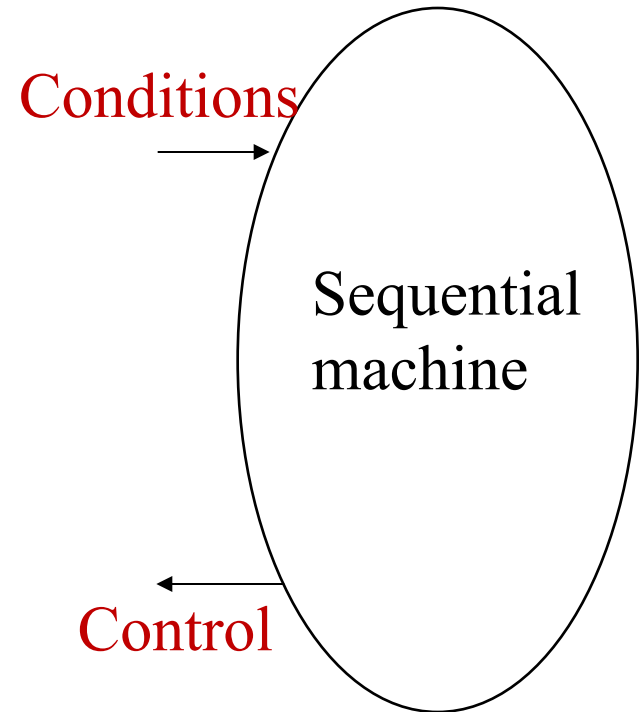
$$s_i^{t+1} = g_i(x_1^t, \dots, x_n^t, s_1^t, \dots, s_m^t)$$

Scope: Overall Picture of CS140

Data Path Subsystem



Control Subsystem



CLK: Synchronizing Clock

Scope

- The purpose of this course is that we:
 - Learn the principles of digital design
 - Learn to systematically debug increasingly complex designs
 - Design and build digital systems
 - Learn what's under the hood of an electronic component

We will cover four major things in this course:

- Combinational Logic (Harris-Chap 2)
- Sequential Networks (Harris-Chap 3)
- Standard Modules (Harris-Chap 5)
- System Design (Harris-Chap 4, 6-8)

Scope

Subjects	Building Blocks	Theory
Combinational Logic	AND, OR, NOT, XOR	Boolean Algebra
Sequential Network	AND, OR, NOT, FF	Finite State Machine
Standard Modules	Operators, Interconnects, Memory	Arithmetics, Universal Logic
System Design	Data Paths, Control Paths	Methodologies