

Lecture 19:

Sequential Networks: Timing (contd), Standard Modules

CSE 140: Components and Design Techniques for
Digital Systems

Diba Mirza
Dept. of Computer Science and Engineering
University of California, San Diego

Announcements

- We will have lecture on Friday (02/27)
- Students registered in Section A
 - Lecture at CENTER 109 at noon
- Students registered in Section B:
 - Lecture at SOLIS 104 at 3pm

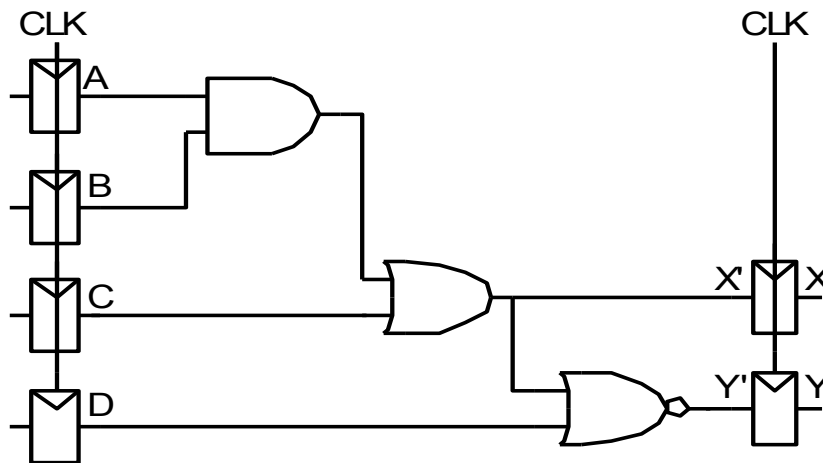
Important: Midterm 2 time and location

- Students registered in Section A:
 - Midterm at CENTER 216 at 2pm
- Students registered in Section B:
 - Midterm at SOLIS 104 at 2pm

Please check the section that you are registered in, this may be different from the one you normally attend lectures.

Timing Analysis

Timing Characteristics



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

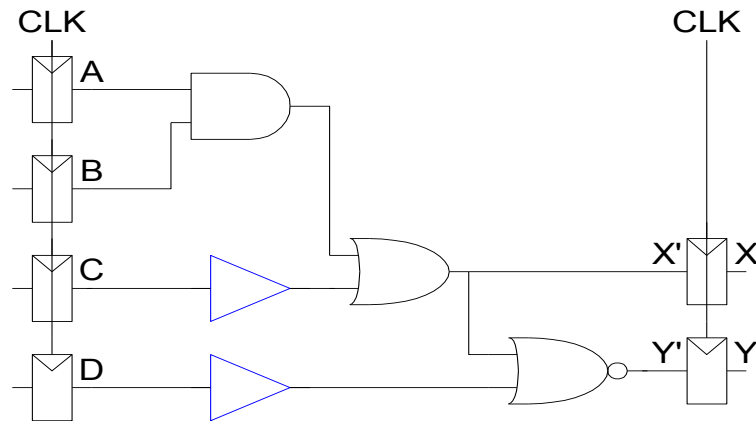
Hold time constraint:

$$t_{ccq} + t_{cd} > t_{\text{hold}} ?$$

$$(30 + 25) \text{ ps} > 70 \text{ ps} ? \text{ No!}$$

Fixing Hold Time Violation

Add buffers to the short paths:



$$t_{pd} =$$

$$t_{cd} =$$

Setup time constraint:

$$T_c \geq$$

$$f_c =$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

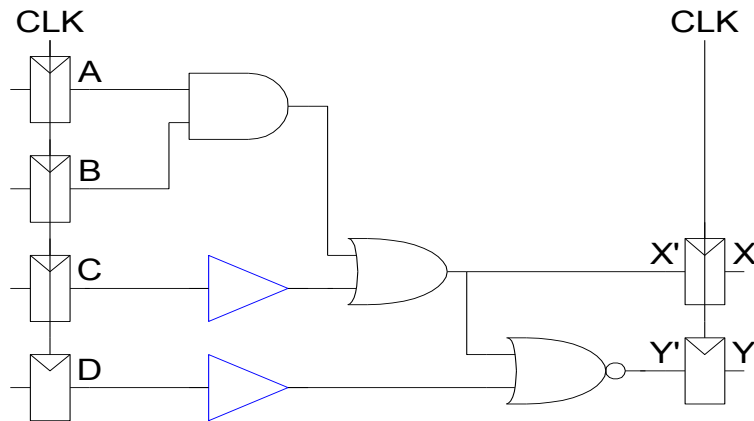
$$t_{cd} = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{\text{hold}} ?$$

Fixing Hold Time Violation

Add buffers to the short paths:



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 2 \times 25 \text{ ps} = 50 \text{ ps}$$

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

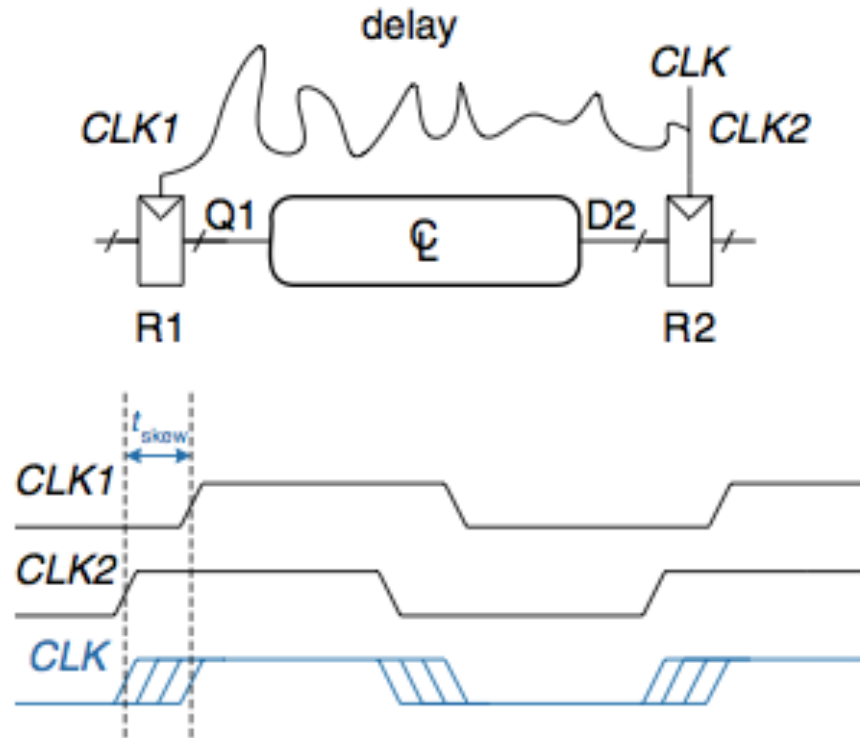
$$t_{cd} = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{\text{hold}} ?$$

$$(30 + 50) \text{ ps} > 70 \text{ ps} ? \text{ Yes!}$$

Clock Skew



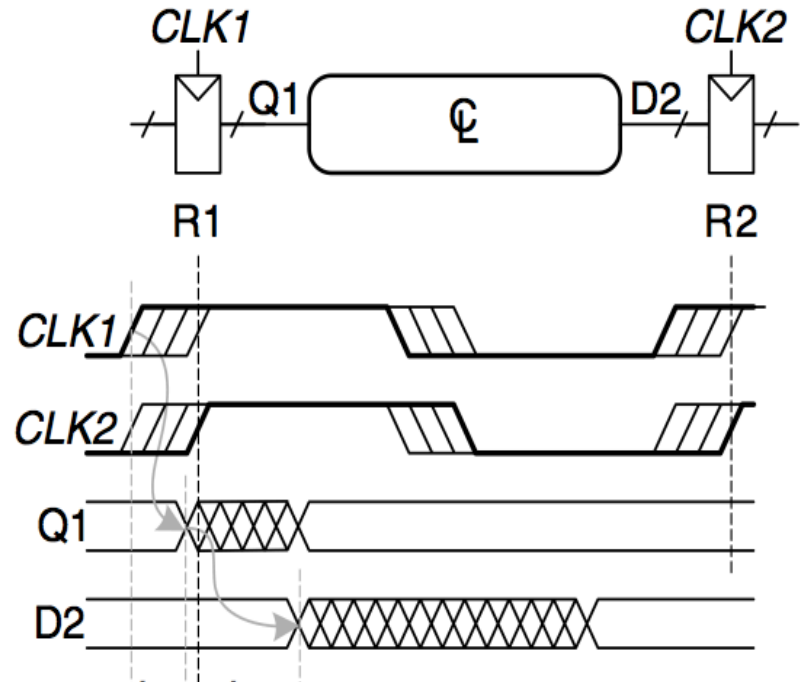
- The clock doesn't arrive at all registers at the same time
- Skew is the difference between two clock edges
- Examine the worst case to guarantee that the dynamic discipline is not violated for any register – many registers in a system!

Setup time constraint

Consider a circuit where the setup constraint is satisfied for R2 when there is no clock skew.

If CLK 2 is delayed (as shown in the figure), would the setup constraint be still satisfied ?

- A. Yes
- B. No

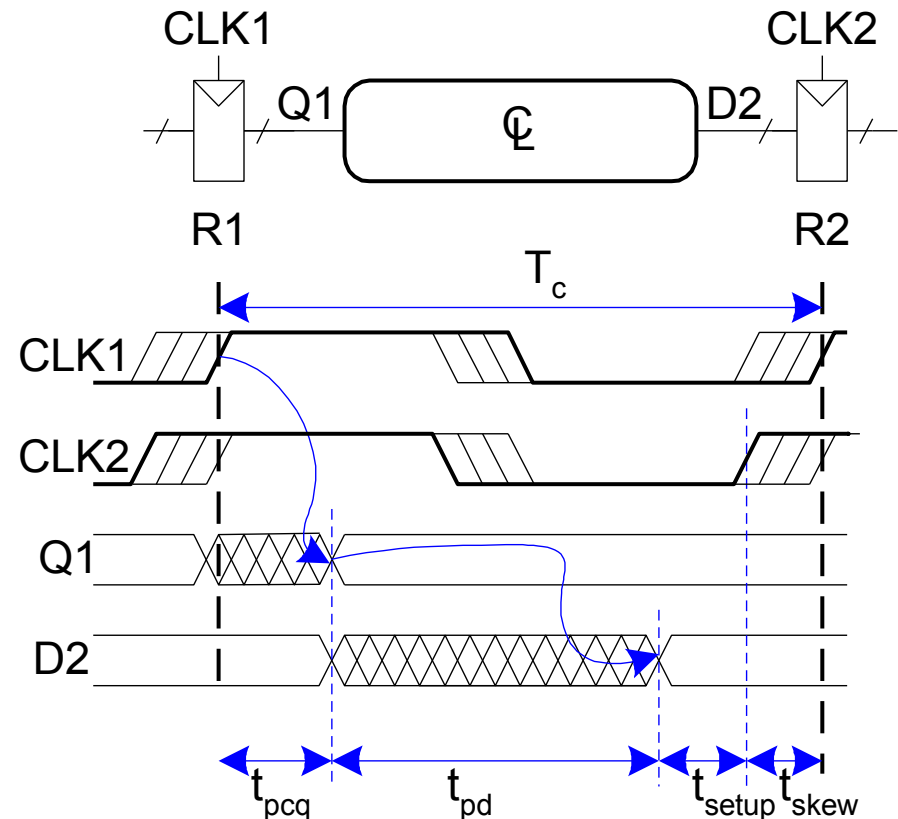


Setup Time Constraint with Clock Skew

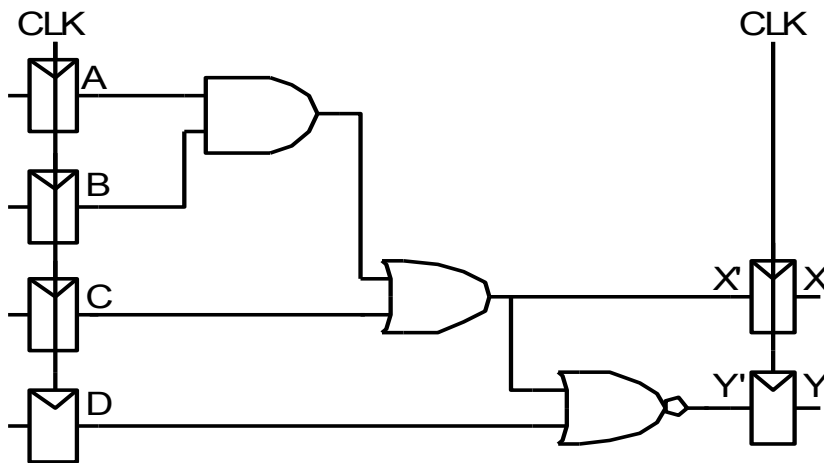
- In the worst case, the CLK2 is earlier than CLK1

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} + t_{\text{skew}}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}} + t_{\text{skew}})$$



Timing Analysis with clock skew



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

What is the minimum allowable clock period given that the clocks are skewed by 50ps?

- A. 215ps
- B. 265 ps
- C. None of the above

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

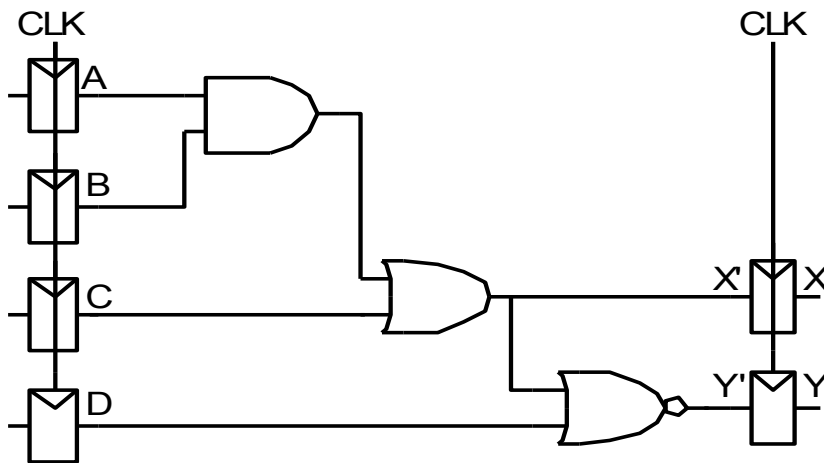
$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

$$t_{\text{skew}} = 50 \text{ ps}$$

Timing Analysis with clock skew



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

$$T_c \geq 265 \text{ ps}$$

$$f_c = 1/T_c = 3.77 \text{ GHz}$$

Without skew we got $f_c = 4.65 \text{ GHz}$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

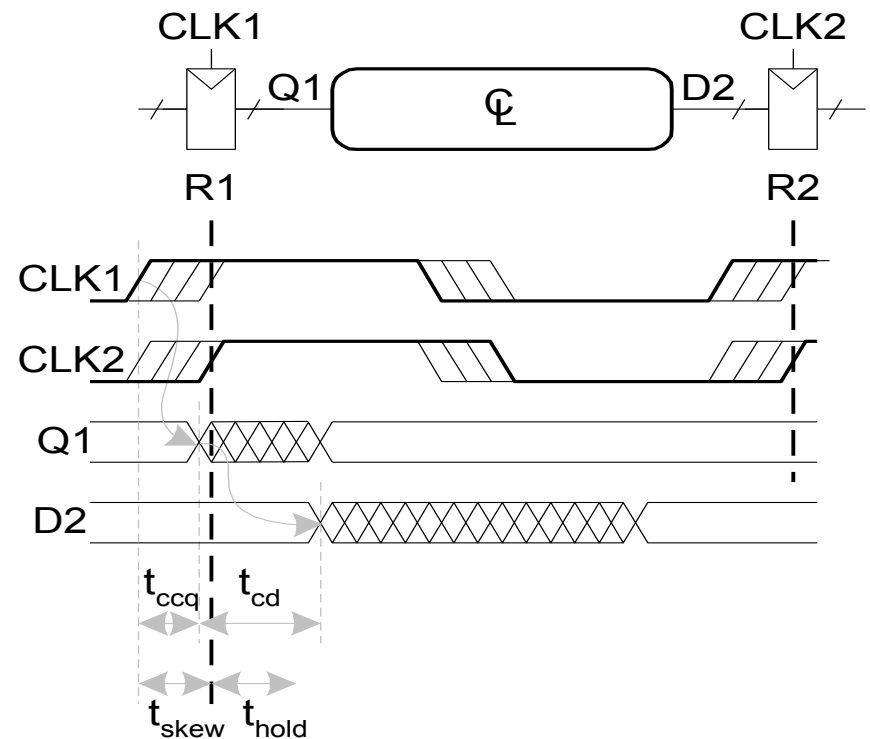
$$t_{\text{skew}} = 50 \text{ ps}$$

Hold Time Constraint with Clock Skew

- In the worst case, CLK2 is later than CLK1

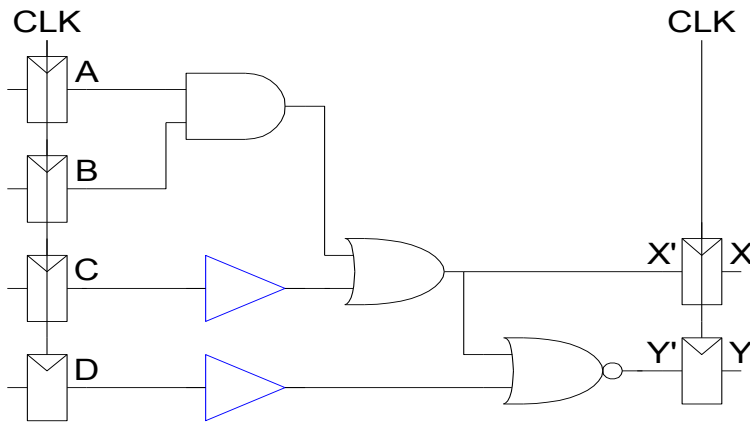
$$t_{ccq} + t_{cd} > t_{hold} + t_{skew}$$

$$t_{cd} > t_{hold} + t_{skew} - t_{ccq}$$



Hold Time Violation

Add buffers to the short paths:



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 2 \times 25 \text{ ps} = 50 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} + t_{skew}?$$

$$(30 + 50) \text{ ps} > (70 \text{ ps} + 50) \text{ ps} ?$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{setup} = 60 \text{ ps}$$

$$t_{hold} = 70 \text{ ps}$$

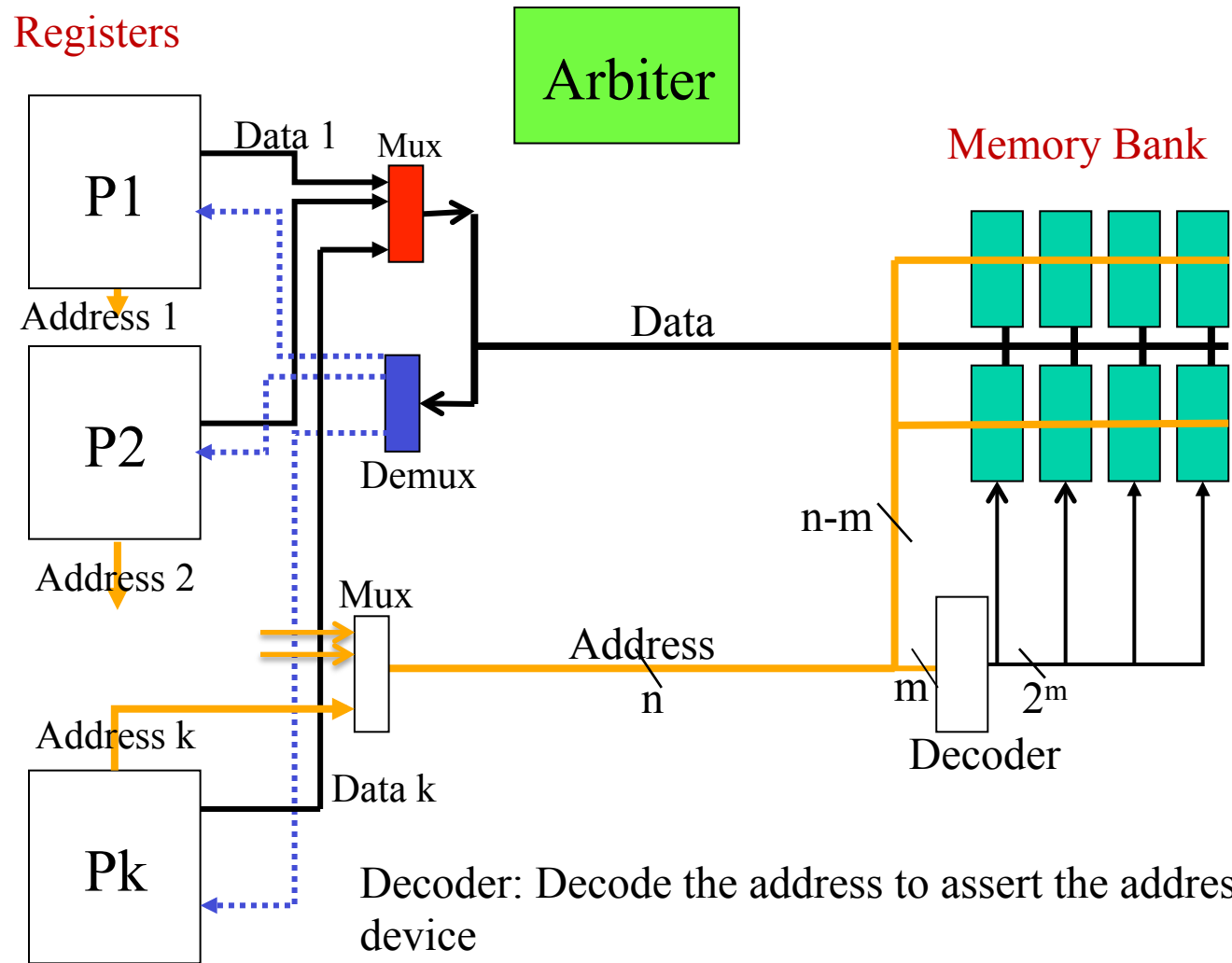
$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

$$t_{skew} = 50 \text{ ps}$$

STANDARD MODULES

Interconnect: Decoder, Encoder, Mux, DeMux



Decoder: Decode the address to assert the addressed device

Mux: Select the inputs according to the index addressed by the control signals

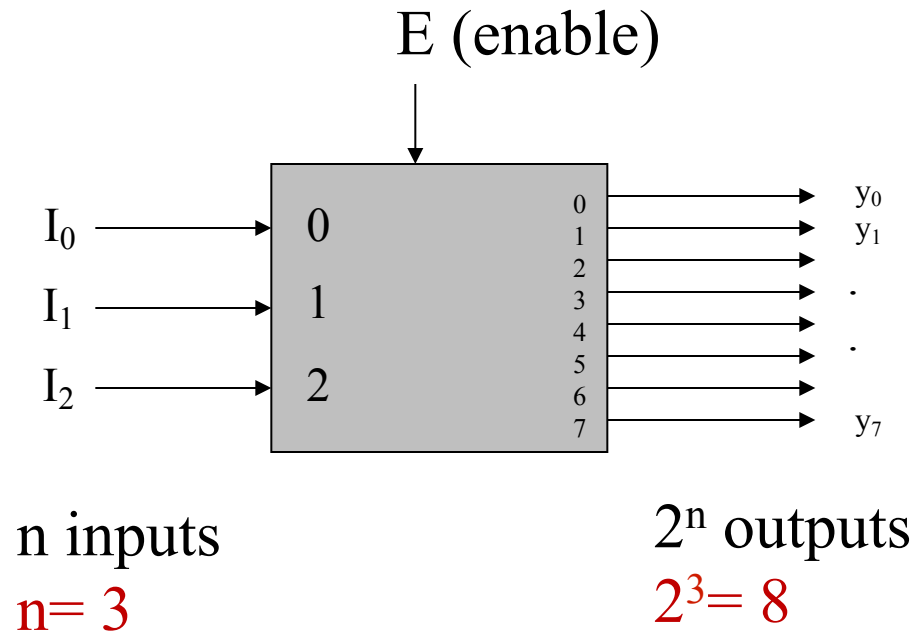
Part III. Standard Modules

Interconnect Modules:

1. Decoder, 2. Encoder

3. Multiplexer, 4. Demultiplexer

Decoder Definition: A digital module that converts a binary address to the assertion of the addressed device

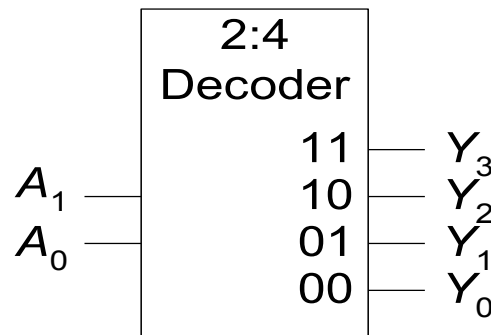


n to 2^n decoder
function:

$y_i = 1$ if $E= 1$ & $(I_2, I_1, I_0) = i$
 $y_i = 0$ otherwise

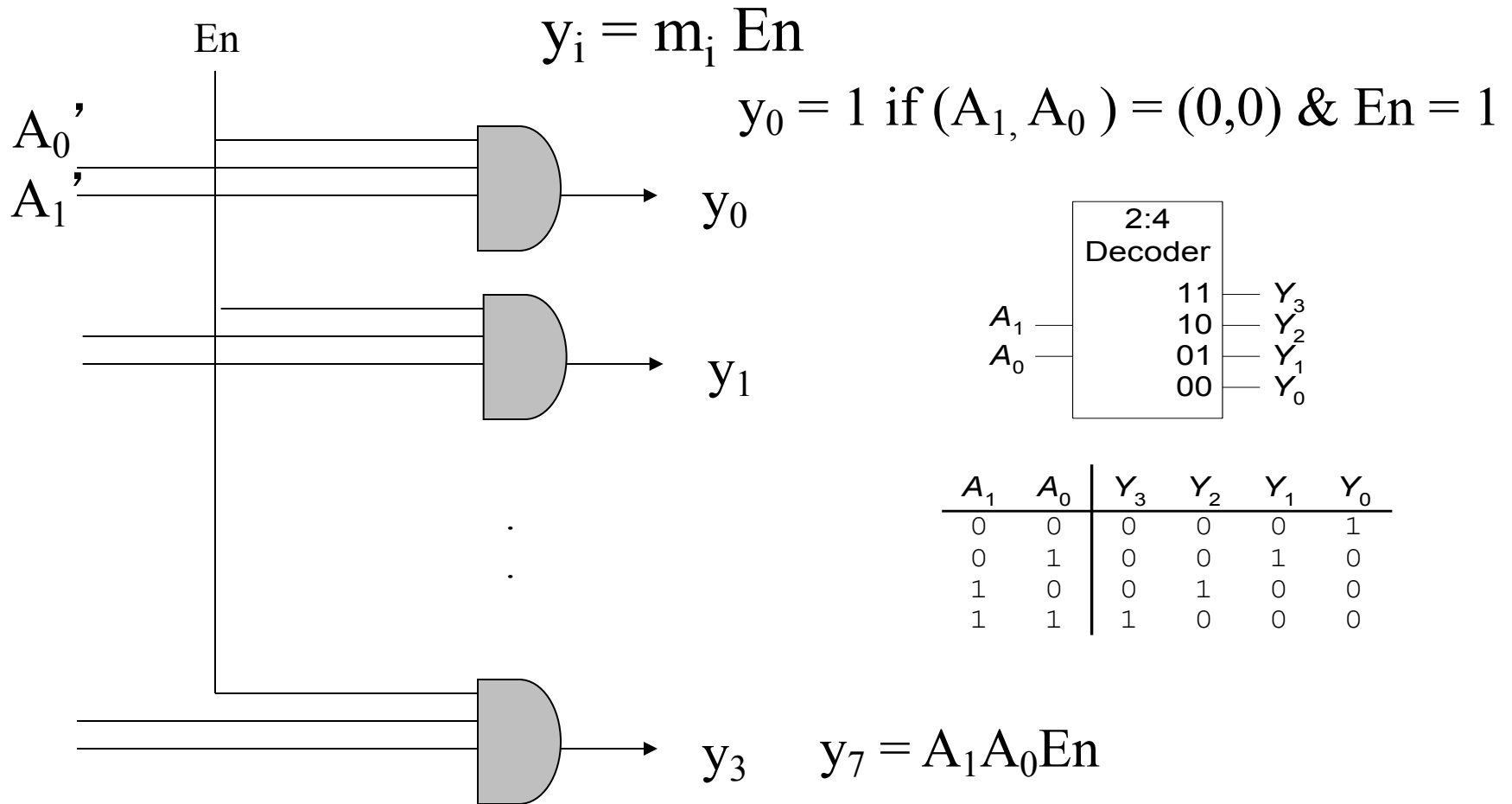
1. Decoder: Definition

- N inputs, 2^N outputs
- One-hot outputs: only one output HIGH at any point in time



A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

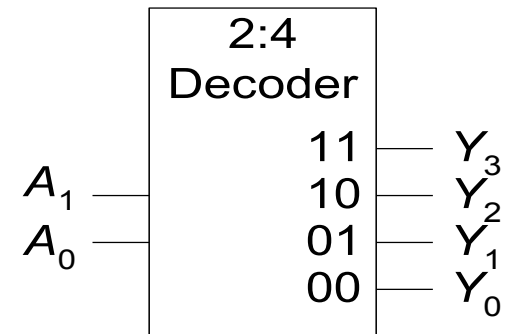
Decoder: Logic Diagram (Inside a decoder)



1. Decoder: Definition

PI Q: What is the output $Y_{3:0}$ of the 2:4 decoder for $(A_1, A_0) = (1, 0)$?

- A. (1, 1, 0, 0)
- B. (1, 0, 1, 1)
- C. (0, 0, 1, 0)
- D. (0, 1, 0, 0)



Implementing functions using Decoders

- OR minterms

