

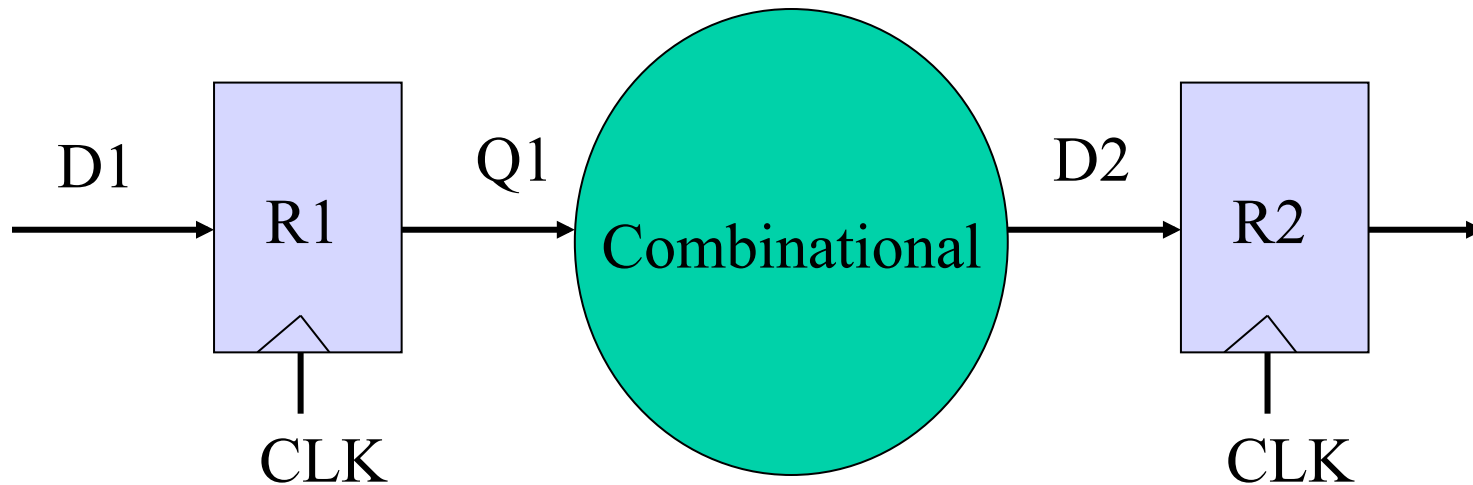
Lecture 18:

Sequential Networks: Timing and Retiming

CSE 140: Components and Design Techniques for
Digital Systems

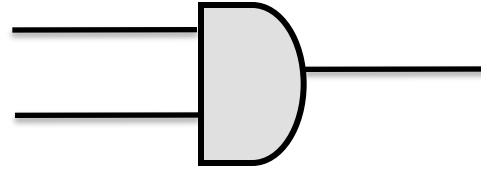
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Fact 1: Once a flip flop has been ‘built’ we are stuck with its timing characteristics: t_{setup} , t_{hold} , t_{ccq} , t_{pcq}



Now let's look at the timing characteristics of the combinational part

Combinational Logic Timing



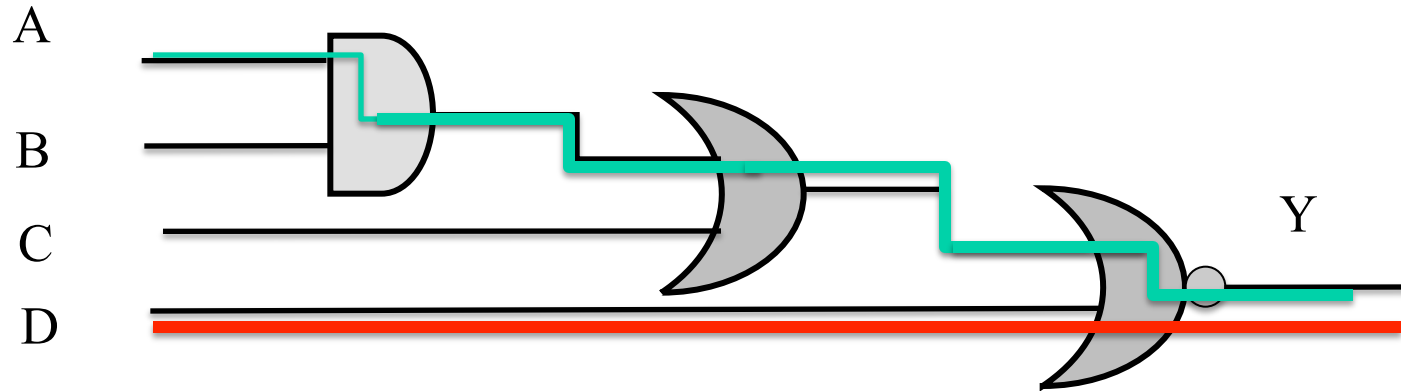
I. Min delay of a gate, also called Contamination delay: t_{cd}

Minimum time from when an input changes until the output *starts* to change

II. Max delay of a gate, also called Propagation delay: t_{pd}

Maximum time from when an input changes until the output *is* guaranteed to reach its final value (i.e., stop changing)

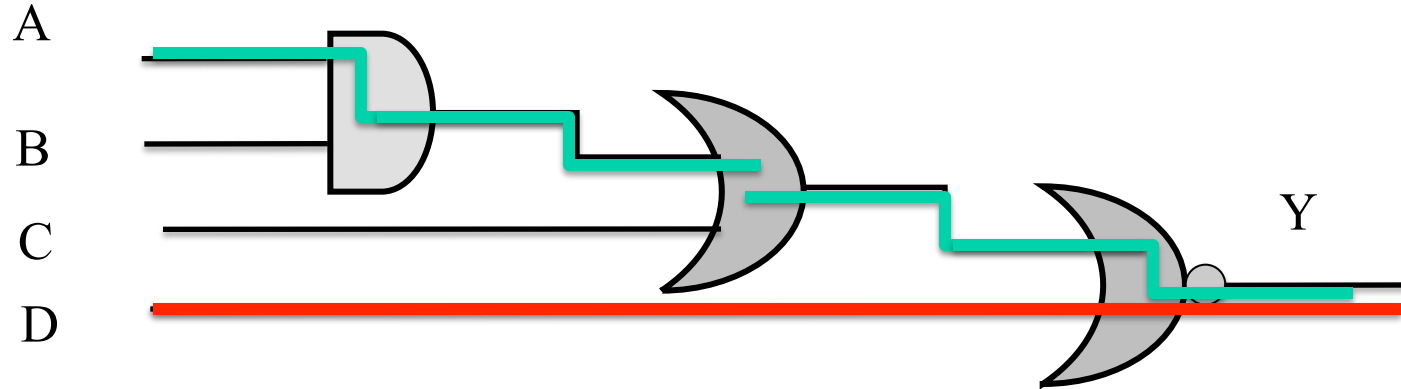
Combinational Logic: Output timing constraints



PI Q: Which path in the above circuit determines the **contamination** delay of the circuit (assuming the delay of all the gates is the same)?

- A. Green path
- B. Red path
- C. Both
- D. Neither

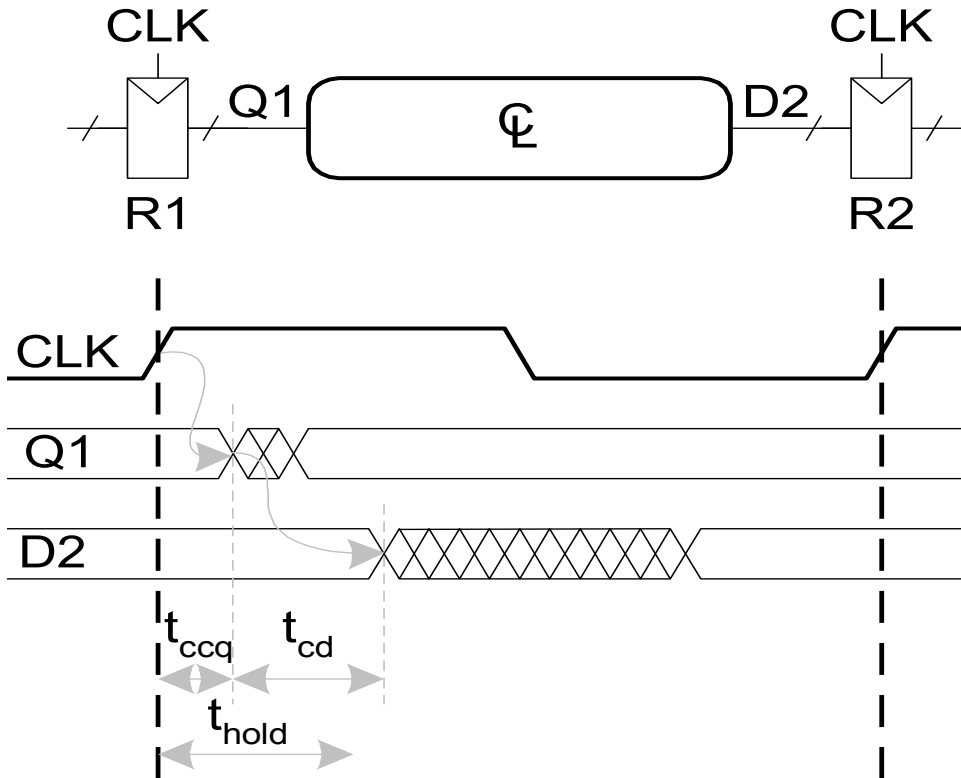
Combinational Logic: Output timing constraints



PI Q: Which path in the above circuit determines the **propagation** delay of the circuit (assuming the delay of all the gates is the same)?

- A. Green path
- B. Red path
- C. Both
- D. Neither

Formalizing the hold time constraint in Sequential Circuits

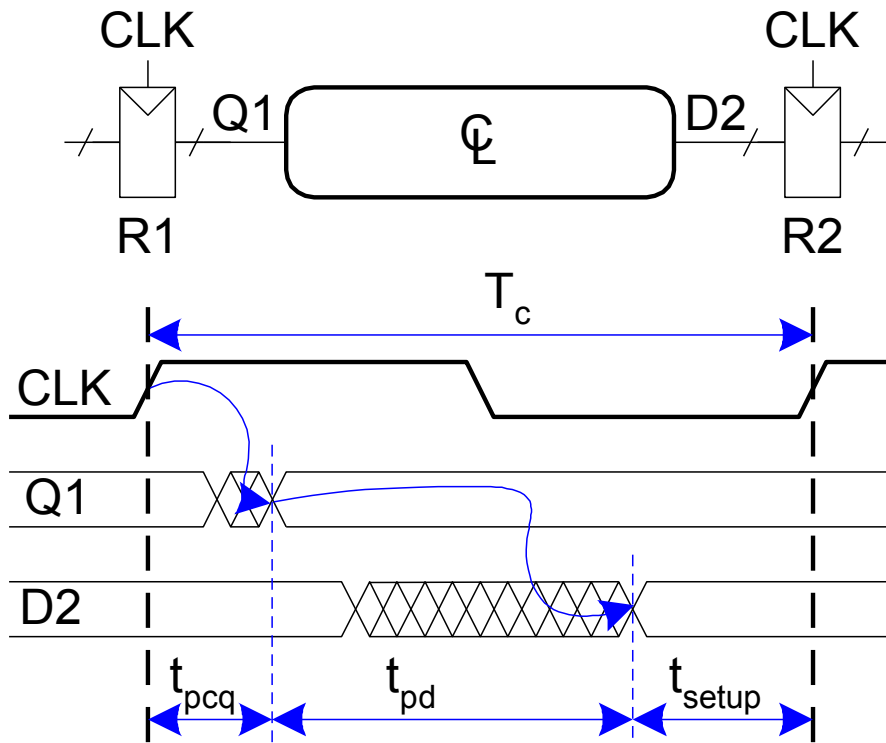


To meet the hold time constraint:

$$t_{\text{hold}} < \text{min delay}(\text{flipflop}) + \text{min delay}(\text{combinational})$$

$$t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}}$$

Formalizing the setup time constraints in Sequential Circuits



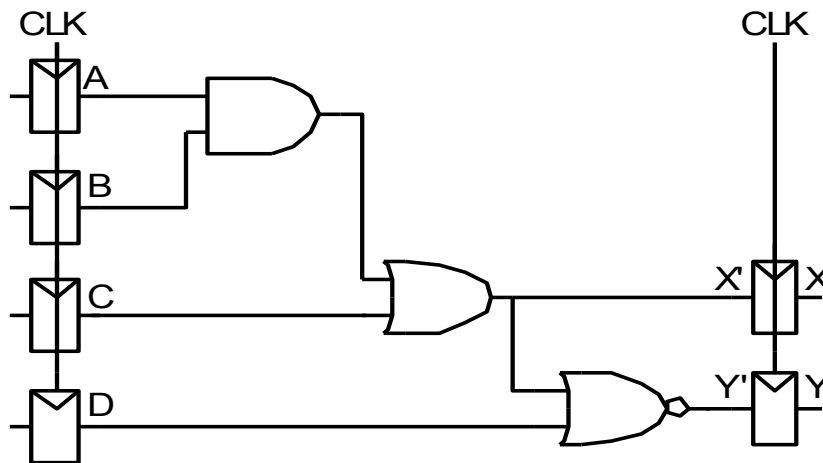
To meet the setup time constraint:

$$T_c \geq \max \text{delay}(\text{flipflop}) + \max \text{delay}(\text{combinational}) + t_{\text{setup}}$$

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

Timing Analysis

Timing Characteristics



$$t_{pd} =$$

$$t_{cd} =$$

Setup time constraint:

$$T_c \geq$$

$$f_c = 1/T_c =$$

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

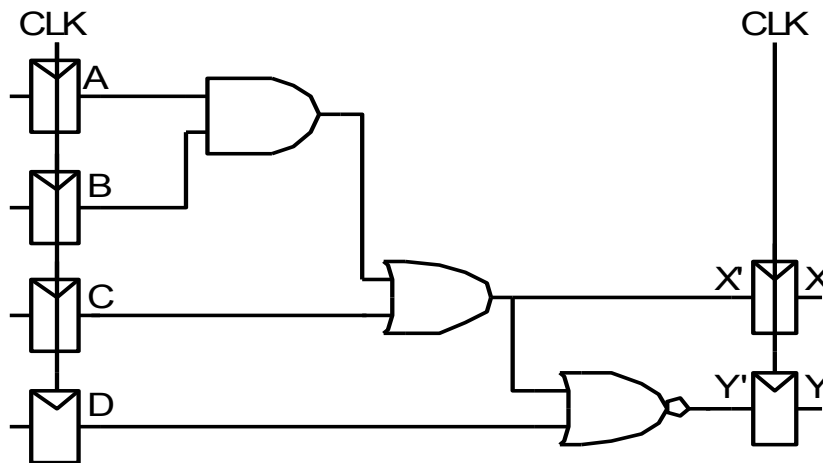
$$t_{cd} = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{pd} > t_{\text{hold}} ?$$

Timing Analysis

Timing Characteristics



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

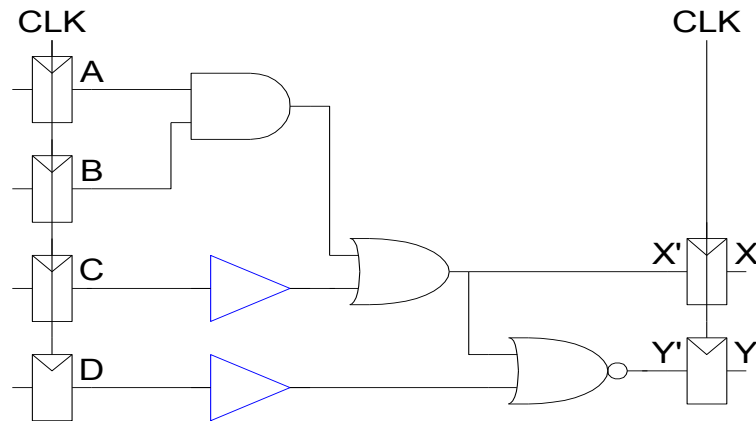
Hold time constraint:

$$t_{ccq} + t_{cd} > t_{\text{hold}} ?$$

$$(30 + 25) \text{ ps} > 70 \text{ ps} ? \text{ No!}$$

Fixing Hold Time Violation

Add buffers to the short paths:



$$t_{pd} =$$

$$t_{cd} =$$

Setup time constraint:

$$T_c \geq$$

$$f_c =$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

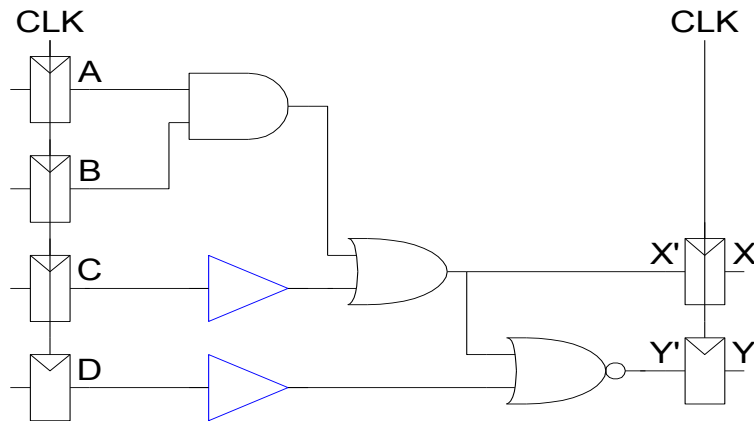
$$t_{cd} = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{pd} > t_{\text{hold}} ?$$

Fixing Hold Time Violation

Add buffers to the short paths:



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 2 \times 25 \text{ ps} = 50 \text{ ps}$$

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

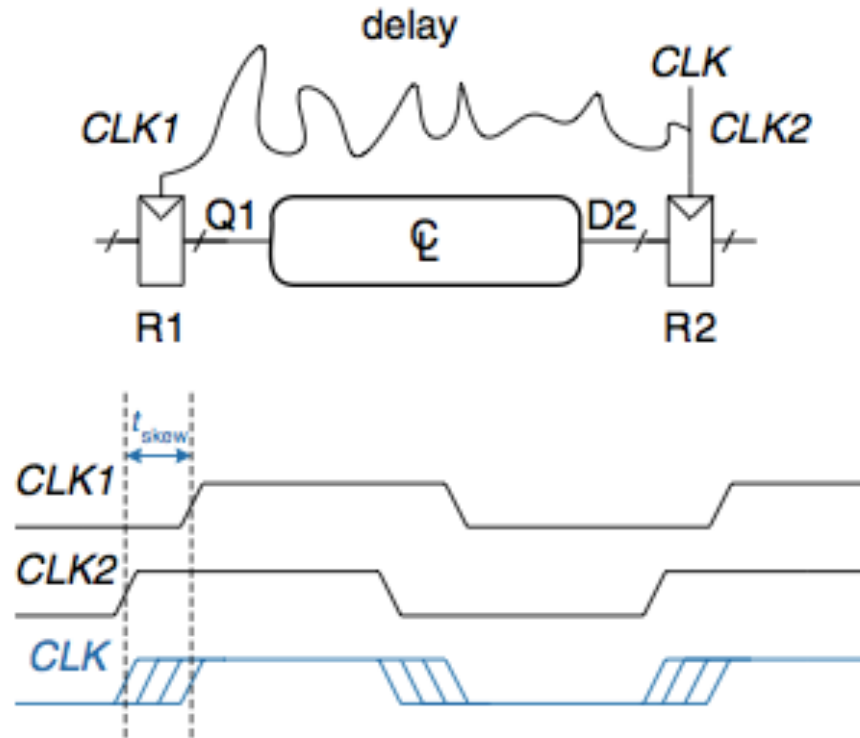
$$t_{cd} = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{\text{hold}} ?$$

$$(30 + 50) \text{ ps} > 70 \text{ ps} ? \text{ Yes!}$$

Clock Skew

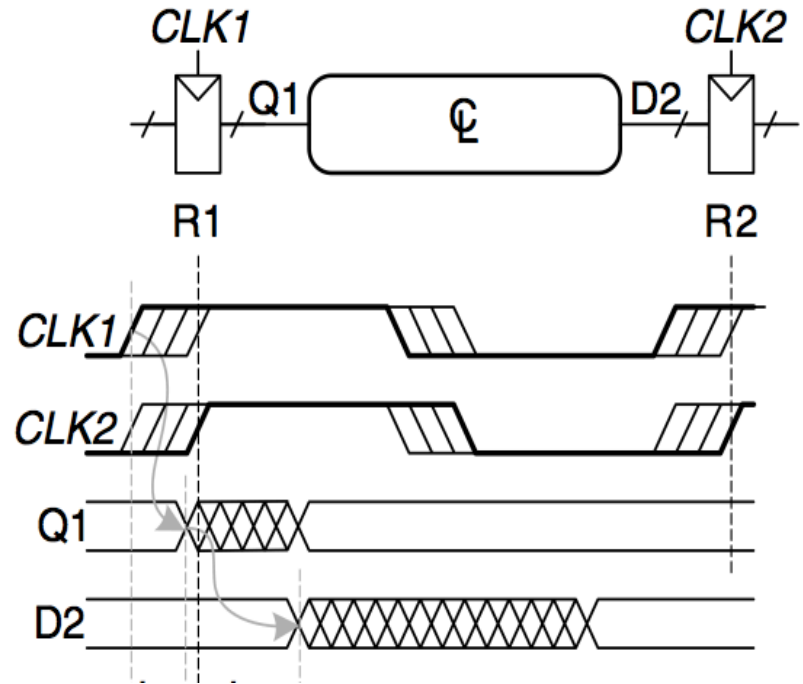


- The clock doesn't arrive at all registers at the same time
- Skew is the difference between two clock edges
- Examine the worst case to guarantee that the dynamic discipline is not violated for any register – many registers in a system!

Setup time constraint

Consider a circuit where the setup constraint is satisfied for R2 when there is no clock skew.

Is the setup constraint guaranteed to be satisfied if the rising edge of CLK2 arrives later than that of CLK1, i.e. CLK 2 is delayed (as shown in the figure ?



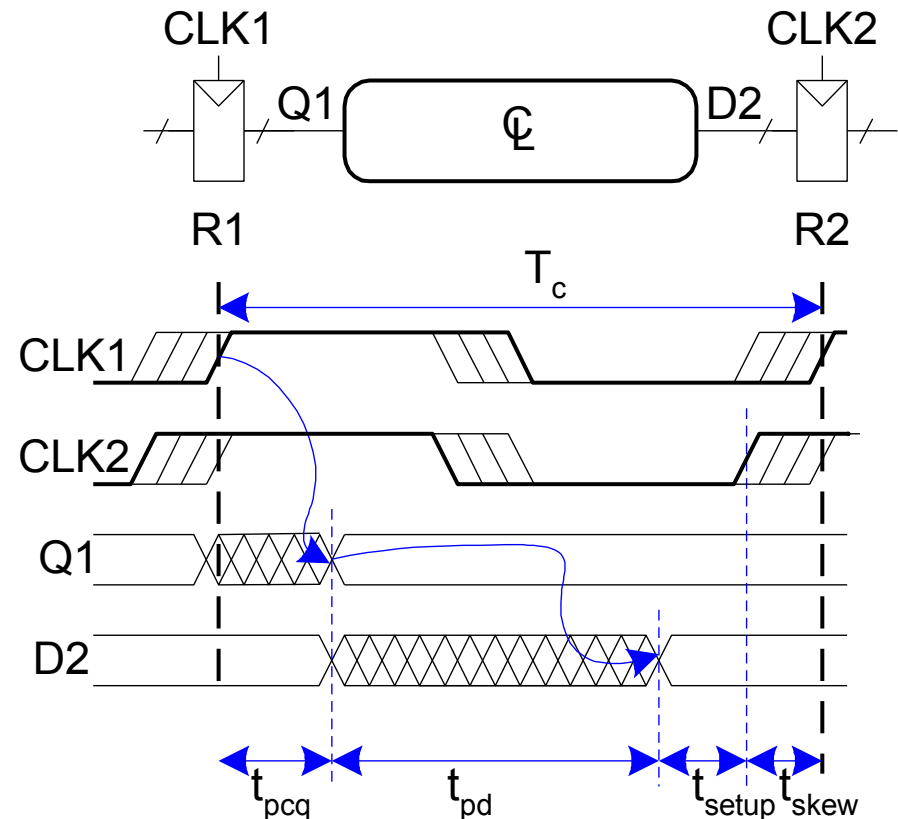
- A. Yes
- B. No

Setup Time Constraint with Clock Skew

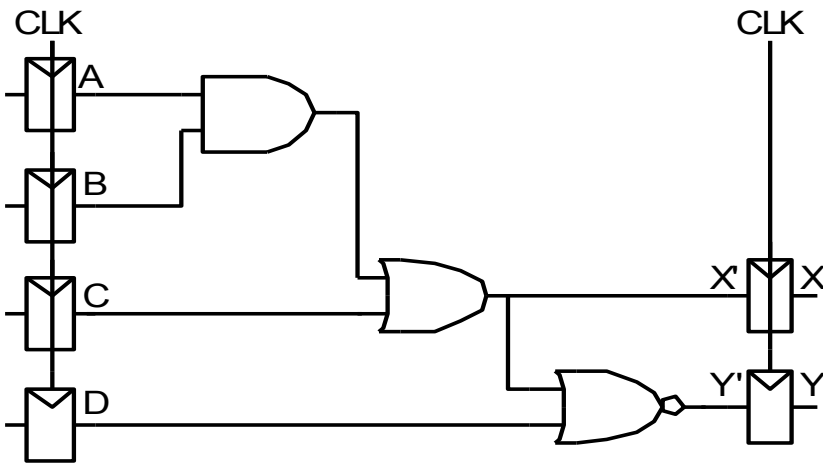
- In the worst case, the CLK2 is earlier than CLK1

$$T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{setup} + t_{skew})$$



Timing Analysis with clock skew



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

What is the minimum allowable clock period given that the clocks are skewed by 50ps

- A. 215ps
- B. 265 ps
- C. None of the above

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

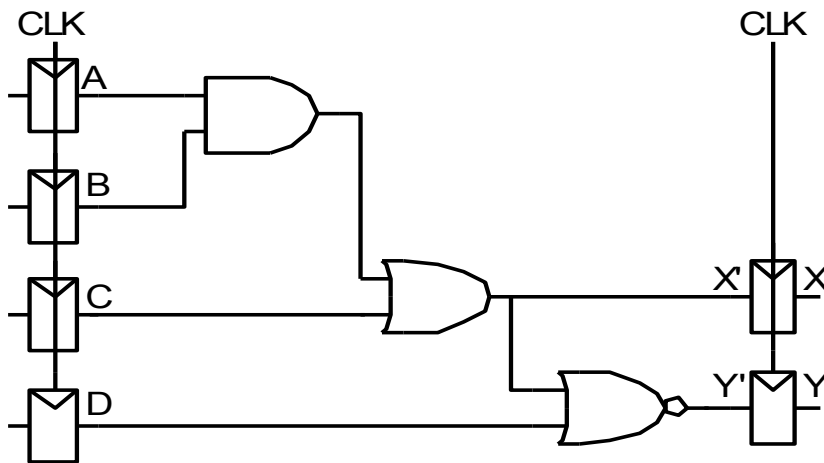
$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

$$t_{\text{skew}} = 50 \text{ ps}$$

Timing Analysis with clock skew



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

$$T_c \geq 265 \text{ ps}$$

$$f_c = 1/T_c = 3.77 \text{ GHz}$$

Without skew we got $f_c = 4.65 \text{ GHz}$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

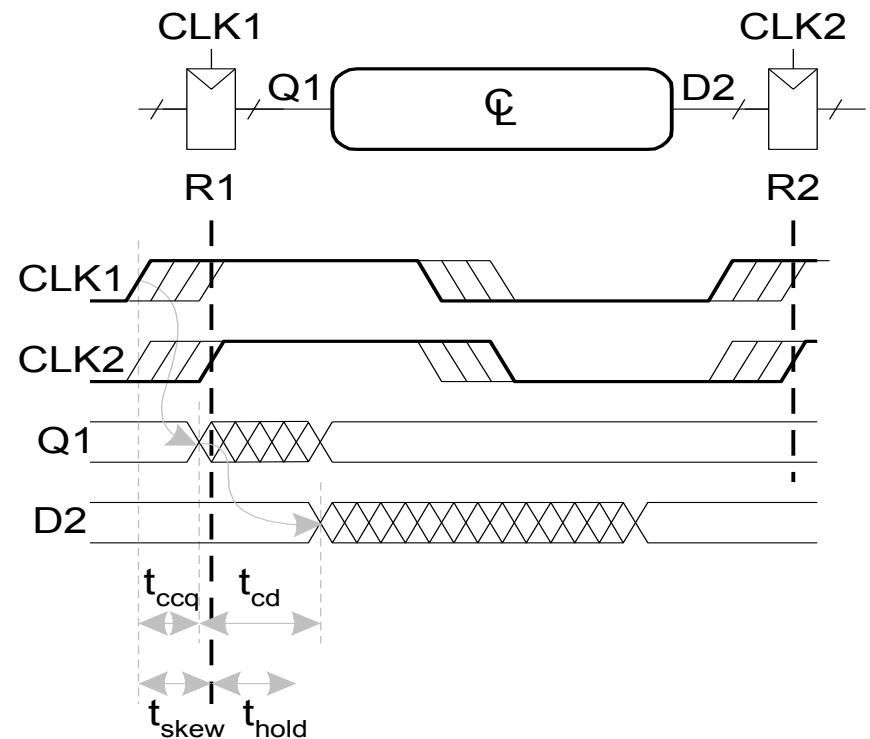
$$t_{\text{skew}} = 50 \text{ ps}$$

Hold Time Constraint with Clock Skew

- In the worst case, CLK2 is later than CLK1

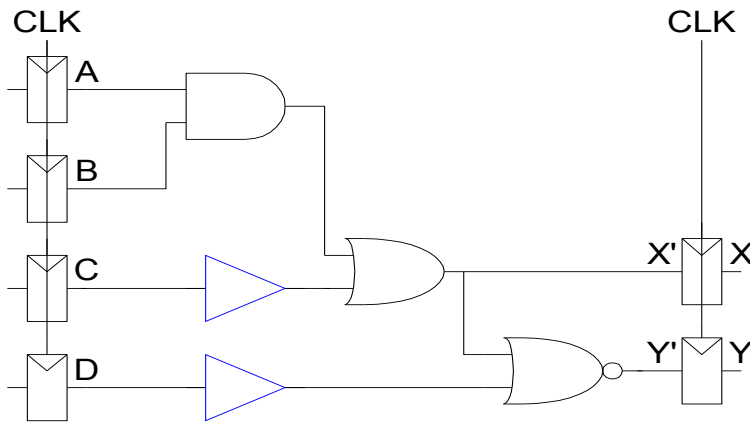
$$t_{ccq} + t_{cd} > t_{hold} + t_{skew}$$

$$t_{cd} > t_{hold} + t_{skew} - t_{ccq}$$



Hold Time Violation

Add buffers to the short paths:



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 2 \times 25 \text{ ps} = 50 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} + t_{skew}?$$

$$(30 + 50) \text{ ps} > (70 \text{ ps} + 50) \text{ ps} ?$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{setup} = 60 \text{ ps}$$

$$t_{hold} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

$$t_{skew} = 50 \text{ ps}$$