

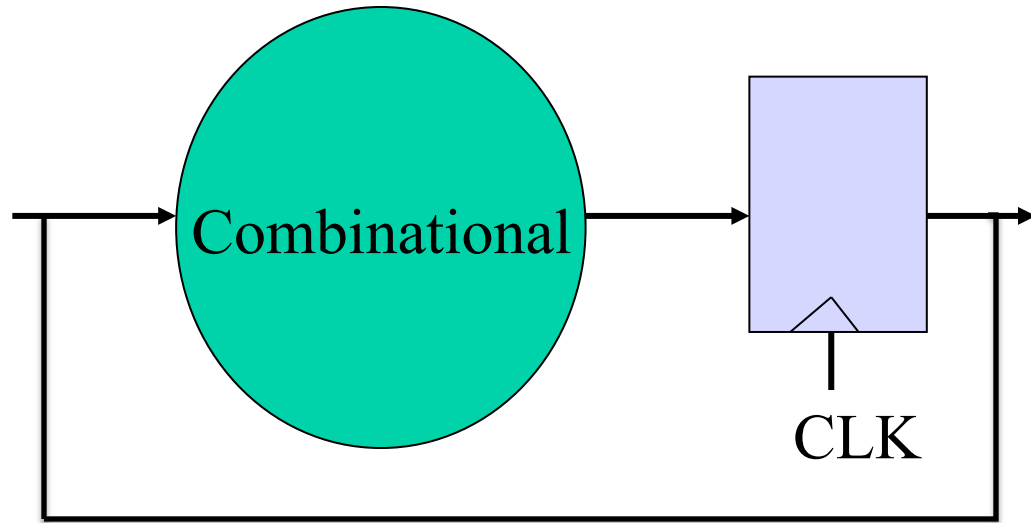
Lecture 17:

Sequential Networks: Timing and Retiming

CSE 140: Components and Design Techniques for
Digital Systems

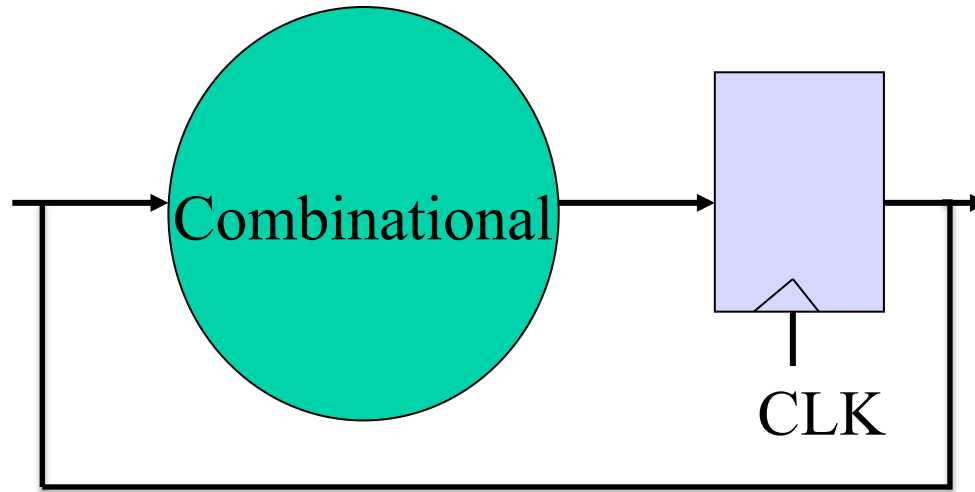
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So far



Logic-level analysis

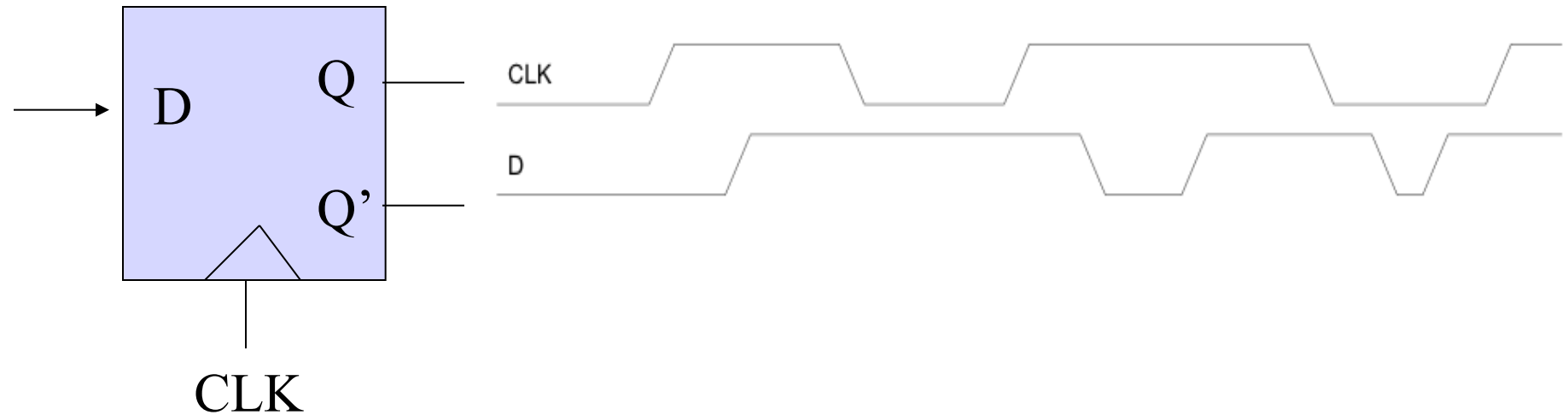
This lecture ...



- Our seemingly logically correct design can go wrong
- How can we design a circuit that works under real constraints?

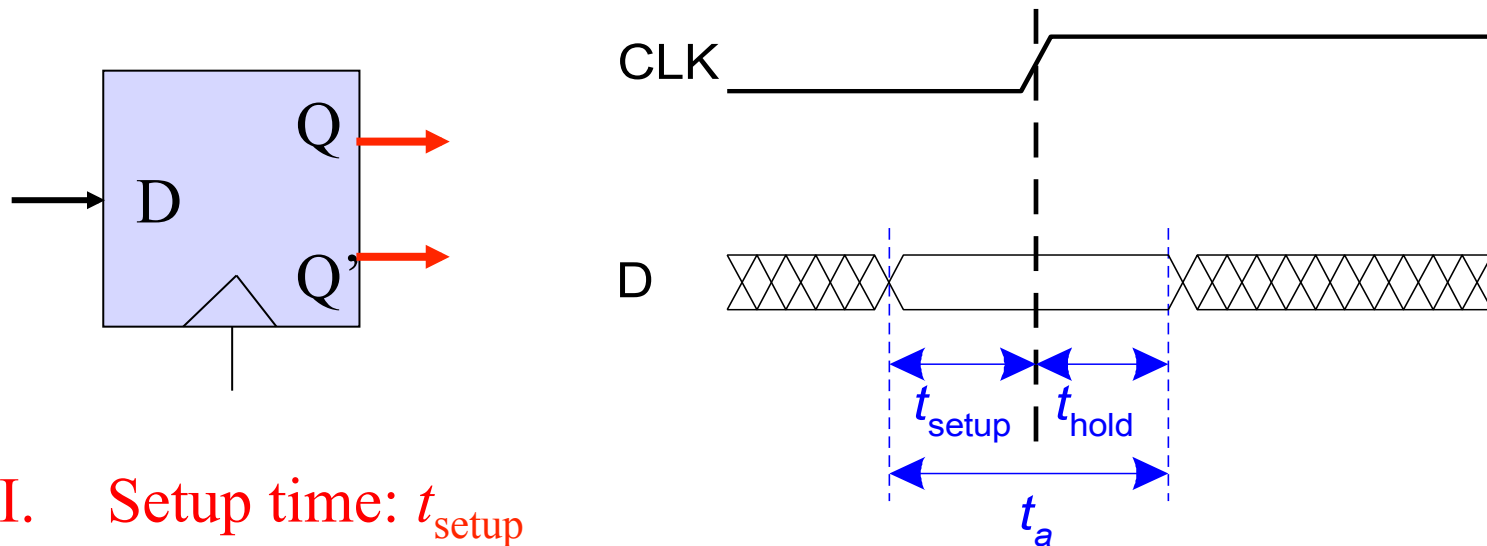
Timing Constraints of flip flops

- What happens if the input to the flip-flop changes just as the clock is transitioning from low to high?



- The input to a flip-flop should be stable for a period of time around the rising edge of the clock

Input Constraints: Set up and hold time



I. Setup time: t_{setup}

Time *before* the clock edge that data must be stable (i.e. not change)

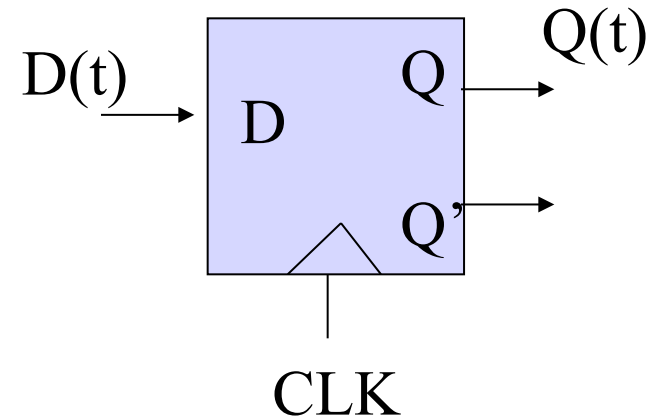
II. Hold time: t_{hold}

Time *after* the clock edge that data must be stable

Aperture time: t_a

Time around clock edge that data must be stable ($t_a = t_{\text{setup}} + t_{\text{hold}}$)

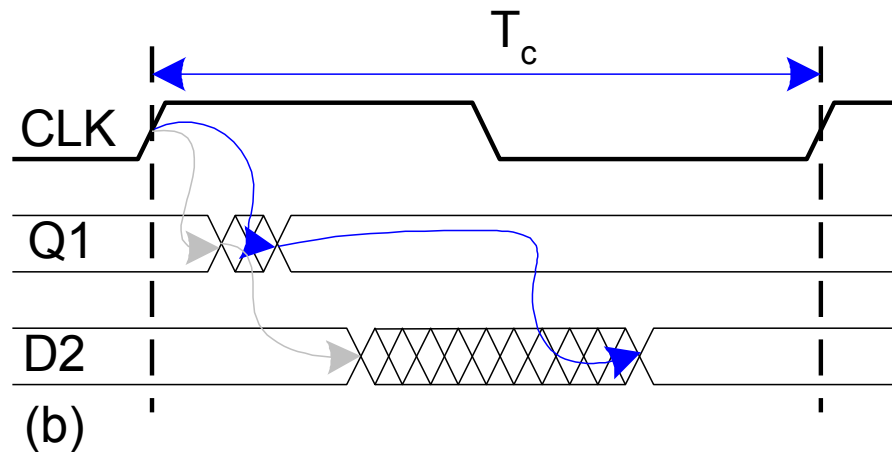
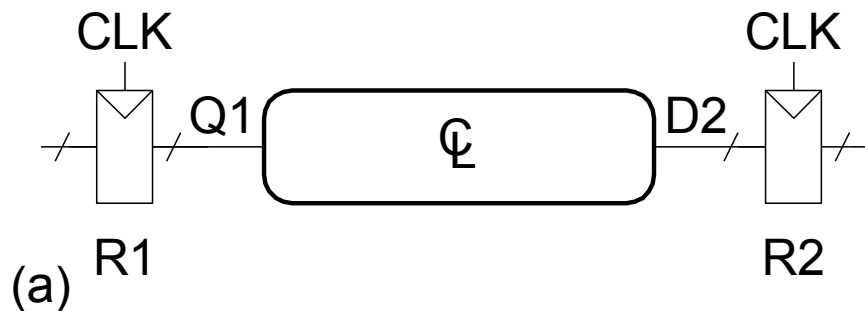
PIQ: The timing of which of the following signals can cause a setup-time violation?



- A. The input signal $D(t)$
- B. The output signal $Q(t)$
- C. Both of the above
- D. None of the above

Why timing in Sequential Circuits can go wrong?

- Input to a flip-flop comes from the output of another flip flop, through a combinational circuit
- The flipflop and combinational circuit have a min and max delay

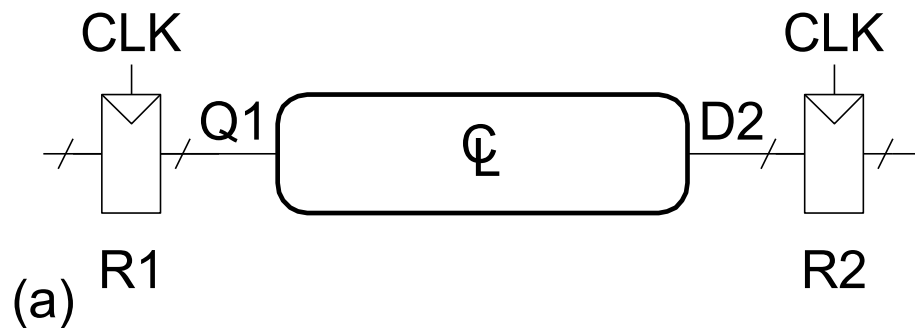


Which of the following violations would occur if the **min** delay of R1 was 0 and the combinational circuit was just a wire?

- A. Hold time violation for R2
- B. Setup violation for R2
- C. Hold time violation for R1
- D. Setup violation for R1
- E. None of the above

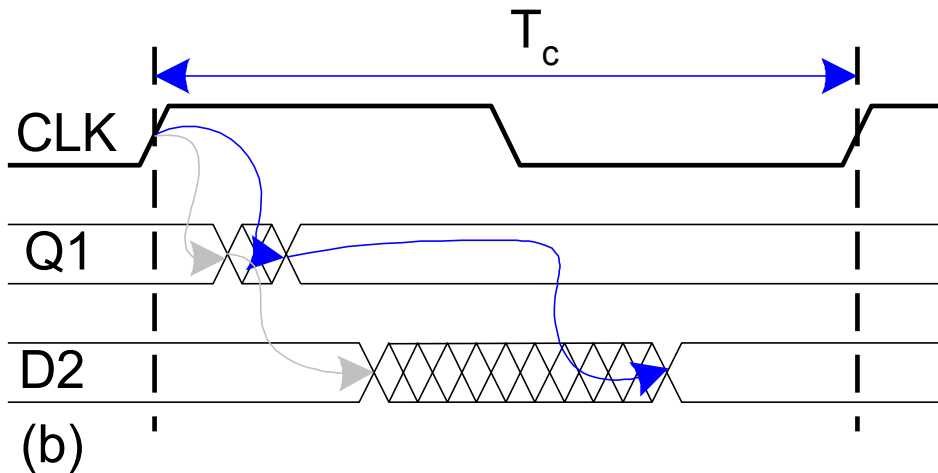
Meeting the hold time constraint

- Input to a flip-flop comes from the output of another flip flop, through a combinational circuit
- The flipflop and combinational circuit have a min and max delay



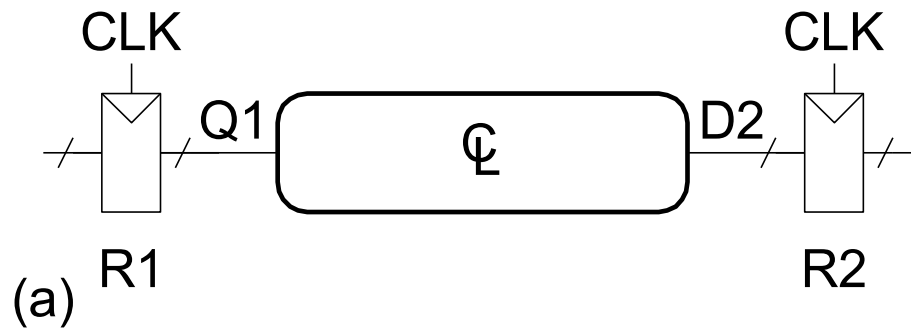
To meet the hold time constraint:

$$t_{\text{hold}} < \text{min delay}(\text{flipflop}) + \text{min delay}(\text{combinational})$$

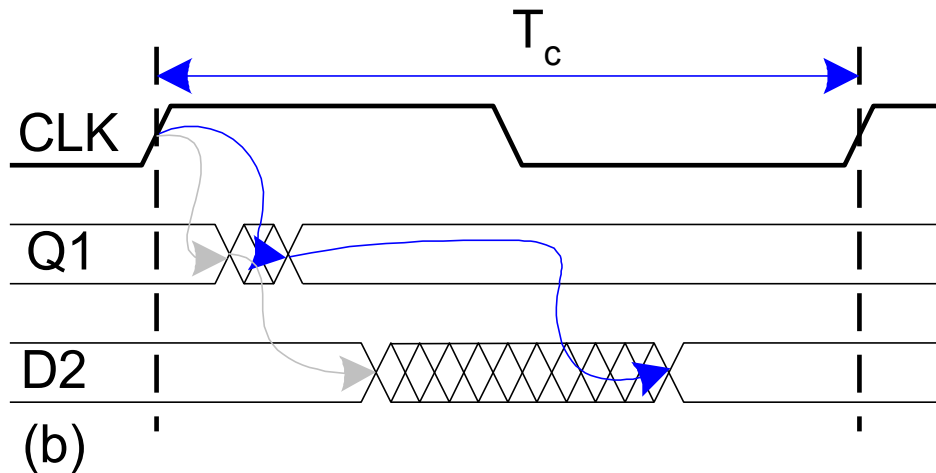


Why timing in Sequential Circuits can go wrong?

- Input to a flip-flop comes from the output of another flip flop, through a combinational circuit
- The flipflop and combinational circuit have a min and max delay



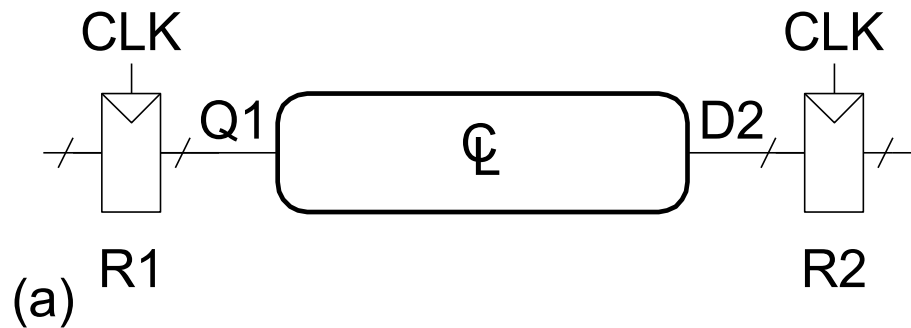
Which of the following violations would occur if the **max** delay of R1 was 0 and the **max** delay of the combinational circuit was equal to the clock period



- A. Hold time violation for R2
- B. Setup violation for R2
- C. Hold time violation for R1
- D. Setup violation for R1
- E. None of the above

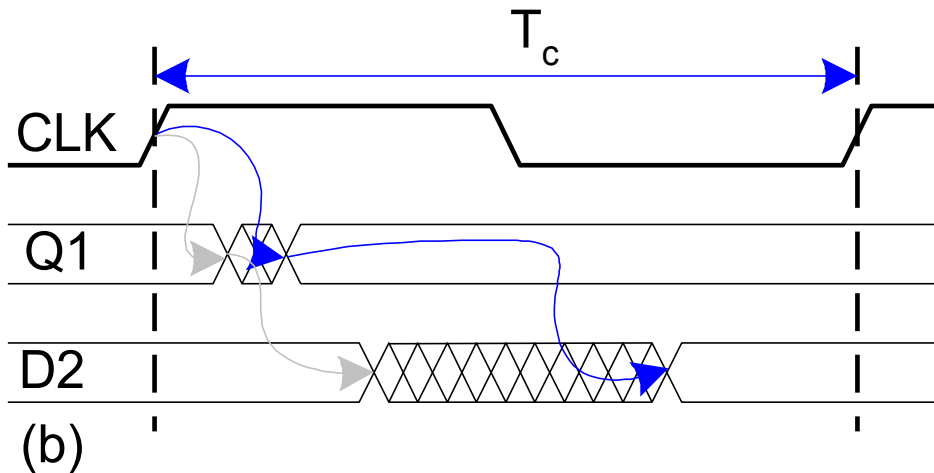
Meeting the setup time constraint

- Input to a flip-flop comes from the output of another flip flop, through a combinational circuit
- The flipflop and combinational circuit have a min and max delay

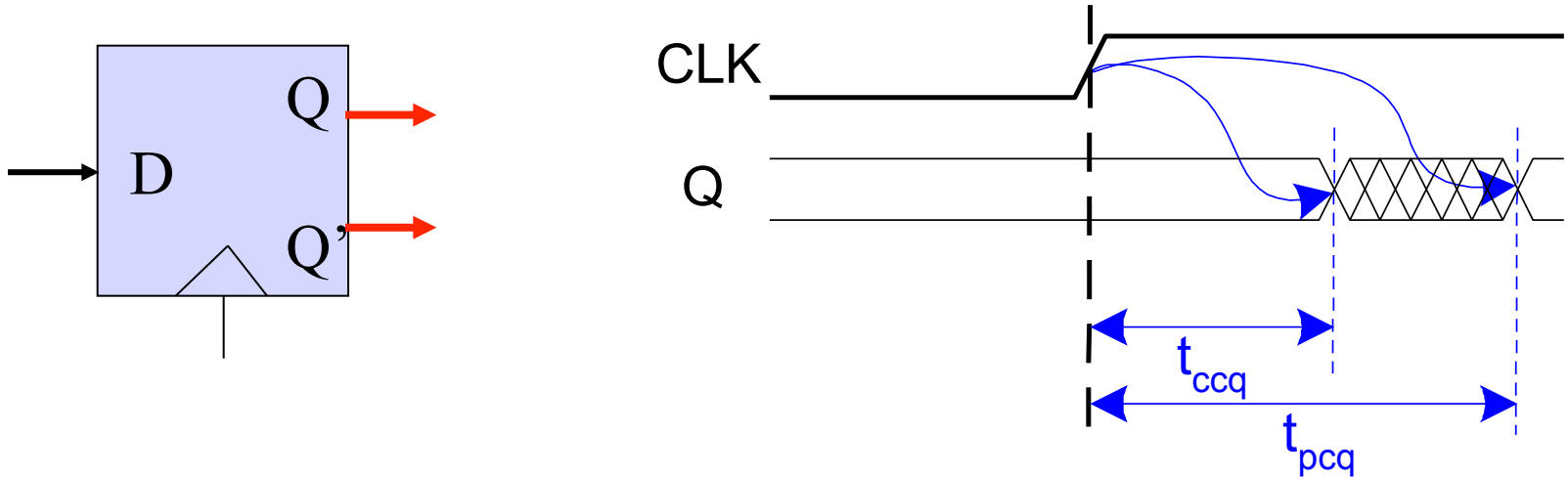


To meet the setup time constraint:

$$T_c \geq \text{max delay(flipflop)} + \text{max delay(combinational)} + t_{\text{setup}}$$

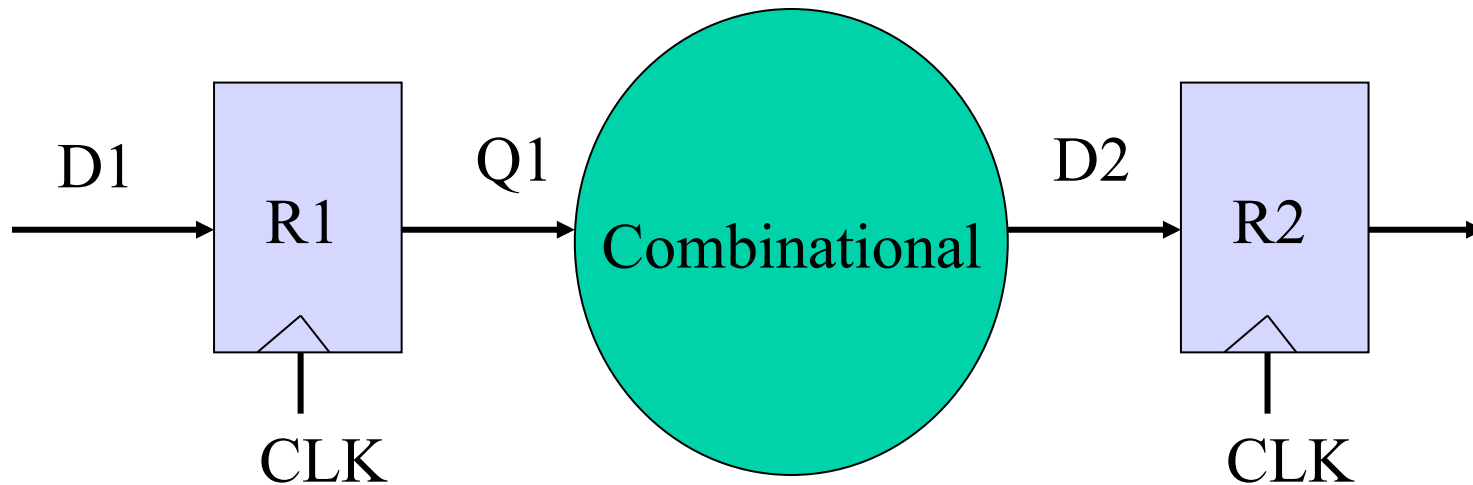


Output Timing Constraints



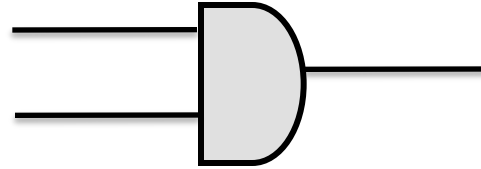
- I. Min delay of flip flop, also called Contamination delay or min CLK to Q delay: t_{ccq}
Time after clock edge that Q might be unstable (i.e., start changing)
- II. Max delay of flip flop, also called Propagation delay or maximum CLK to Q delay: t_{pcq}
Time after clock edge that the output Q is guaranteed to be stable (i.e., to stop changing)

Fact 1: Once a flip flop has been ‘built’ we are stuck with its timing characteristics: t_{setup} , t_{hold} , t_{ccq} , t_{pcq}



Now let's look at the timing characteristics of the combinational part

Combinational Logic Timing



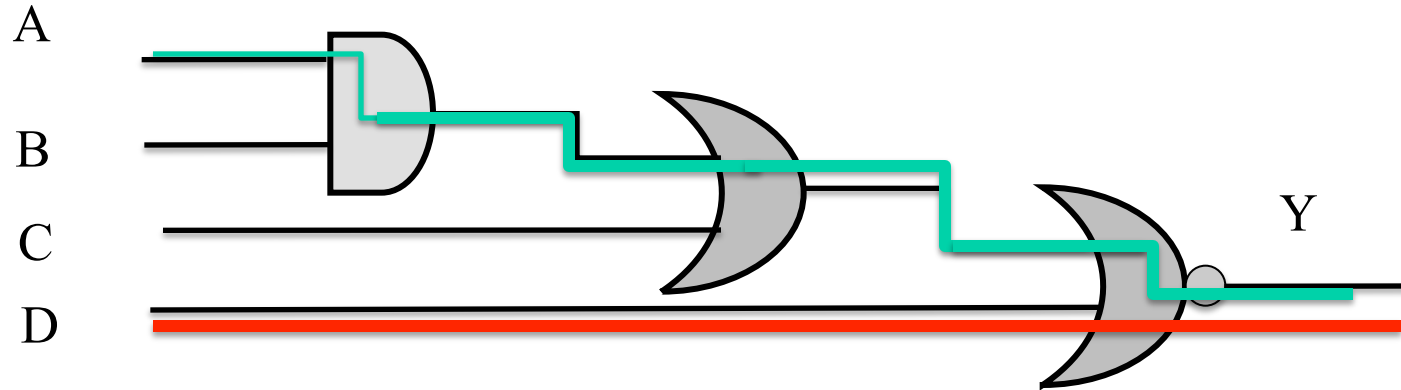
I. Min delay of a gate, also called Contamination delay: t_{cd}

Minimum time from when an input changes until the output *starts* to change

II. Max delay of a gate, also called Propagation delay: t_{pd}

Maximum time from when an input changes until the output *is* guaranteed to reach its final value (i.e., stop changing)

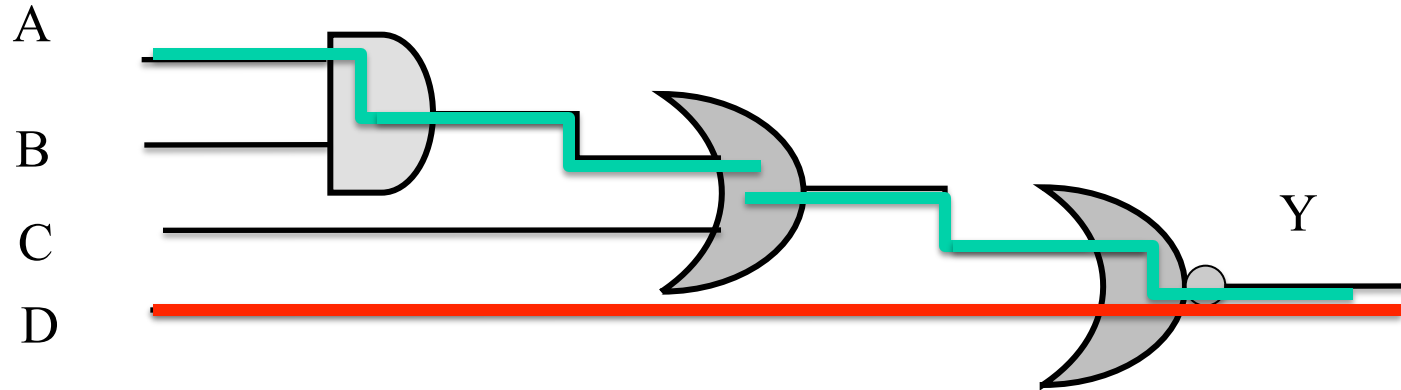
Combinational Logic: Output timing constraints



PI Q: Which path in the above circuit determines the **contamination** delay of the circuit (assuming the delay of all the gates is the same)?

- A. Green path
- B. Red path
- C. Both
- D. Neither

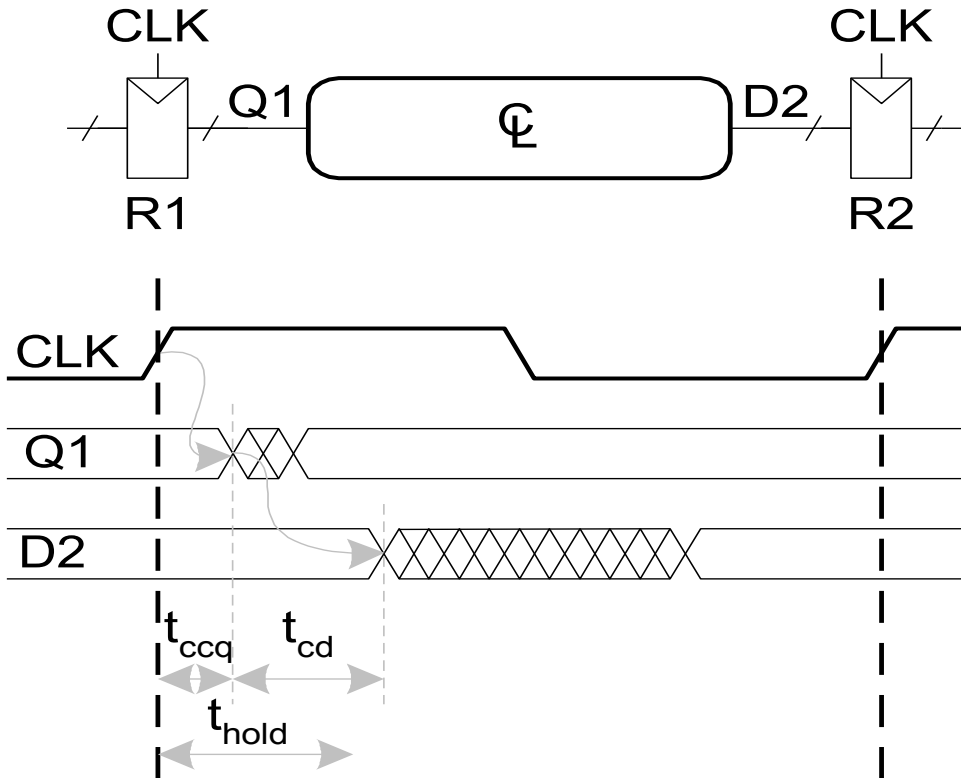
Combinational Logic: Output timing constraints



PI Q: Which path in the above circuit determines the **propagation** delay of the circuit (assuming the delay of all the gates is the same)?

- A. Green path
- B. Red path
- C. Both
- D. Neither

Formalizing the hold time constraint in Sequential Circuits

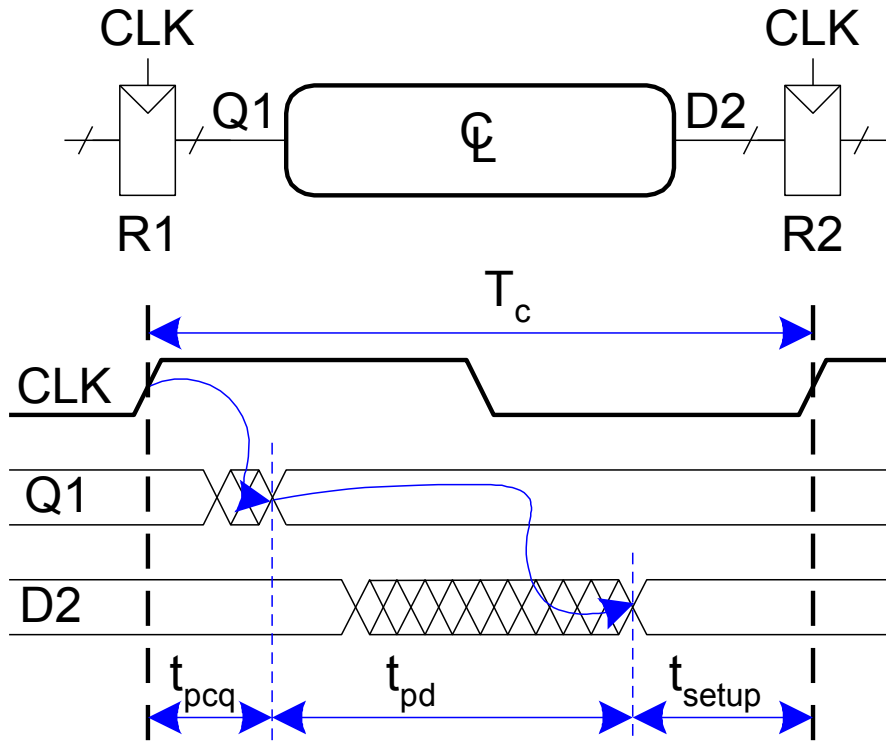


To meet the hold time constraint:

$$t_{\text{hold}} < \text{min delay}(\text{flipflop}) + \text{min delay}(\text{combinational})$$

$$t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}}$$

Formalizing the setup time constraints in Sequential Circuits



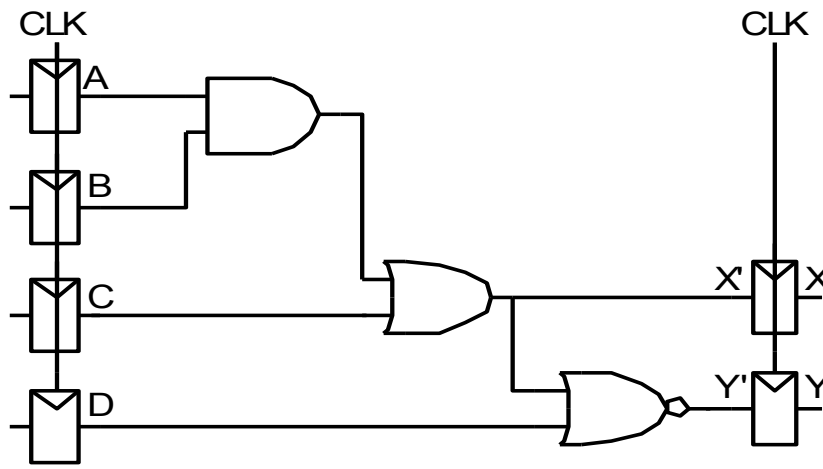
To meet the setup time constraint:

$$T_c \geq \text{max delay(flipflop)} + \text{max delay(combinational)} + t_{\text{setup}}$$

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}}$$

Timing Analysis

Timing Characteristics



$$t_{pd} =$$

$$t_{cd} =$$

Setup time constraint:

$$T_c \geq$$

$$f_c = 1/T_c =$$

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

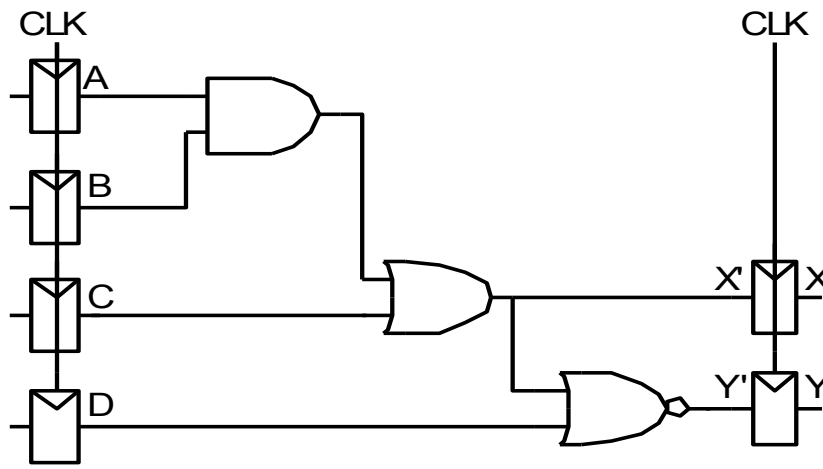
$$t_{cd} = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{pd} > t_{\text{hold}} ?$$

Timing Analysis

Timing Characteristics



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

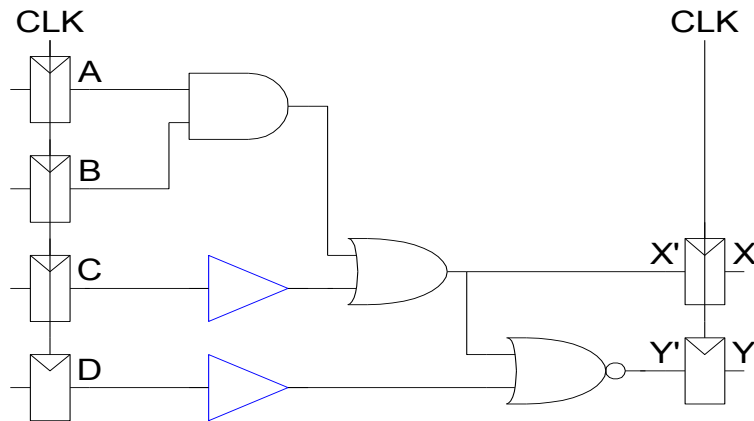
Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} ?$$

$(30 + 25) \text{ ps} > 70 \text{ ps}$? No!

Fixing Hold Time Violation

Add buffers to the short paths:



$$t_{pd} =$$

$$t_{cd} =$$

Setup time constraint:

$$T_c \geq$$

$$f_c =$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

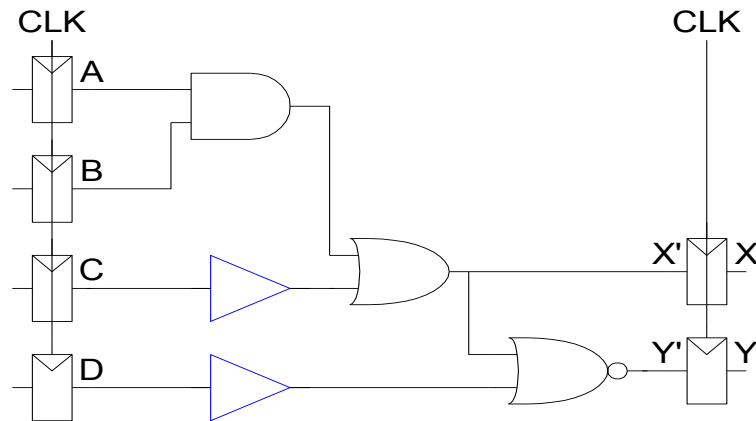
$$t_{cd} = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{pd} > t_{\text{hold}} ?$$

Fixing Hold Time Violation

Add buffers to the short paths:



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 2 \times 25 \text{ ps} = 50 \text{ ps}$$

Setup time constraint:

$$T_c \geq (50 + 105 + 60) \text{ ps} = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{\text{hold}} ?$$

$$(30 + 50) \text{ ps} > 70 \text{ ps} ? \text{ Yes!}$$