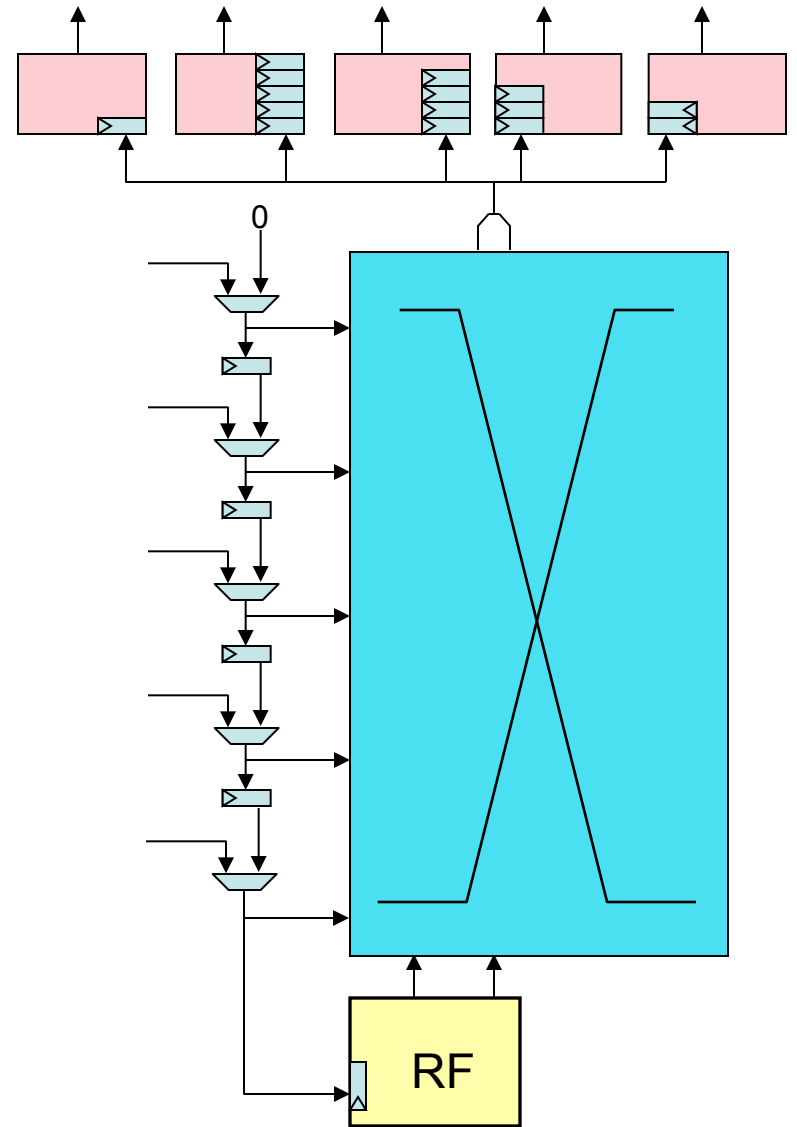


CSE 240A:

Principles of Computer Architecture

Professor: Michael Taylor

UCSD Department of
Computer Science & Engineering

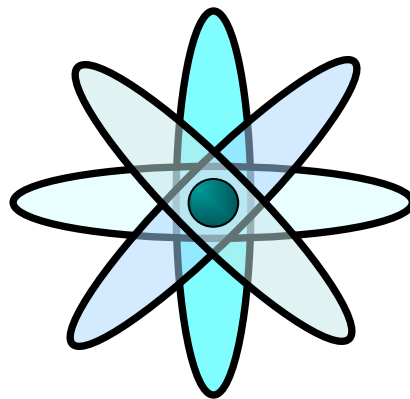
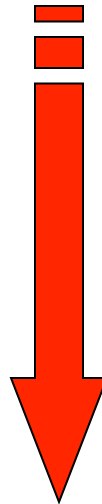


<http://www.cse.ucsd.edu/classes/fa10/cse240a/>

Computer Architecture from 10,000 feet

```
foo(int x)  
{ .. }
```

Class of
application



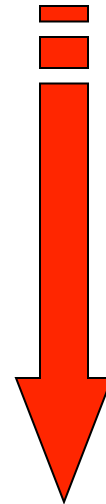
Physics

Computer Architecture from 10,000 feet

```
foo(int x)  
{ .. }
```

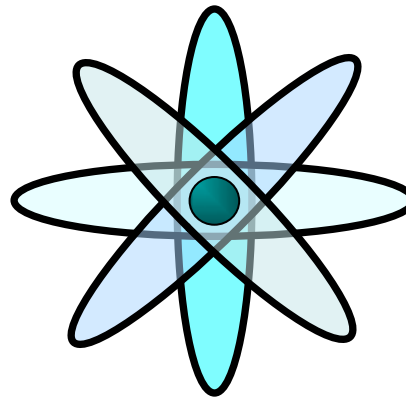
Class of
application

An impossibly
large gap!



In the olden days:

"In 1942, just after the United States entered World War II, hundreds of women were employed around the country as computers..." (source: IEEE)



Physics

The Great Battles in Computer Architecture Are About How to Refine the Abstraction Layers

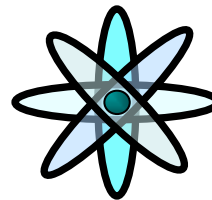
```
foo(int x) { .. }
```

Computation

Language
Compiler
ISA
Micro Architecture
Register-Transfer Level
Circuits
Devices
Materials Science

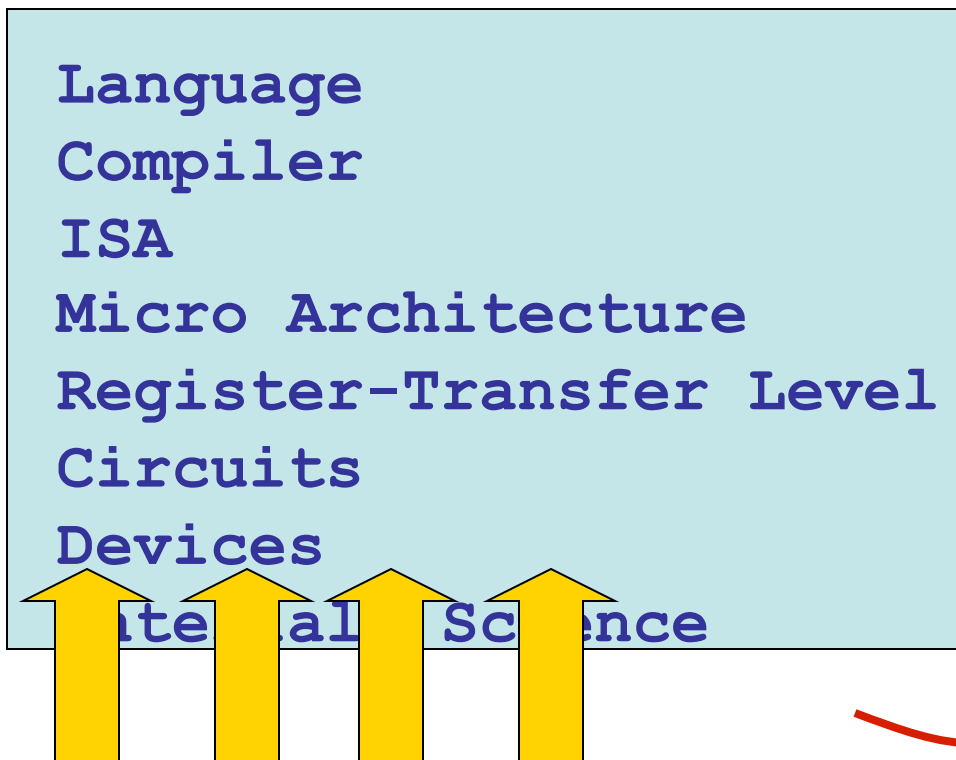
Fortran
IBM 360, VLIW
RISC, T'meta
Superscalar, caches
Mead & Conway

Physics



Abstractions protect us from change
-- but must also change as the world changes

Computation



Changes in fabrication
capabilities

Slower Wires!
Denser VLSI gates!
More pins!
More Power/cm²!

Abstraction Layers - reflected in organization of research communities

Computation

Language
Compiler
ISA
Micro Architecture
Reg-Transfer Level
Circuits
Devices
Materials Science

International Symposium
on Computer Architecture (ISCA)

High Performance
Computer Architecture (HPCA)

Architectural Support for
Programming Languages and OS
(ASPLOS)

International Symposium on
Microarchitecture (MICRO)

Design Automation Conference (DAC)
Int. Conf. Computer Aided Design
(ICCAD)

International Solid State Circuit Conference
(ISSCC)

International Electron Devices Meeting (IEDM)

Physics

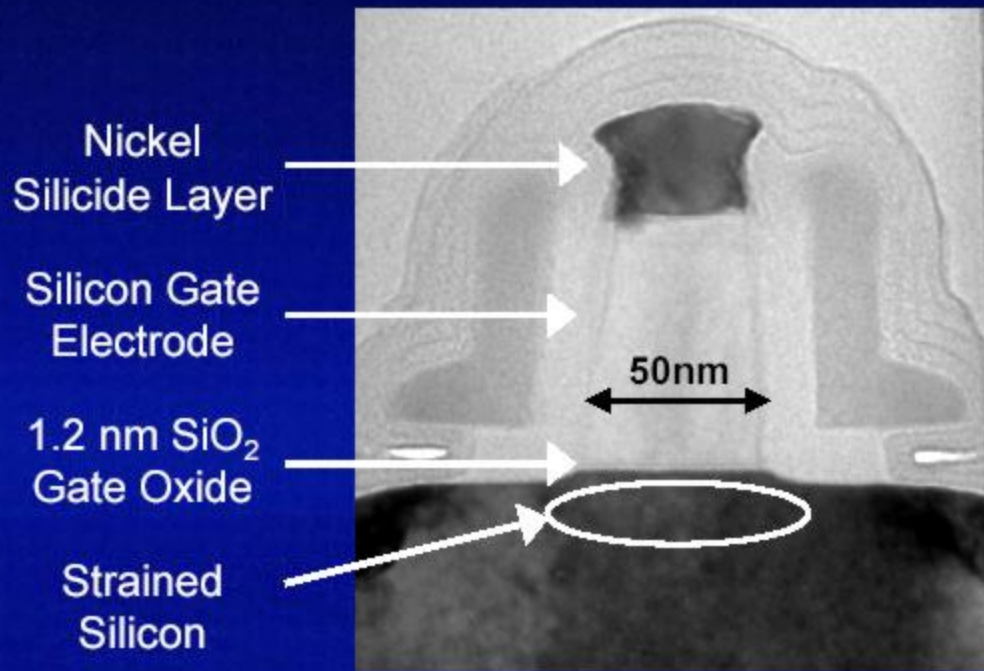
48C 4W	49C 4W	50C 5W	50C 6W	51C 6W	52C 7W	53C 7W	54C 7W	55C 8W	56C 8W	57C 9W	58C 9W	59C 10W	60C 10W	61C 10W	63C 11W	61C
39C 2W	39C 3W	40C 3W	41C 4W	42C 4W	42C 4W	43C 5W	44C 5W	45C 5W	45C 5W	46C 6W	47C 6W	47C 7W	48C	49C	Failed	
32C 2W	33C 2W	33C 3W	35C 3W	35C 3W	36C 3W	36C 4W	37C 4W	37C 4W	38C 4W	38C 4W	39C	39C	Failed			
28C 2W	28C 2W	29C 2W	29C 2W	30C 2W	30C 3W	30C 3W	31C 3W	31C 3W	31C 3W	32C	Failed					
25C 1W	26C 1W	26C 1W	26C 2W	27C 2W	27C 2W	27C	Failed									
2	2.2	2.4	2.6	2.8	3	3.2	3.4	3.6	3.8	4	4.2	4.4	4.6	4.8	5	5.2
Freq (GHz)																

48C 4W	49C 4W	50C 5W	50C 6W	51C 6W	52C 7W	53C 7W	54C 7W	55C 8W	56C 8W	57C 9W	58C 9W	59C 10W	60C 10W	61C 10W	63C 11W	61C	
39C 2W	39C 3W	40C 3W	41C 4W	42C 4W	42C 4W	43C 5W	44C 5W	45C 5W	45C 5W	46C 6W	47C 6W	47C 7W	48C	49C	Failed		
32C 2W	33C 2W	33C 3W	35C 3W	35C 3W	36C 3W	36C 4W	37C 4W	37C 4W	38C 4W	38C 4W	39C	39C					
28C 2W	28C 2W	29C 2W	29C 2W	30C 2W	30C 3W	30C 3W	31C 3W	31C 3W	31C 3W	32C							
25C 1W	26C 1W	26C 1W	26C 2W	27C 2W	27C 2W	27C											
2	2.2	2.4	2.6	2.8	3	3.2	3.4	3.6	3.8	4	4.2	4.4	4.6	4.8	5	5.2	
Freq (GHz)																	

Classic Int. Electron Device Meeting (IEDM)

Paper: How we designed a single transistor

90 nm Generation Transistor



No other company combines these transistor features at the 90 nm generation

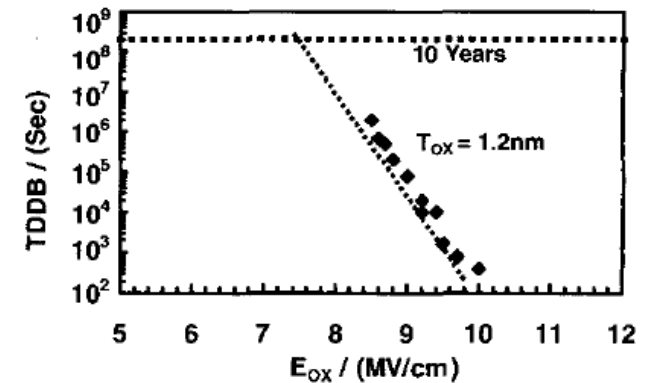


Figure 11: 1.2 nm gate oxide time to fail vs. electric field.

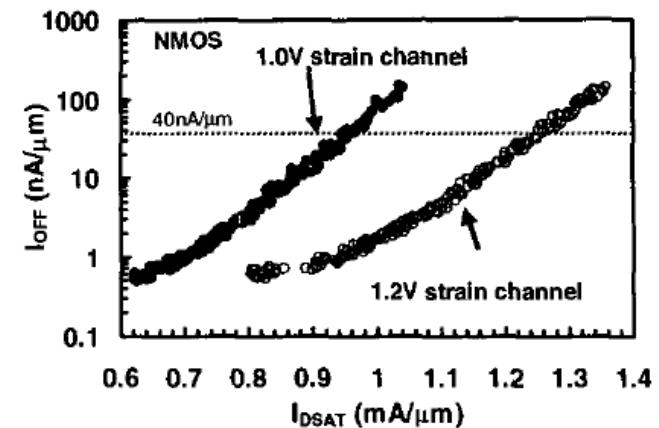
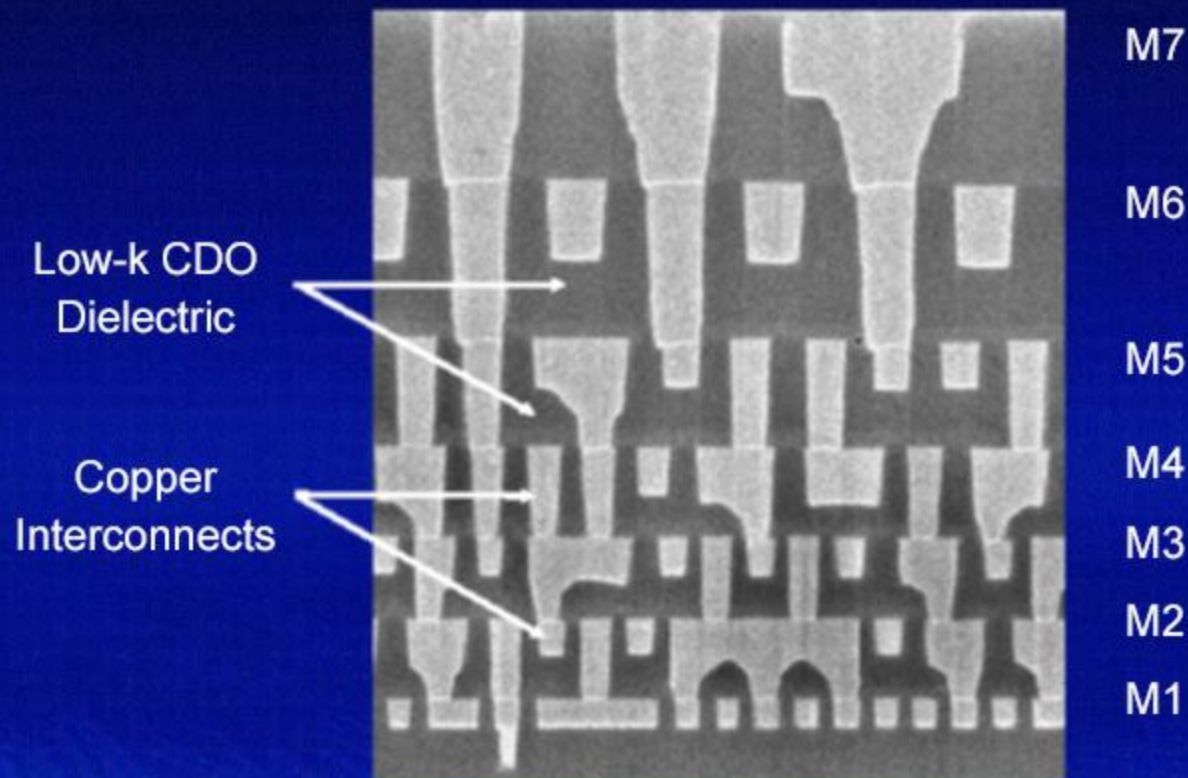


Figure 6: NMOS I_{ON} vs. I_{OFF} at 1.0V and 1.2V.

Classic Int. Electron Device Meeting (IEDM)

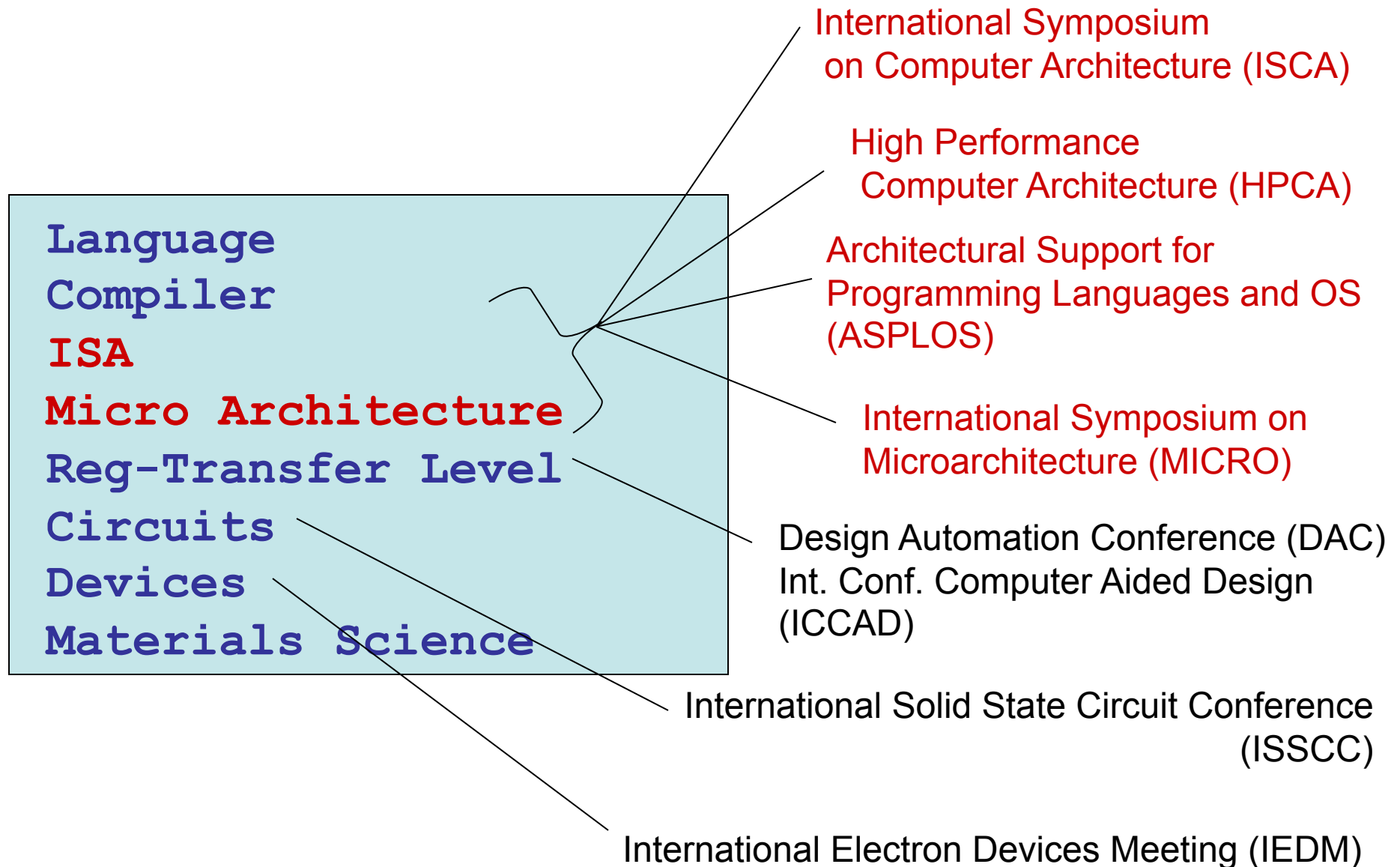
Paper: "How we designed a *wire*"

90 nm Generation Interconnects



Combination of copper + low-k dielectric now meeting performance and manufacturing goals

The focus of this class



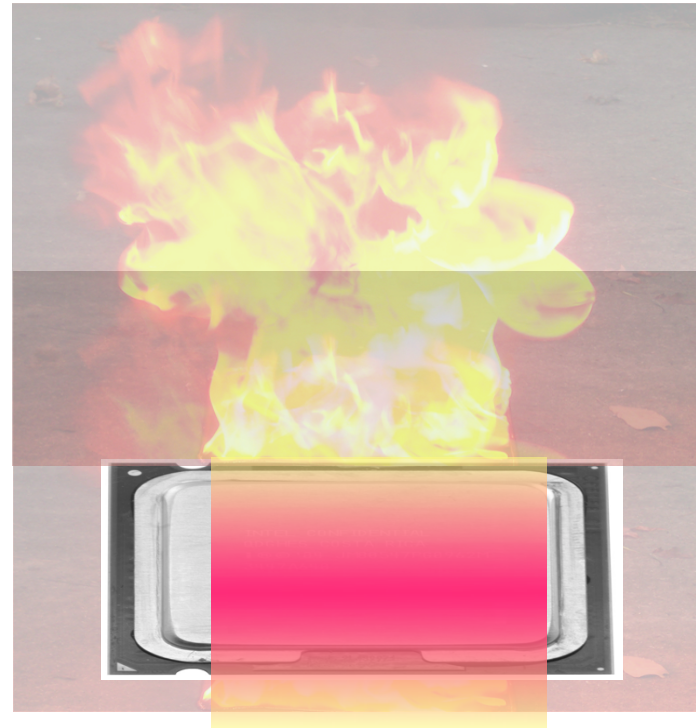
Change: Power

Santa Clara, we have a problem

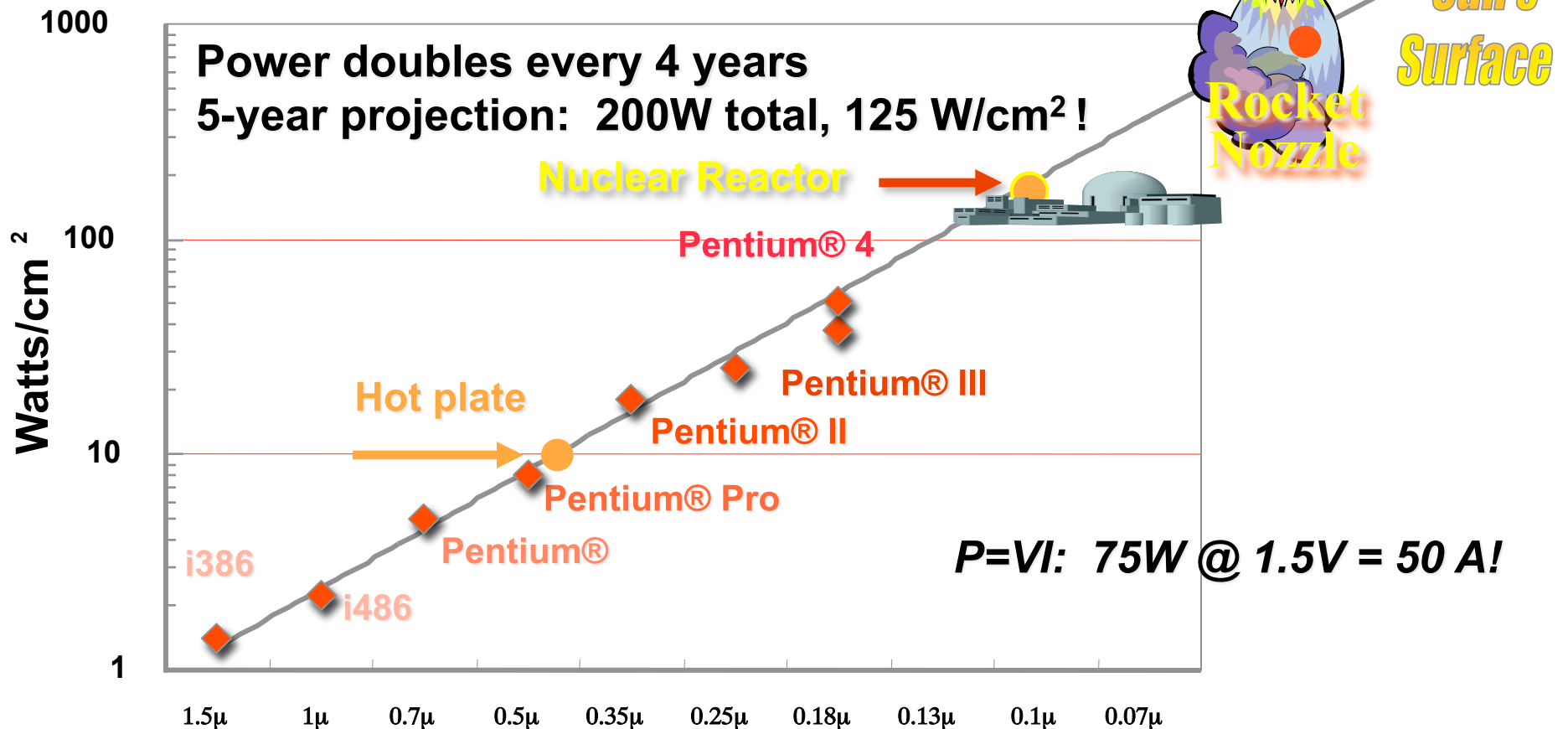
More pipeline stages,
less efficient, more power.

Just can't remove
> 100 watts
without great expense on
a desktop.

All computing is now
Low Power Computing!

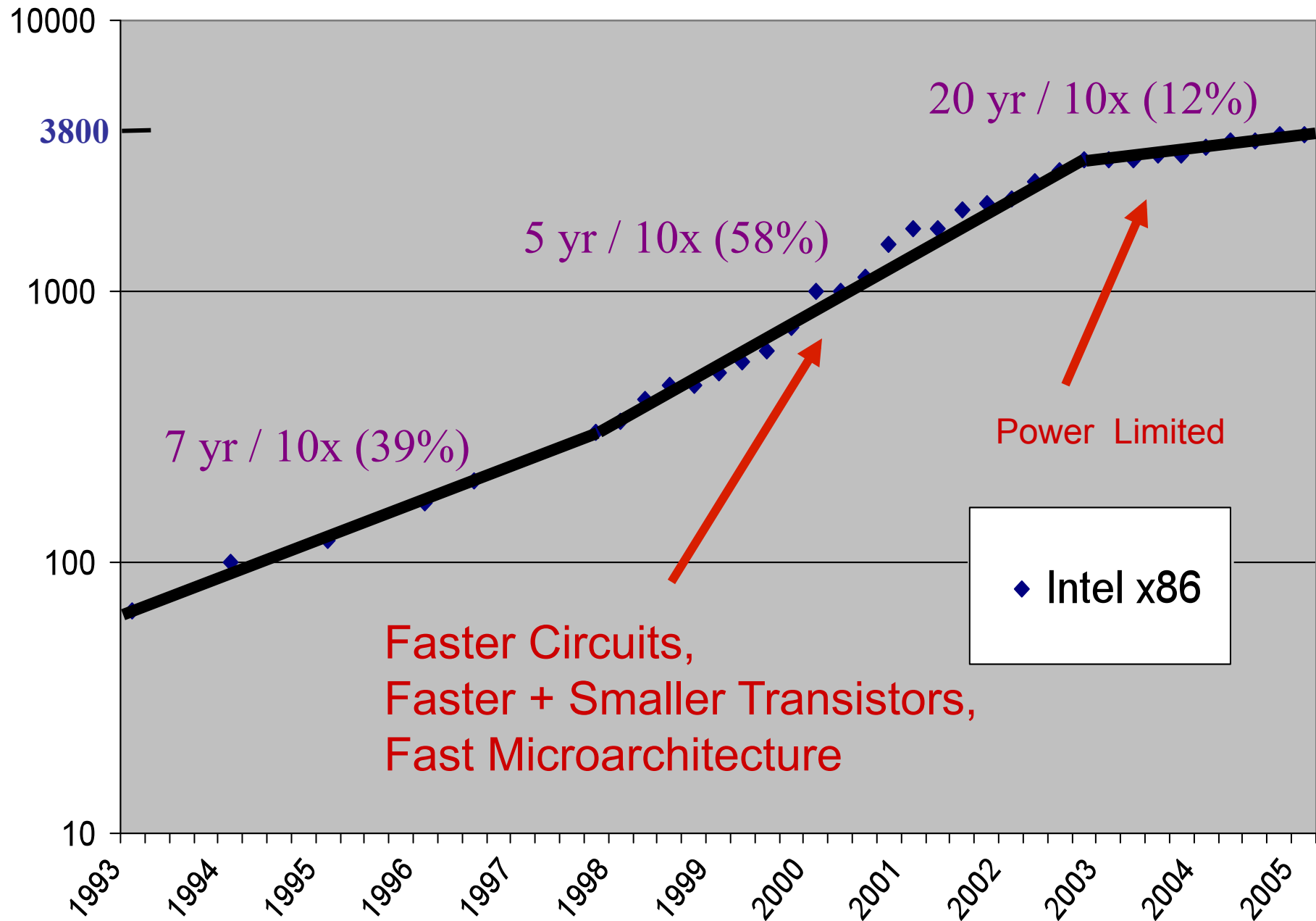


Power Density



From "New Microarchitecture Challenges in the Coming Generations of CMOS Process Technologies"
 – Fred Pollack, Intel Corp. Micro32 conference key note - 1999.

Change: microprocessor frequency versus time



Intel

P3: 12 stages

P4 (b4 paper): 20 stages

P4/prescott: 31 stages

~~**P5/Tejas: >> 31 stages**~~

Intel

P3: 12 stages

P4 (b4 paper): 20 stages

~~**P4/prescott: 31 stages**~~

~~**P5/Tejas: >> 31 stages**~~

Intel

P3: 12 stages

~~**P4 (b4 paper): 20 stages**~~

~~**P4/prescott: 31 stages**~~

~~**P5/Tejas: >> 31 stages**~~

Back to the future

P3:

12 stages

~~P4 (b4 paper):~~

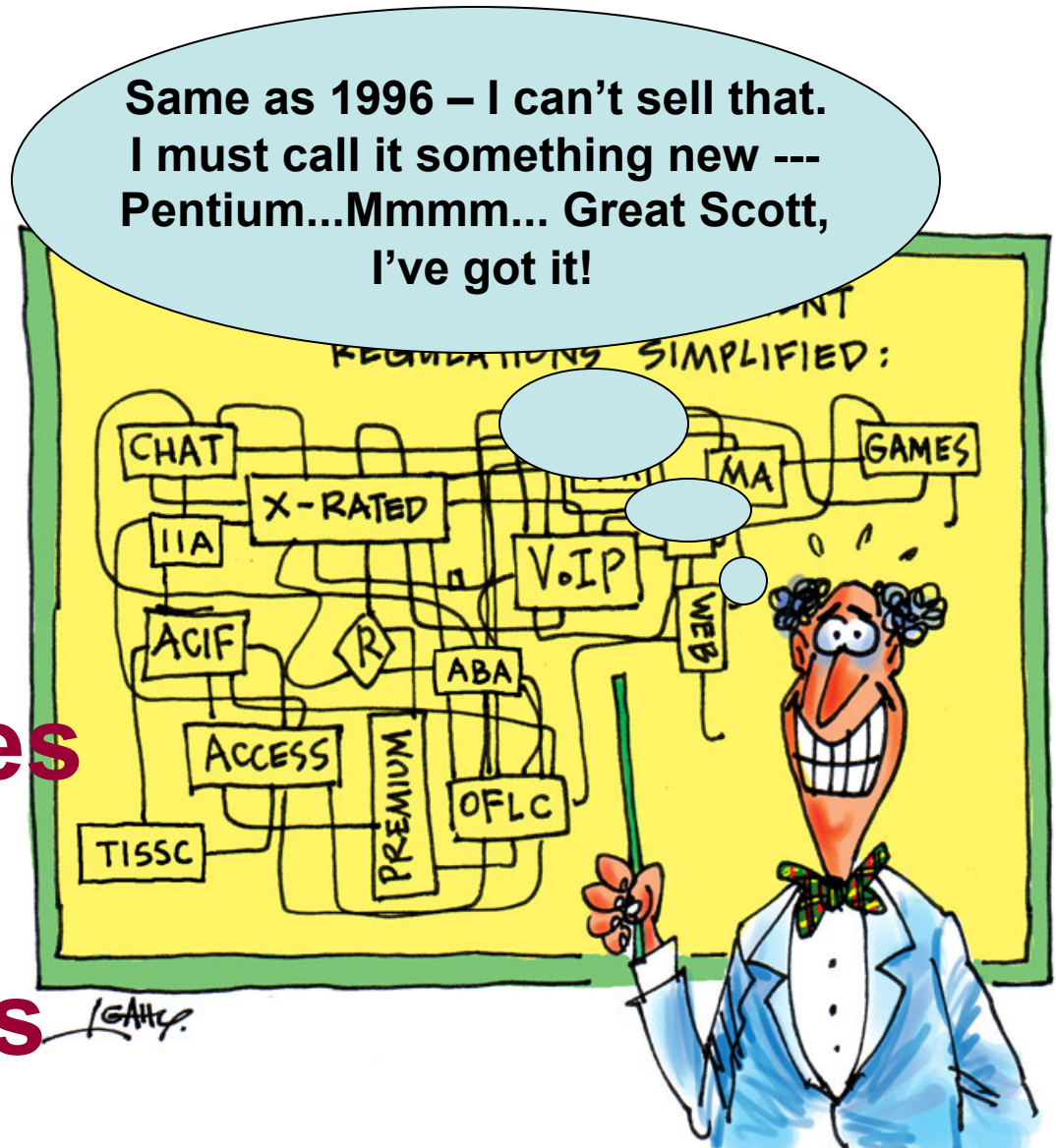
~~20 stages~~

~~P4/prescott:~~

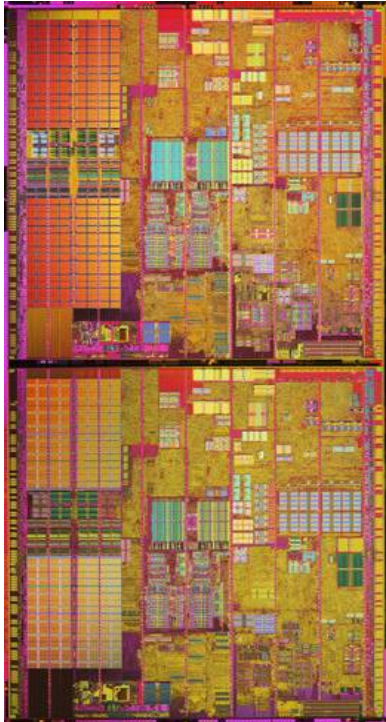
~~31 stages~~

~~P5/Tejas:~~

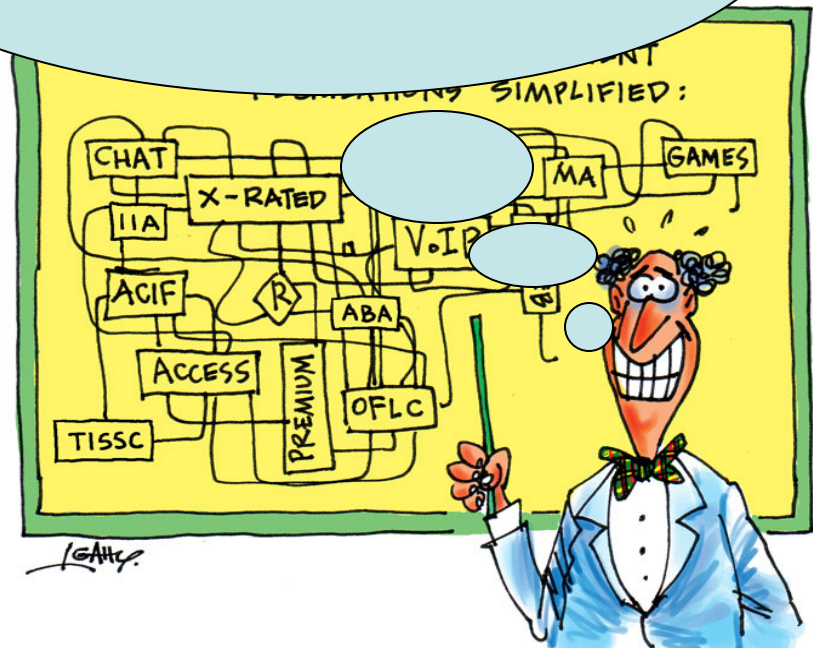
~~>> 31 stages~~



And forward to multi-core



Intel Core Duo



Future outlook

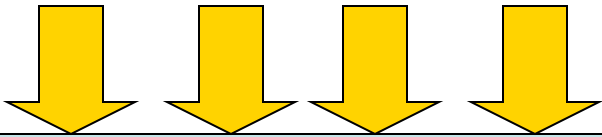
Old Trend: Frequency

New Trend: Parallel processing

→ Processors stuck at 3.8 GHz. Intel and others are pushing multi-core instead

Abstractions protect us from change
-- but must also change as the world changes

Changes in application space



Language
Compiler
ISA
Micro Architecture
Register-Transfer Level
Circuits
Devices
Materials Science

Physics

Virtual Homicide (Quake)

Photographic memory

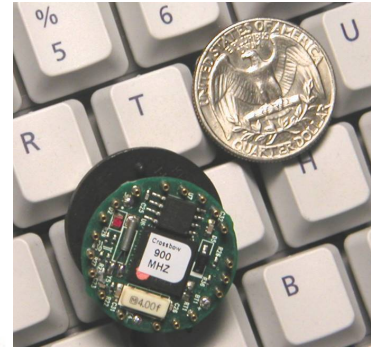
Telepathic

Mathematical Genius

Etc...

And on that note: PC's are not the only important class of computer - in fact they are in the minority (~2%)!

Google™



745i



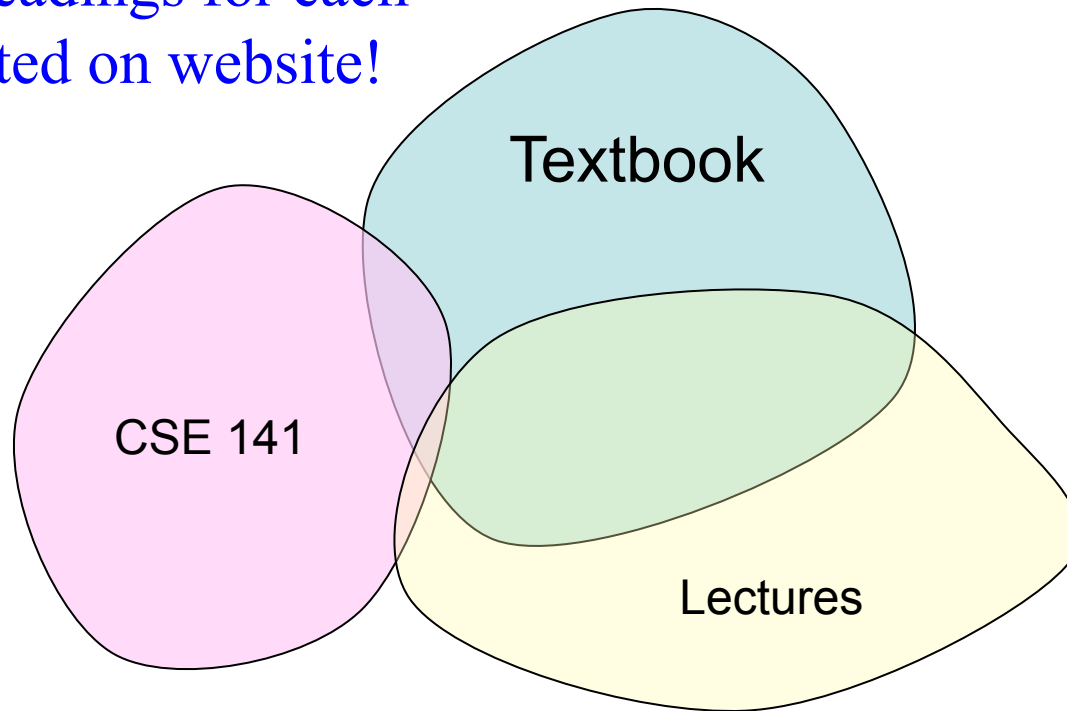
Course Work and Grading

- *See website!*

<http://www-cse.ucsd.edu/classes/fa10/cse240a/>

Text vs. Lectures vs. CSE 141

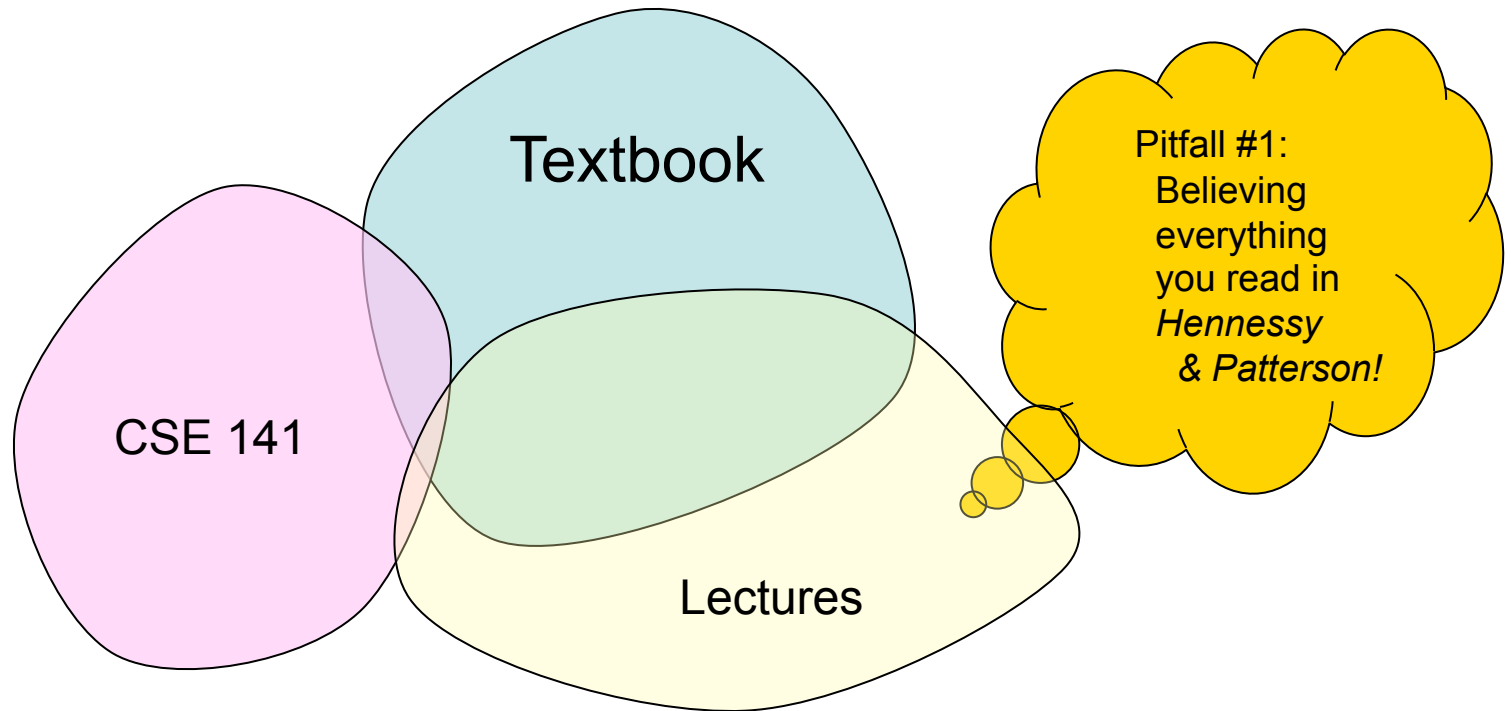
Assigned readings for each
lecture posted on website!



- Lectures will include material not in the text...text will include material not in the lectures. (Midterms and homework will give you an opportunity to calibrate what you need to know.)

- Resource limitations prevent us from addressing material from the prerequisite, CSE 141, in office hours...but we are happy to refer you to the book or your classmates.

Text vs. Lectures vs. CSE 141



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Course Staff

Instructor: Michael Taylor

Email: mbtaylor@cs.ucsd.edu

Office Hours:

EBU 3b 4110

Tuesday right after class



TA: Sravanthi Kota Venkata

Email: tba

Office Hours:

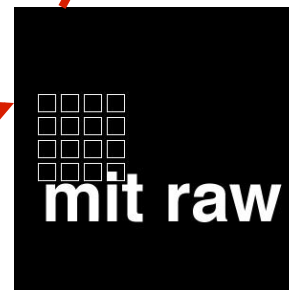
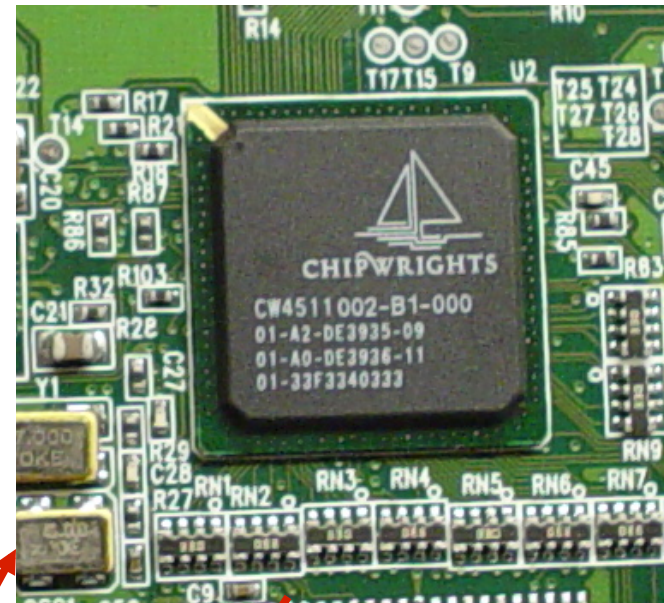
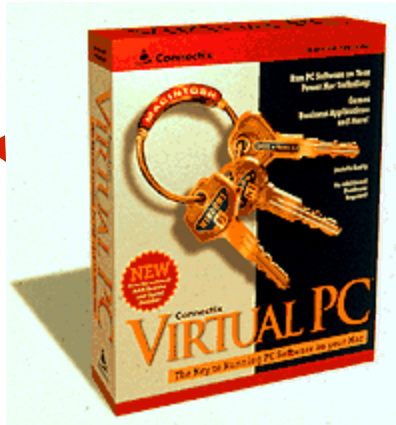
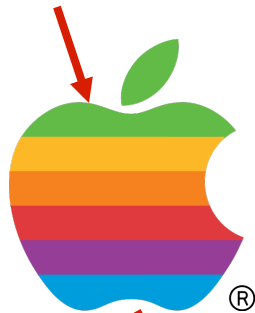
tba

<http://www-cse.ucsd.edu/classes/fa10/cse240a/>

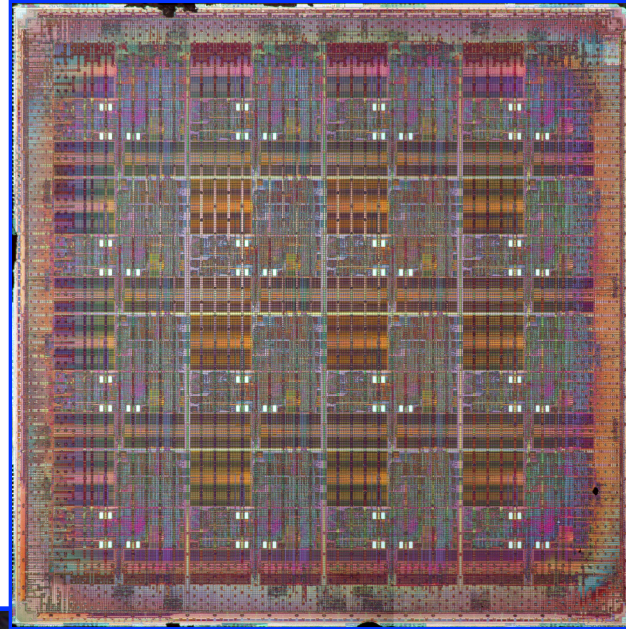
About Me

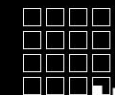
PowerMush 3

PowerMush IV

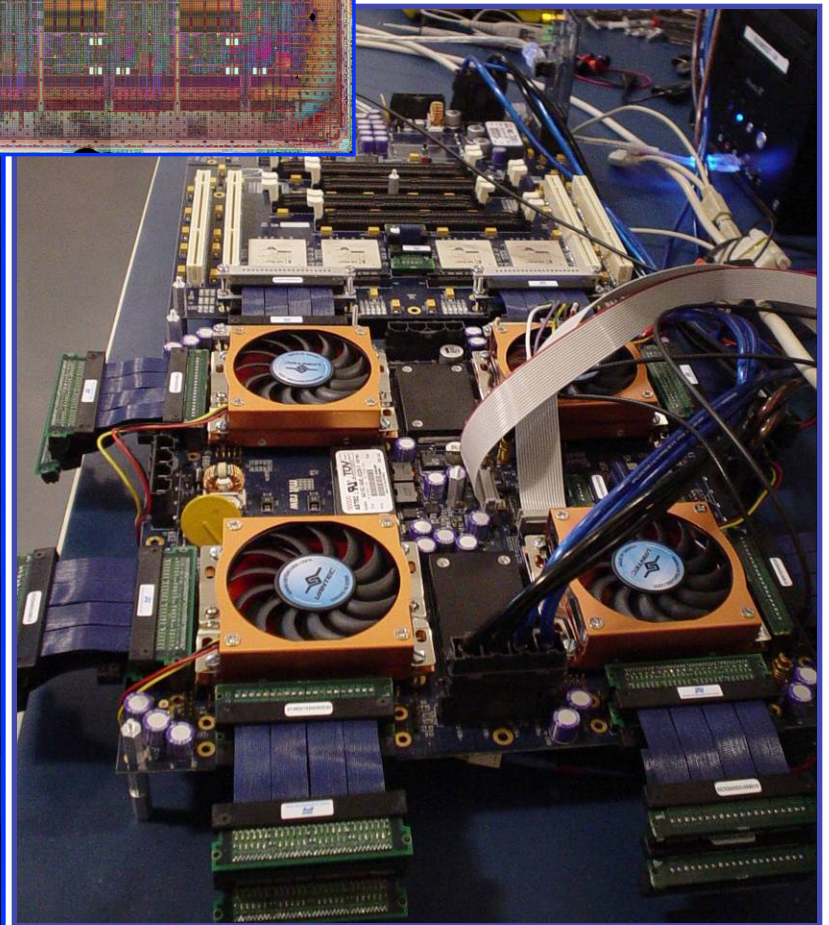


About Me




mit raw

~120 million
transistors



Course Outline

1. Technology
2. Measuring *Goodness*
3. Out-of-Order Superscalar
4. Memory Hierarchy
5. Power
6. Multiprocessors
7. UCSD Arch Greatest Hits

Please watch the website for course updates, reading assignments and homework assignments!