1.1 No Exponential is Forever: But "Forever" Can Be Delayed!

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Over the last fifty years, the solid-state-circuits industry has grown from infancy to become one of the largest industries in the world. Beyond the circuits themselves, solid-state circuits have become the basic building blocks of the trillion-dollar electronics industry, and have found their way into virtually all the products of modern civilization, ranging from automobiles to greeting cards. Looking back, it is hard to realize that early projections, based on the best industrial-engineering calculations of the time, suggested that transistors might eventually approach a fifty-cent manufacturing cost. That projection did not contemplate the invention of the integrated circuit and its subsequent evolution that now allows us to incorporate hundreds of millions of transistors in a single integrated structure.

The development and growth of the industry has been driven in large measure by the unique aspects of the technology, and by a market of unprecedented elasticity. Figures 1.1.1 to 1.1.3 illustrate the growth of the revenue of the semiconductor industry over the last third of a century, an estimate of the number of transistors produced each year, and the average cost of a transistor, as determined by dividing one set of data by the other. Along with a compound annual growth of about 15% per year, the revenue curve (Fig. 1.1.1) shows the ups and downs that the industry has experienced as the balance of production capacity and demand shifted. Figure 1.1.2, by contrast, shows a smooth growth in the estimated number of transistors produced each year, growing by nearly eight orders of magnitude over the last thirty years, an average compound annual growth of 78%, including several years during the 1970s and 1980s when it exceeded 100%.

Figure 1.1.3 divides the industry revenue by the estimated number of transistors produced, to show the average selling price per transistor falling over six orders of magnitude in the last thirty years, to about twenty micro-cents in 2002. Moreover, the cost of transistors in today's DRAMs is lower by another factor of ten. This unprecedented decrease in the cost of a manufactured product, combined with the growth in consumption, constitute the engine that has driven the industry.

No exponential change of a physical quantity can, however, continue forever. For one reason or another something limits continued growth. For our industry many of the exponential trends are approaching limits that require new means for circumvention if we are to continue the historic rate of progress. Business as usual will certainly bump up against barriers in the next decade or so. Already, the flattening of the industry-revenue curve since 1994 (Fig. 1.1.1) gives cause for concern.

A characteristic of the technology that has enabled such remarkable growth is that making devices smaller improves circuit operation in nearly all ways. The transistors become faster and consume less power. Our ability to integrate complex functions increases, thus improving system reliability, reducing size and weight and allowing much-more-complex systems to be constructed economically and reliably. But most importantly, because of the much greater packing density available, the cost of manufacture is greatly reduced.

The minimum feature size in production integrated circuits (Fig. 1.1.4) has continued on an exponential decline since the first integrated circuits appeared. If anything, the rate of feature-size decrease has increased over the last several years from the historical halving time of six years, as industry participants vie for a competitive edge. The time between technology "nodes" as defined in the International Technology Roadmap for Semiconductors, 2001 Edition, is moving toward two years from the historic three. Even though it is increasingly difficult and expensive to decrease feature size, the competitive advantage resulting from being early with next-generation products drives this acceleration. From the technology roadmap, companies know the level of technology likely to exist, so they set their development programs to be competitive.

Several times in the past, it has appeared that technological barriers would slow or even halt these trends, but with the high stakes involved, companies have found pathways around the barriers. But a new and more fundamental barrier must be confronted in the next couple of decades — the fact that materials are made of atoms and the technology is approaching atomic dimensions. This problem is probably most immediate in the thickness of the gate dielectric of transistors (Fig. 1.1.5), another dimension that has shown approximately exponential decrease with time. As the transmission-electron micrograph in Fig. 1.1.6 illustrates, when silicon dioxide is used as the gate dielectric, next-generation transistors provide only a couple of molecular layers of insulator. At least here the possibility of using a material with higher dielectric constant holds the promise of achieving the same electric fields with a thicker insulator, postponing the problem.

One well-known exponential relates to the increase in complexity of the most complex integrated circuits. This is a consequence of the decreasing printed dimensions and improved manufacturing processes that allow the economic production of larger and larger dice. I first observed this trend in the early days of integrated circuits [1], when trying to forecast industry trends over the next decade. Figure 1.1.7a reproduces this original 1965 projection of an annual doubling, which has subsequently been dubbed "Moore's Law". Figure 1.1.7b shows this prediction with the data history available in 1975. Figure 1.1.8 shows a similar graph including my 1975 projections [2] along with data points showing the actual history. To a considerable degree, the approximately two-year doubling time predicted in 1975 is a consequence of shrinking printed dimensions and growing die size. The faster rate of increase in complexity that occurred through 1975 resulted from inclusion of an additional driving factor — new circuits and device structures squeezing out wasted area on the silicon. By 1975, there was little left to squeeze, so the rate of progress slowed.

Many other parameters show approximate-exponential behavior, mostly because of their relationships with decreasing dimensions and increasing complexity. For example, Fig. 1.1.9 shows the increase in computer performance benefiting from both faster transistors and an exponentially increasing transistor budget. Figure 1.1.10 depicts the increasing power-dissipation of microprocessor chips despite all attempts to decrease operating voltage (Fig. 1.1.11) and minimize leakage currents.

Key to continuing the historic trends, the transistor itself must evolve from the planar structure generally used today. Several ideas have been put forth to decrease leakage and continue speed improvements, including fully-depleted silicon-on-insulator [3], as well as double-gate [4] and triple-gate [5] structures. Figure 1.1.12 shows directions in which the standard planar transistor is evolving. Even the crystal structure of the silicon has been modified by introducing strain into the lattice to increase carrier

mobility and, hence, transistor performance [6]. Figure 1.1.13 illustrates a three-dimensional, triple-gate transistor, one of the more radical changes being studied.

Deployment of such new transistors can continue progress for at least an additional few generations. The technological challenges continue to escalate, but so do the financial challenges. As an example, Fig. 1.1.14 shows the cost of a production-lithography tool over the last several generations of technology. Clearly in an industry where revenue growth seems to be slowing, this also represents a formidable obstacle. But the industry has been challenged before, and has risen to the occasion.

There are many approaches to solving the problems that the industry now faces. The resourcefulness of engineers and scientists faced with apparent blockades to continuing progress has been fantastic, and I expect it to continue. For at least several more generations, there appear to be approaches that will continue progress at roughly the rate it has moved historically. But even if the doubling-times stretch in the future, the rate of progress in the semiconductor industry will far surpass that of nearly all other industries. It is truly a revolutionary technology!

References

[1] G. E. Moore, "Cramming more Components onto Integrated Circuits," *Electronics*, vol. 38, no. 8, April 19, 1965.

[2] G. E. Moore, "Progress in Digital Integrated Electronics," *Technical Digest of International Electron Devices Meeting*, p. 11, Dec. 1975.

[3] R. Chau, et al, "A 50nm Depleted-Substrate CMOS Transistor (DST)," *Technical Digest of International Electron Devices Meeting*, pp. 621-624, Dec. 2001.

[4] X. Huang, et al. "Sub 50-nm FinFET: PMOS," *Technical Digest of International Electron Devices Meeting*, pp. 67-70, Dec. 1999.

[5] R. Chau et al, "Advanced Depleted Substrate Transistors: Single-gate, Double-gate and Tri-gate," *Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials*, pp. 68-69, Sept. 2002, Nagoya, Japan.

[6] S. Thompson, et al, "A 90nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1μm² 6-T STAM Cell," to be published in the *Technical Digest of International Electron Devices Meeting*, Dec., 2002.

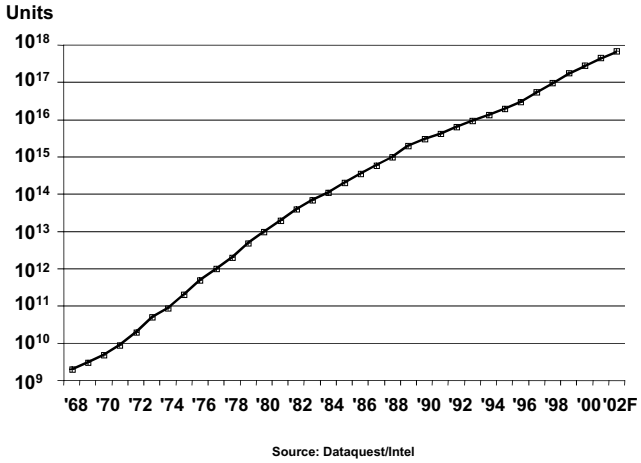


Figure 1.1.2: Transistors shipped per year.

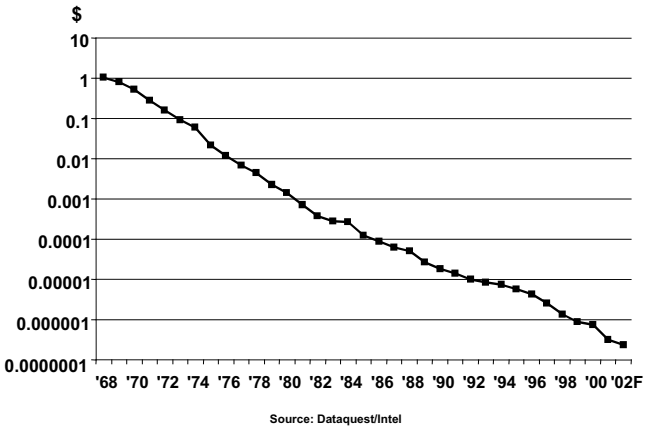


Figure 1.1.3: Average transistor price by year.

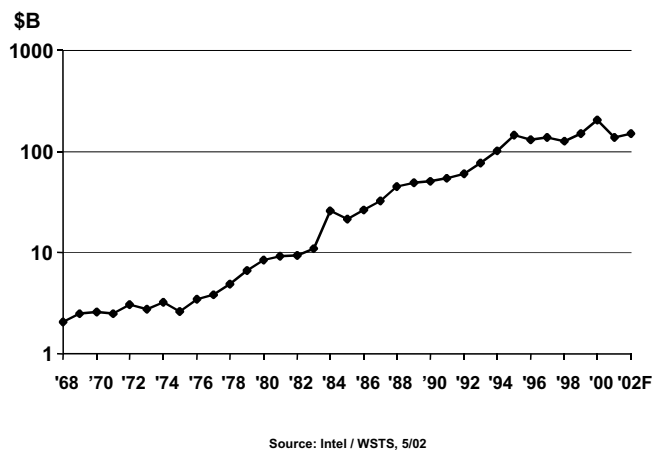


Figure 1.1.1: Worldwide semiconductor revenues.

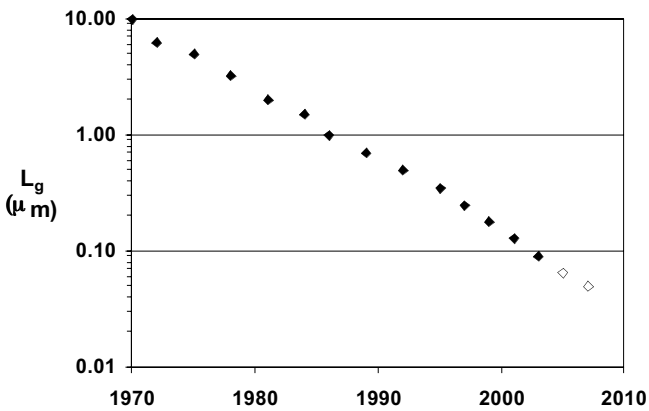


Figure 1.1.4: Minimum feature size (μm).

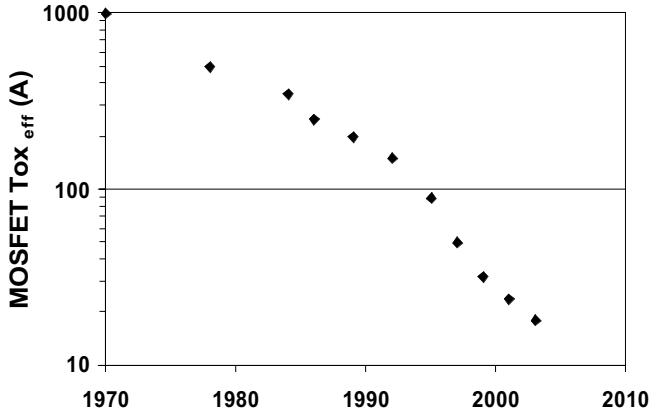
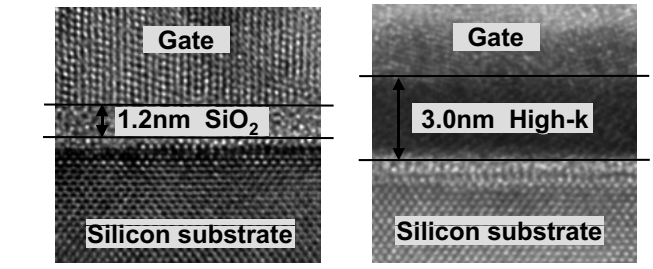


Figure 1.1.5: MOSFET effective dielectric thicness (A).



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Leakage	1X	< 0.01X

Figure 1.1.6: High K for gate dielectrics.

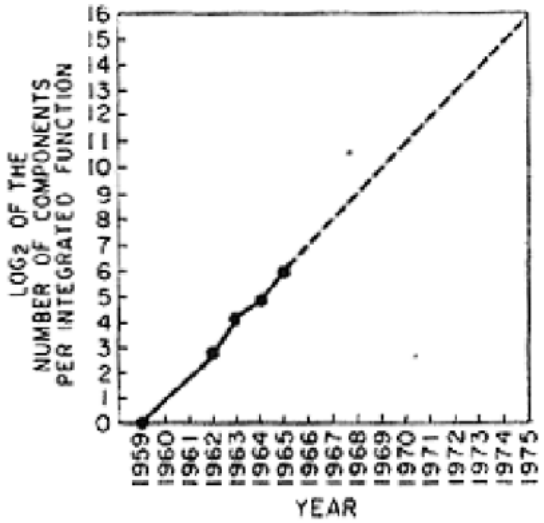


Figure 1.1.7: (a) 1965 transistor projection.

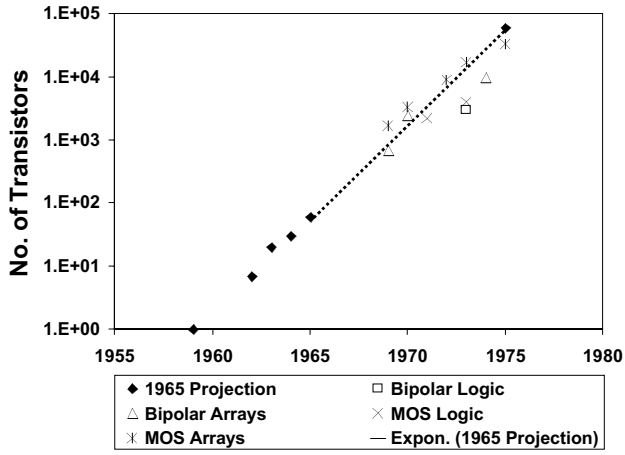


Figure 1.1.7: (b) 1965 transistor projection with Data in 1975.

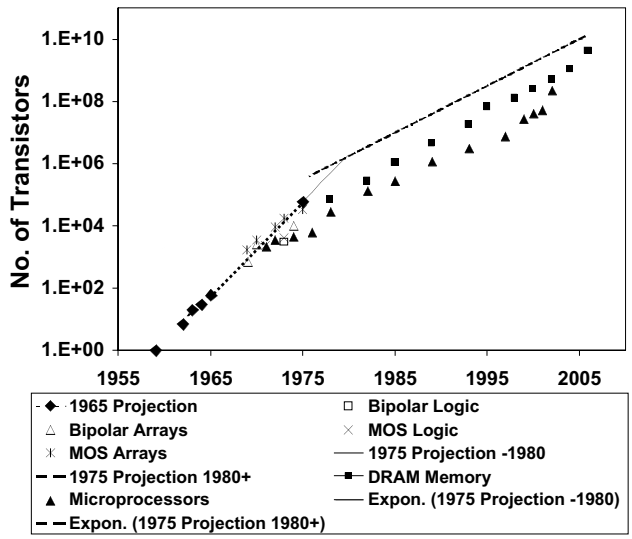


Figure 1.1.8: 1975 transistor projection with data.

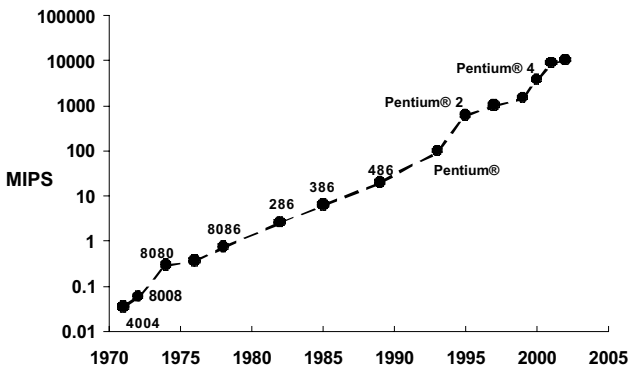


Figure 1.1.9: Processor performance (MIPS).

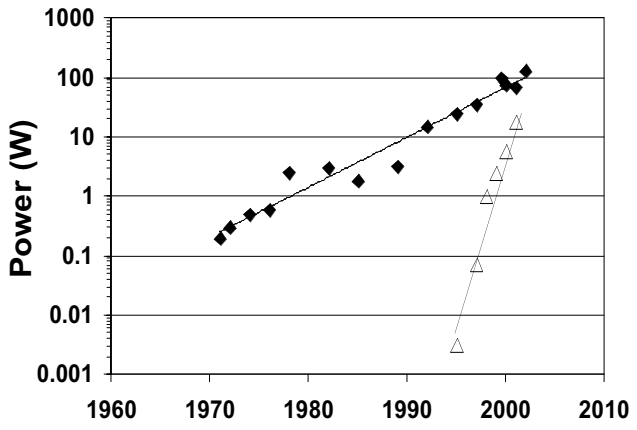
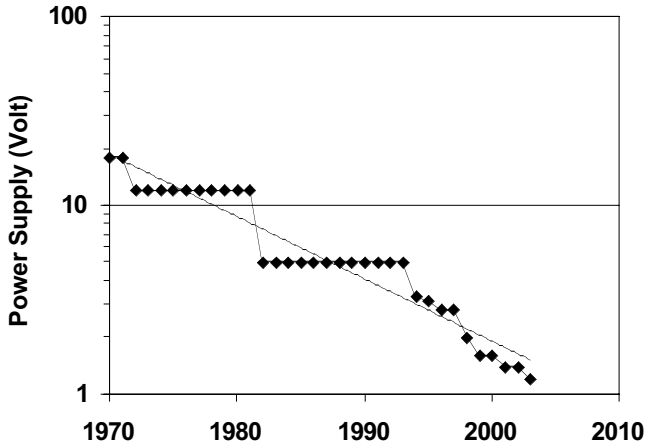


Figure 1.1.10: Processor power (watts) - active and leakage.



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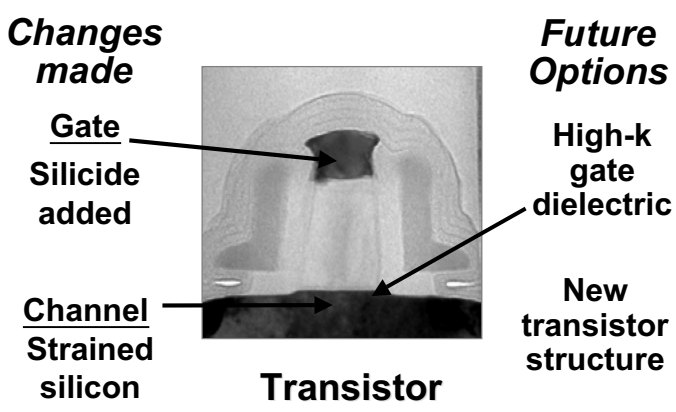

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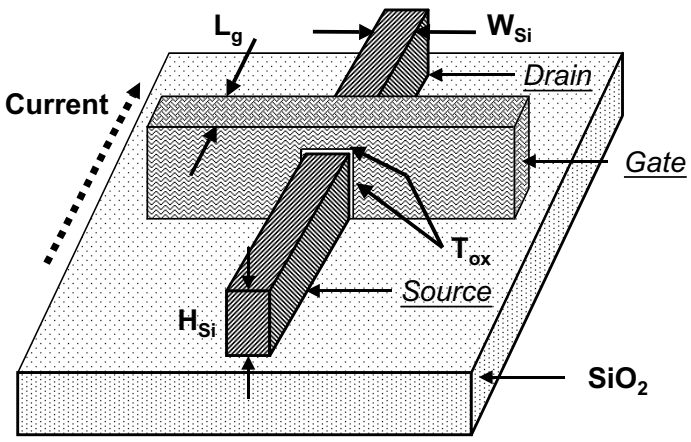


Figure 1.1.13: Tri-gate transistor structure.

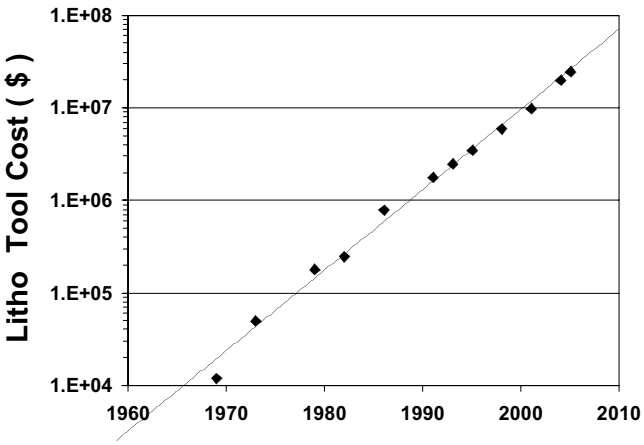
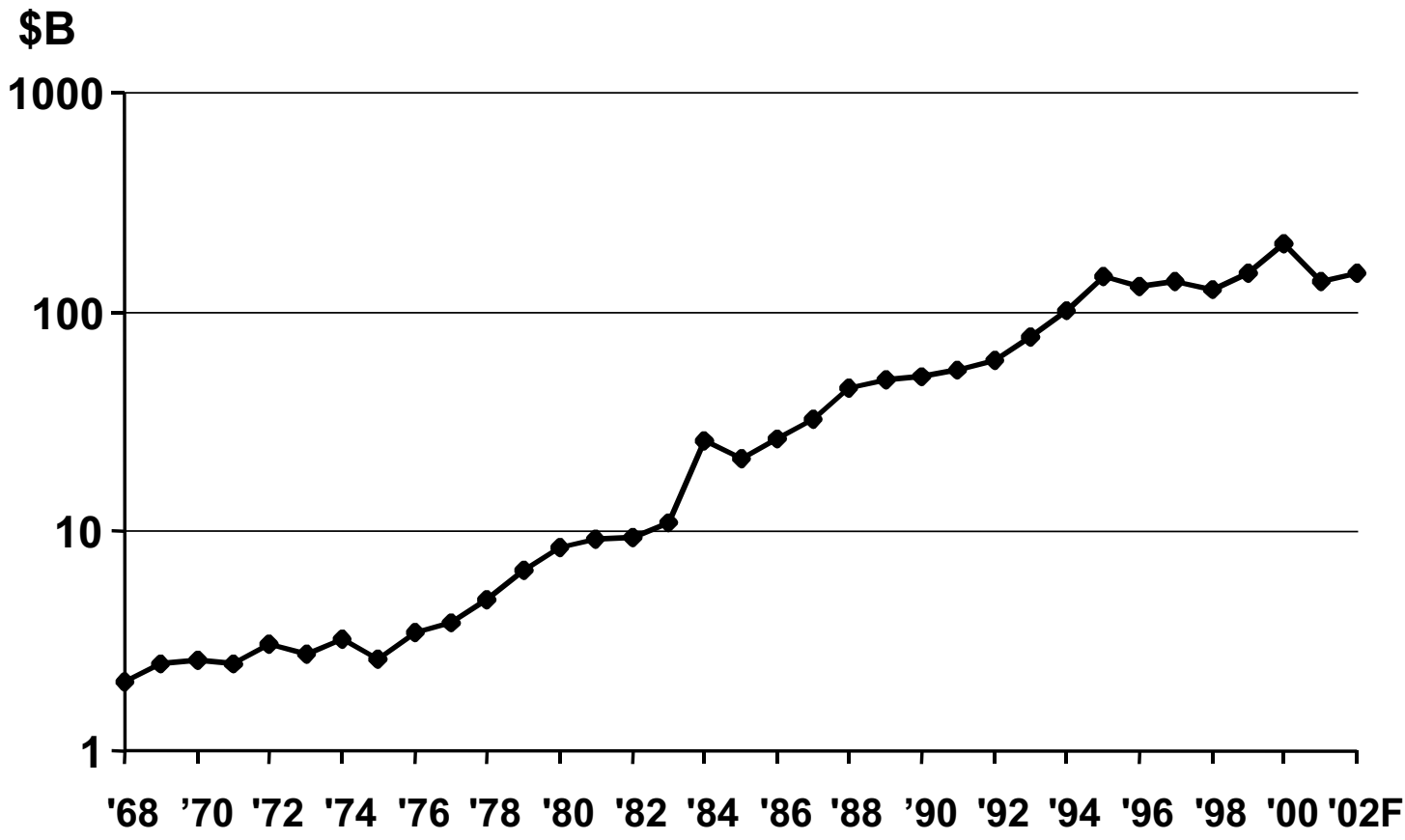


Figure 1.1.14: Lithography Tool Cost ($).



Source: Intel / WSTS, 5/02

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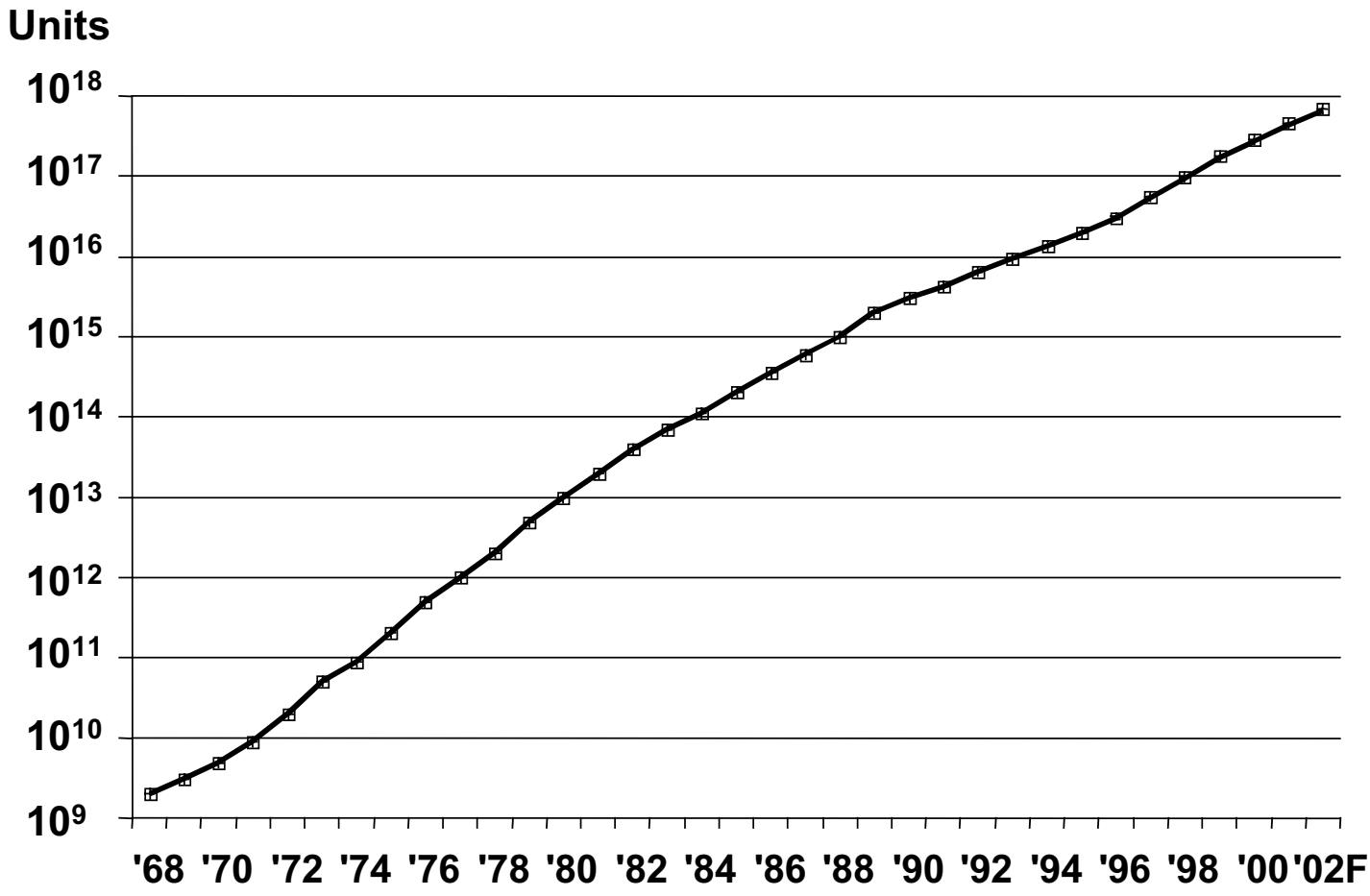

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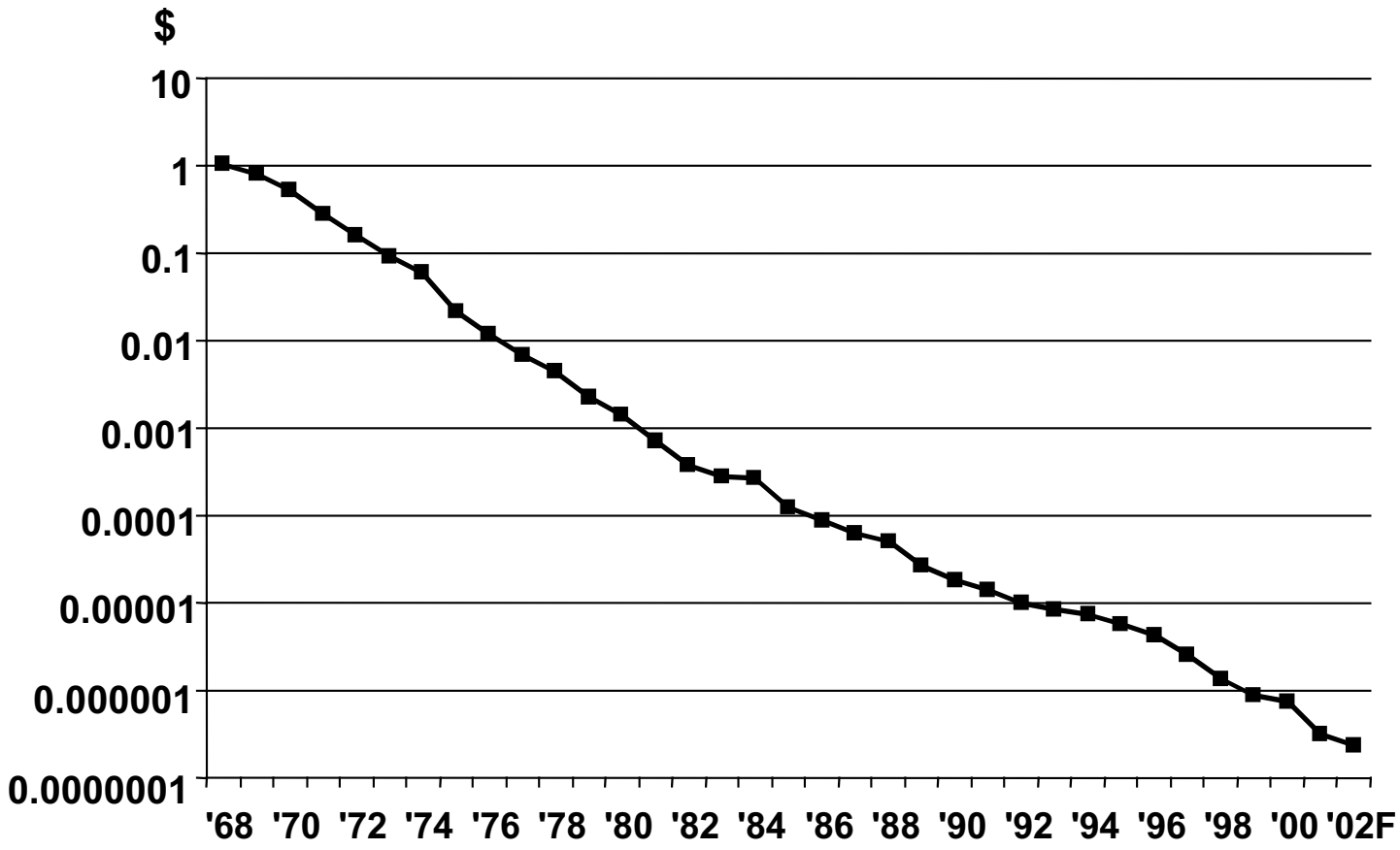

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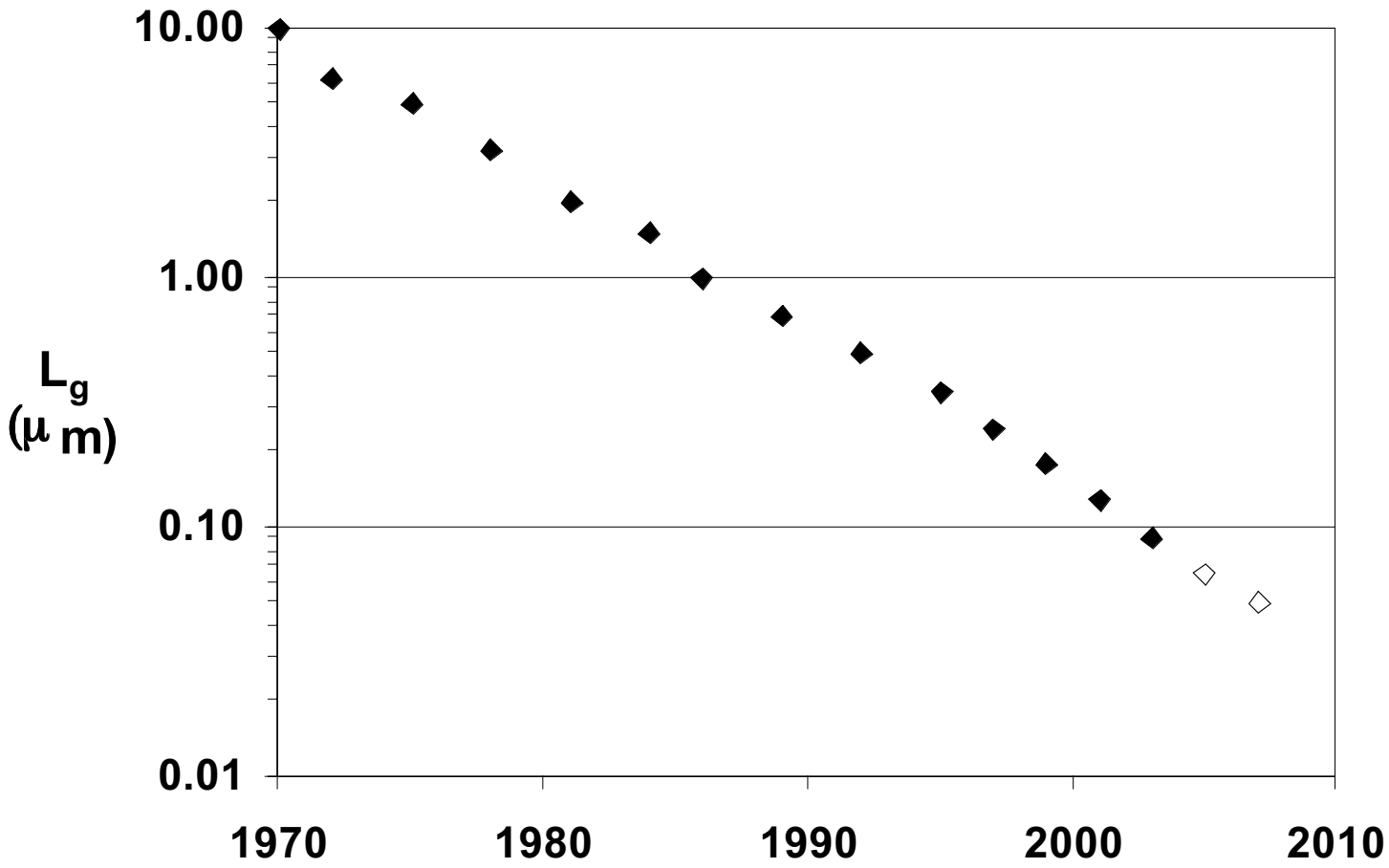

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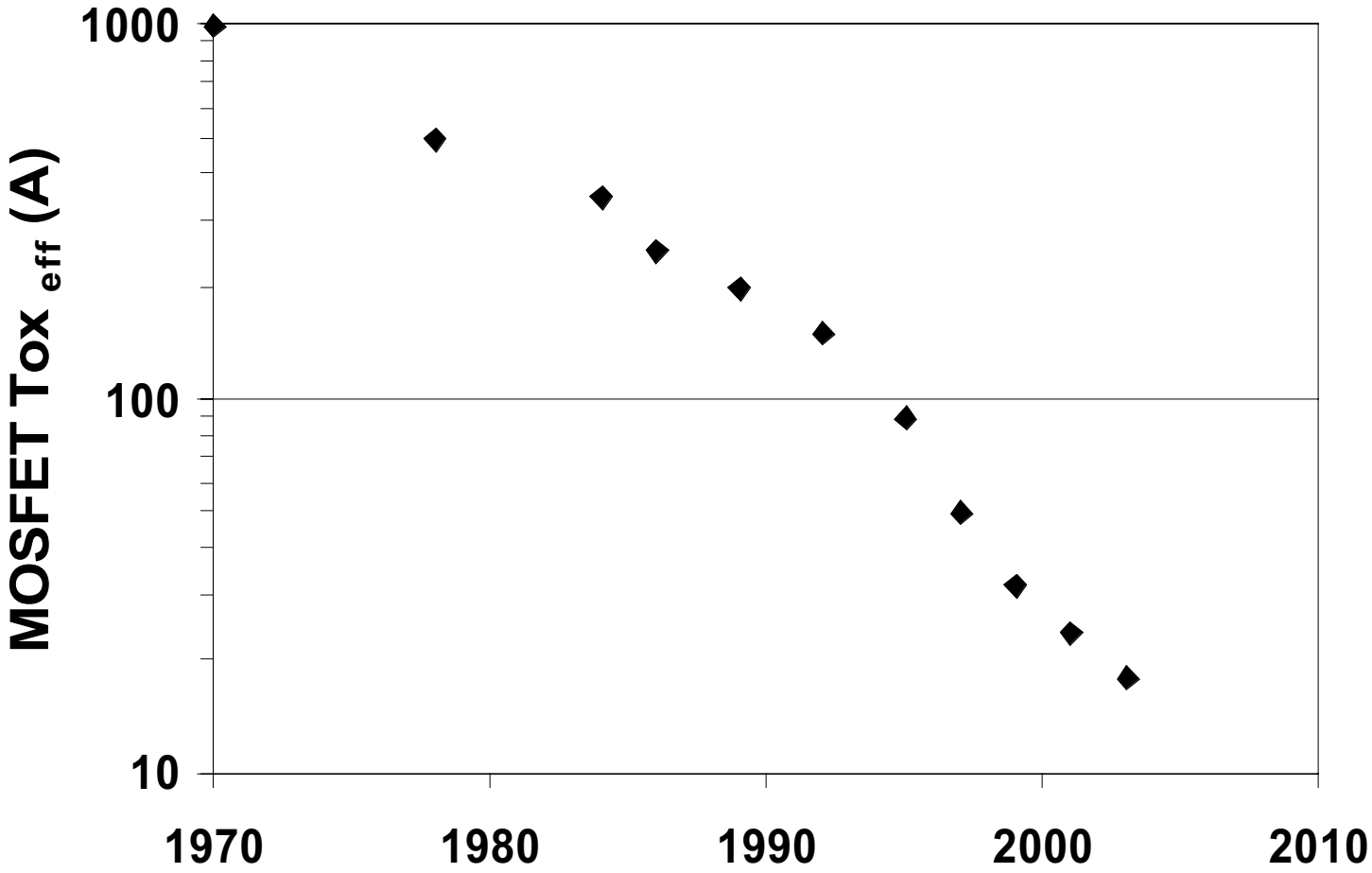

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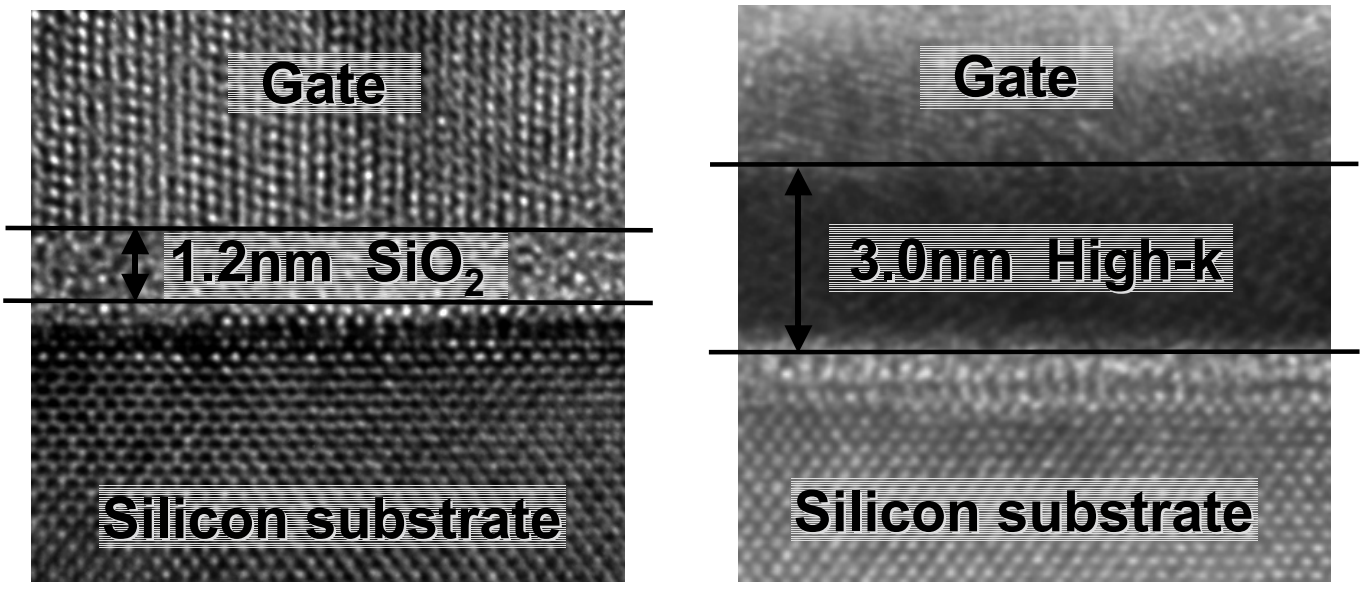

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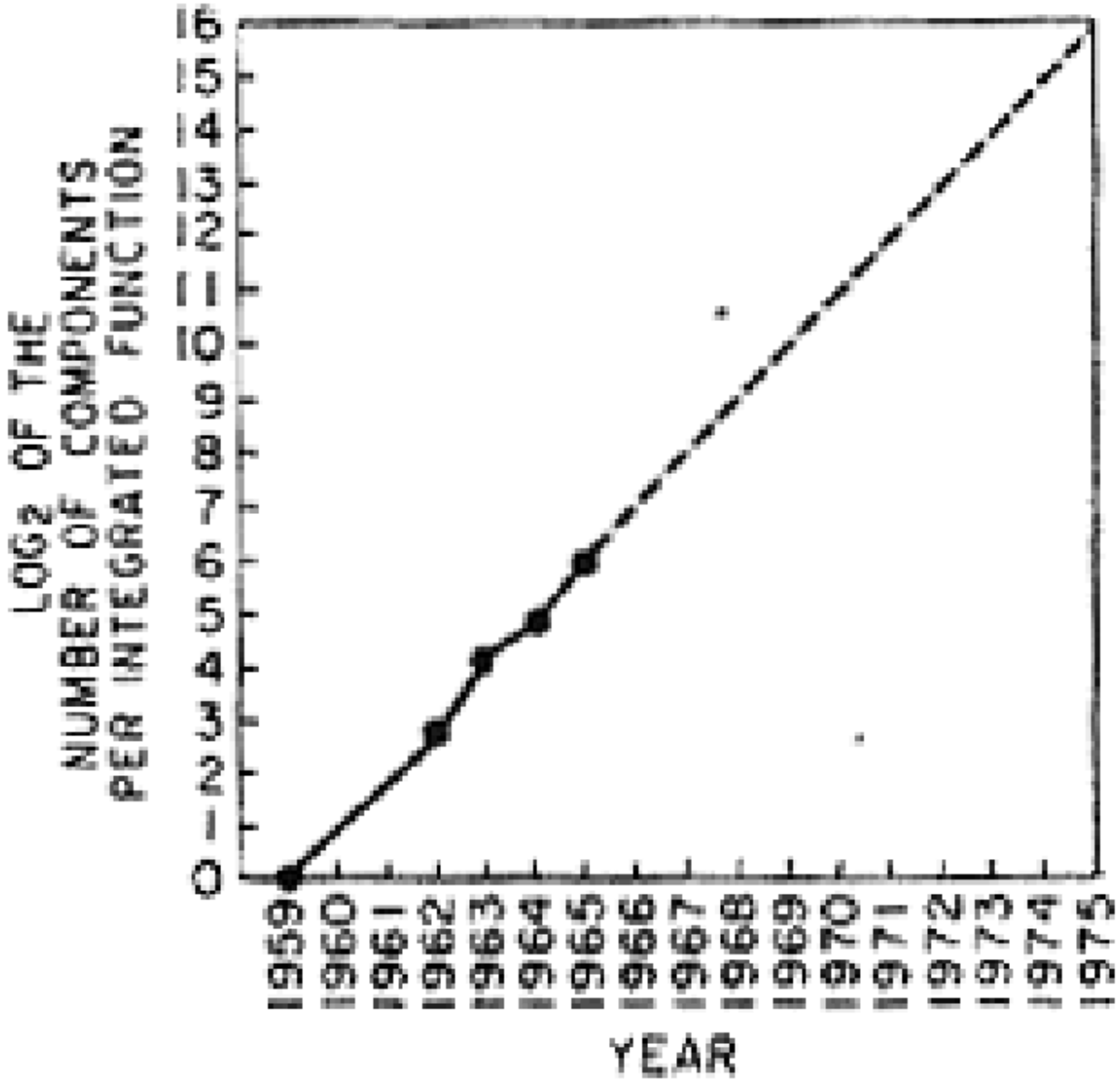

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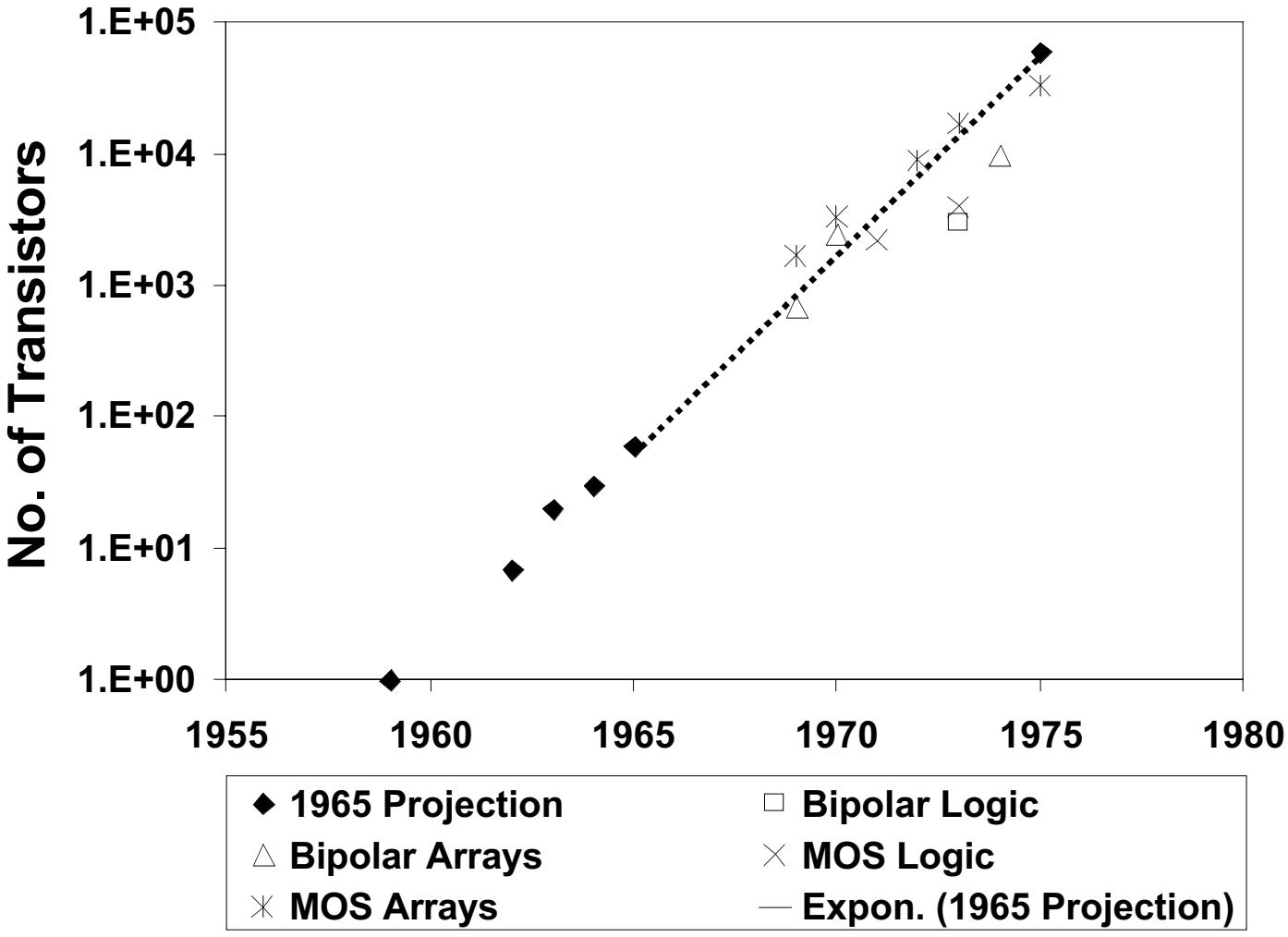

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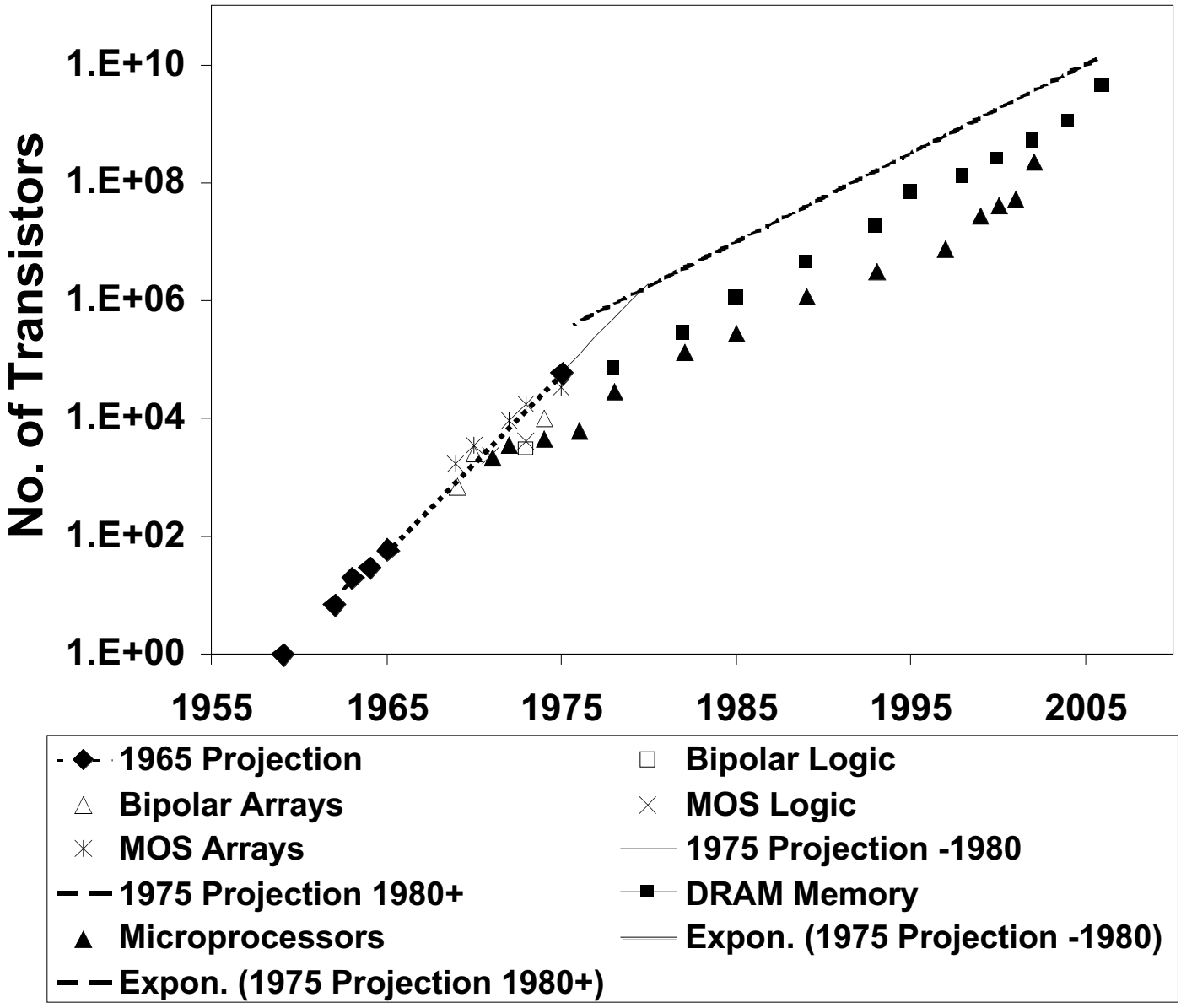

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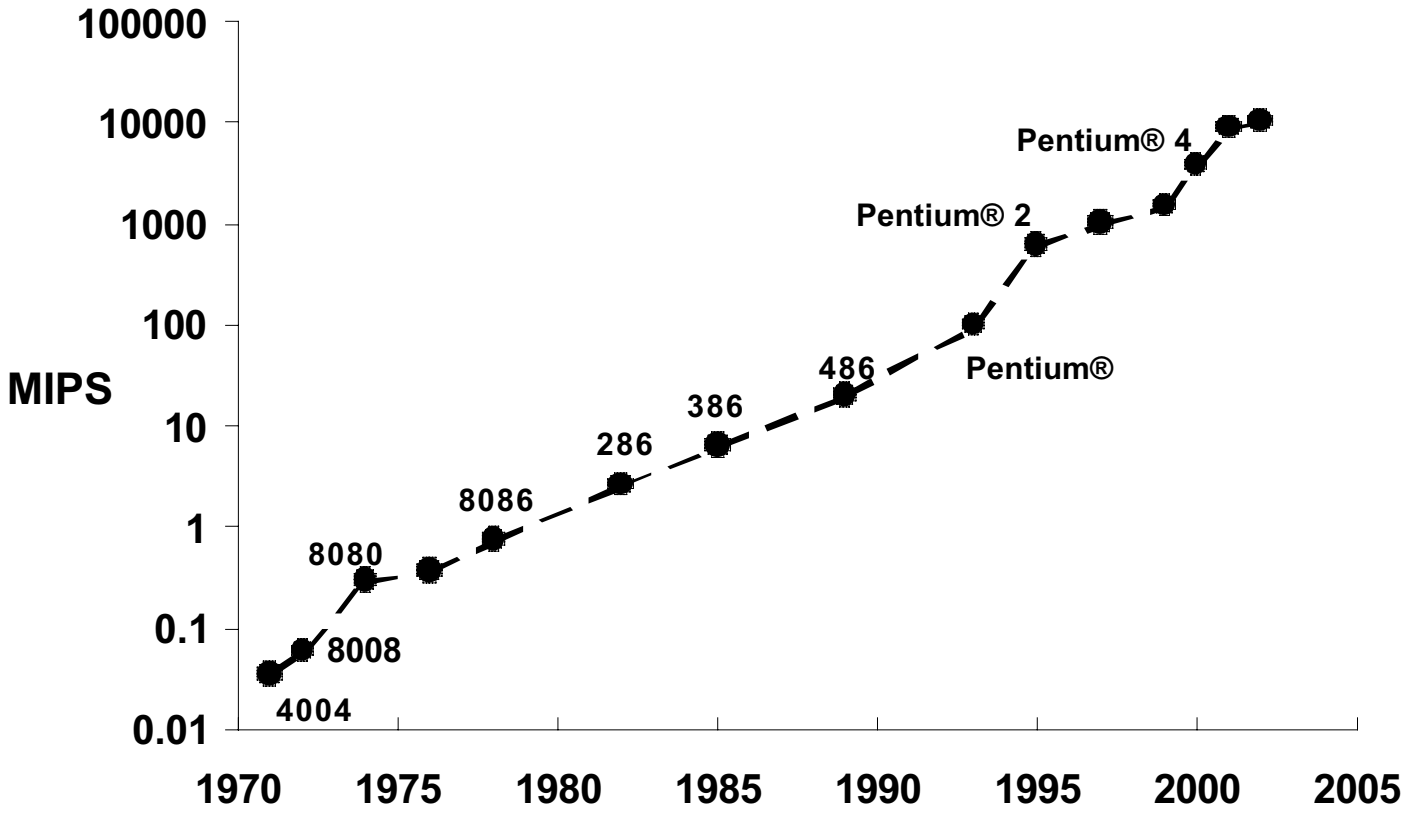

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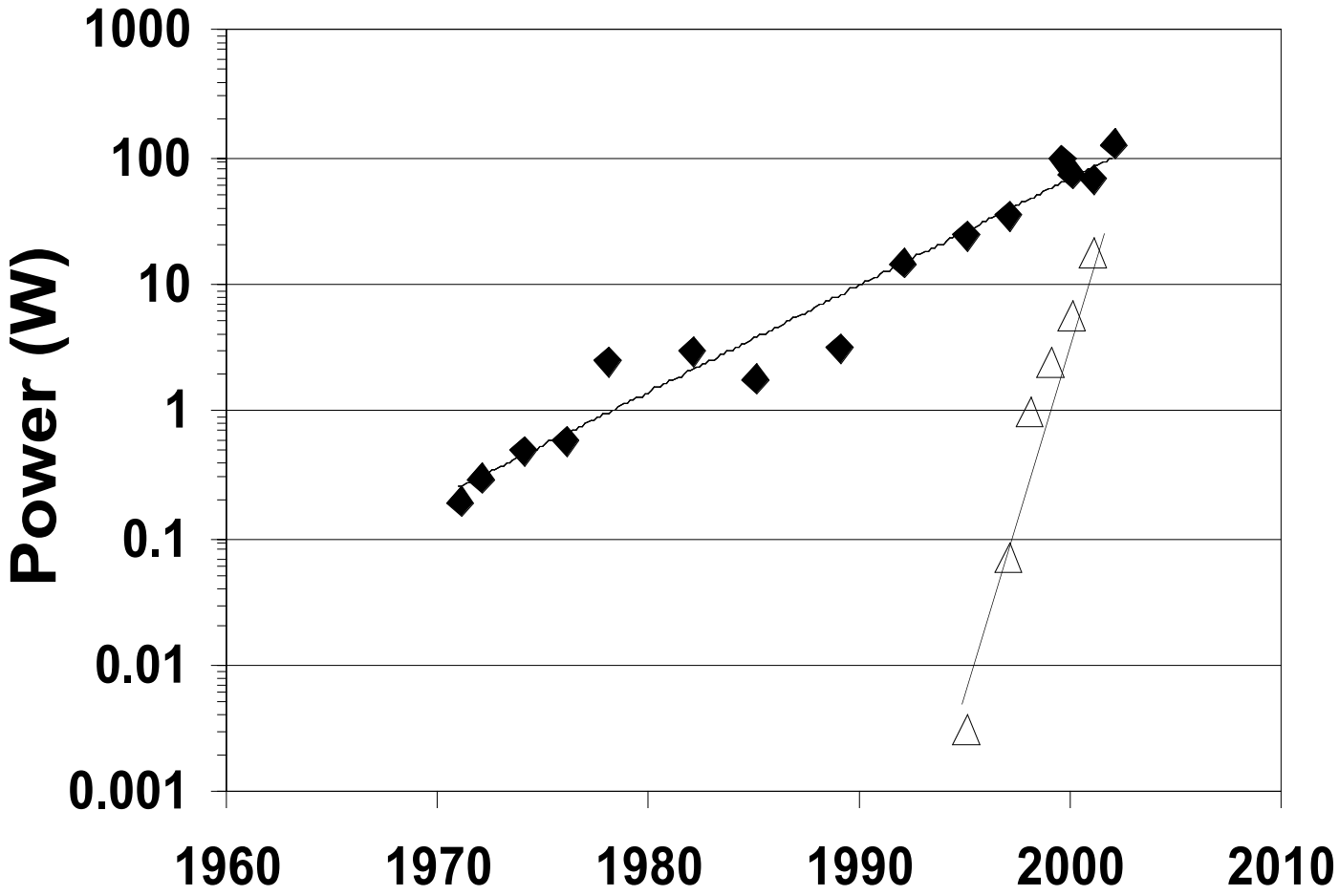

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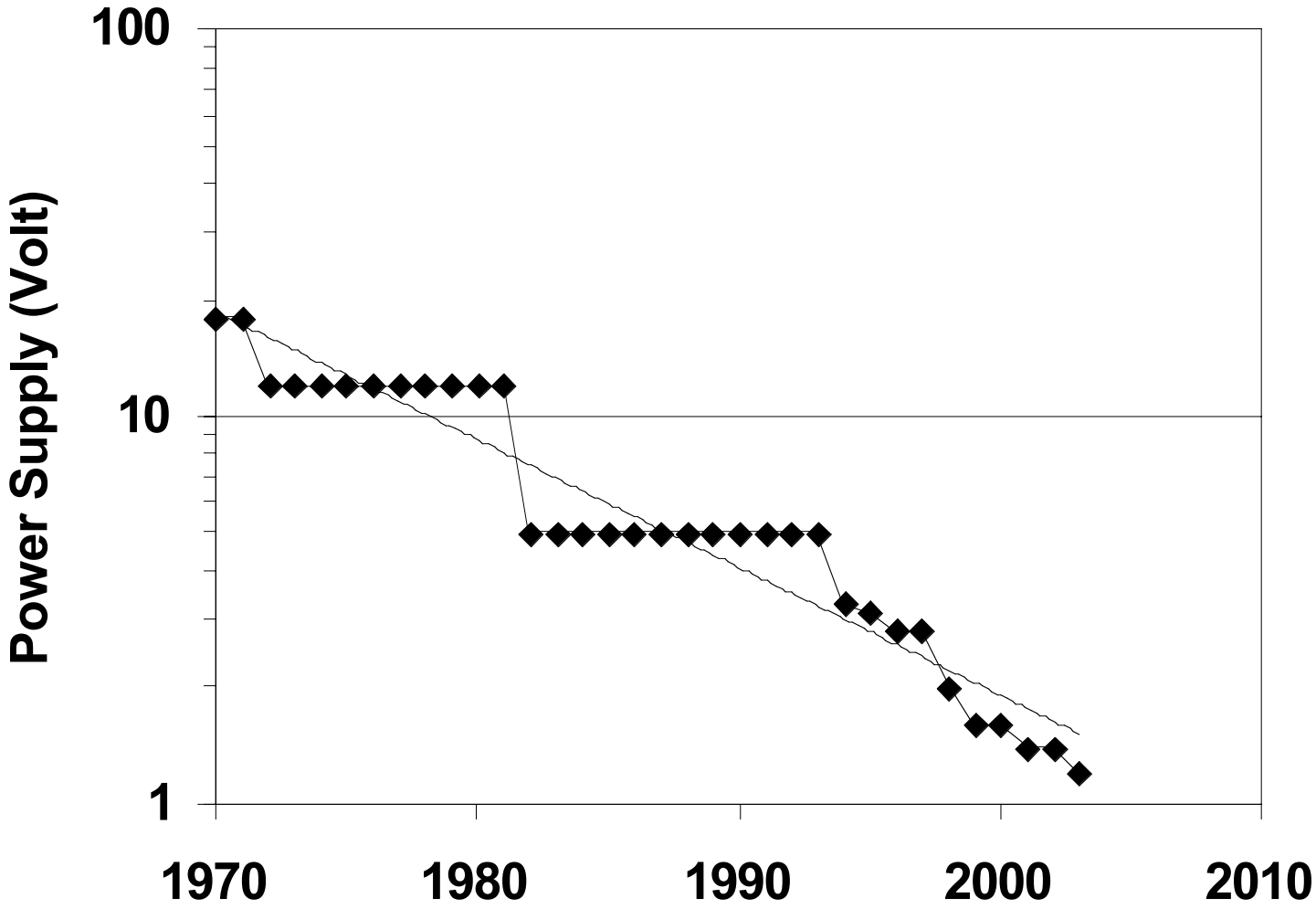

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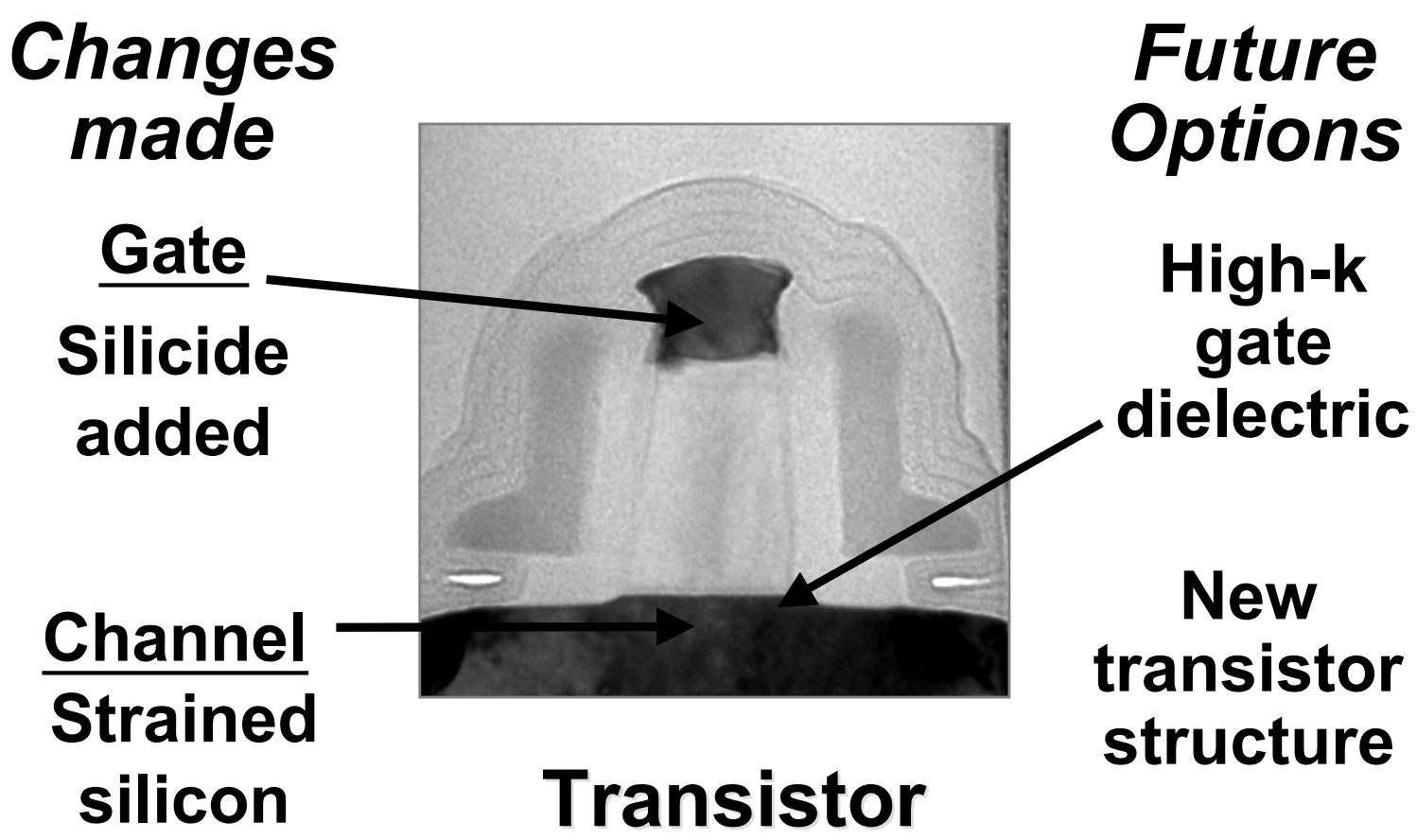

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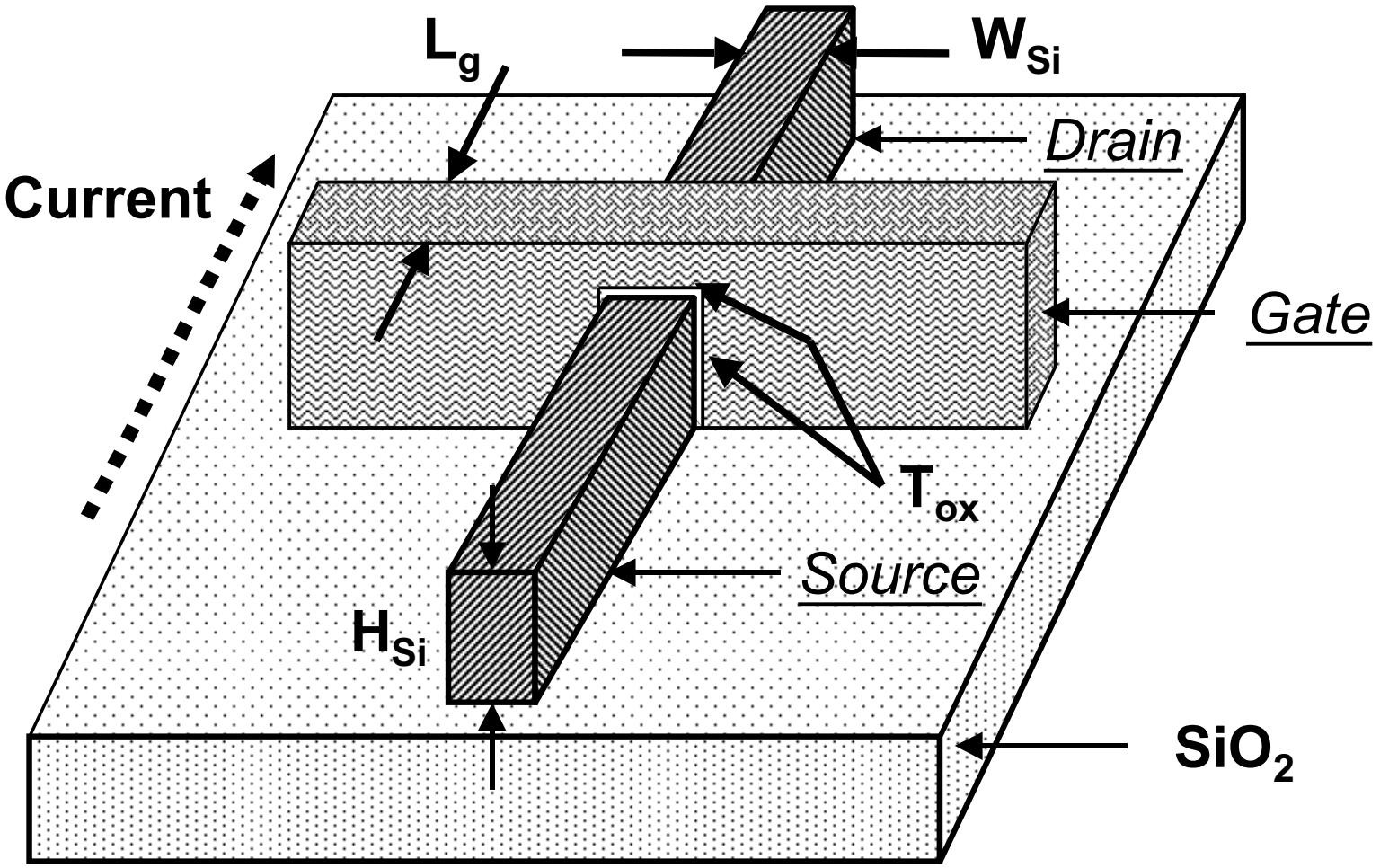

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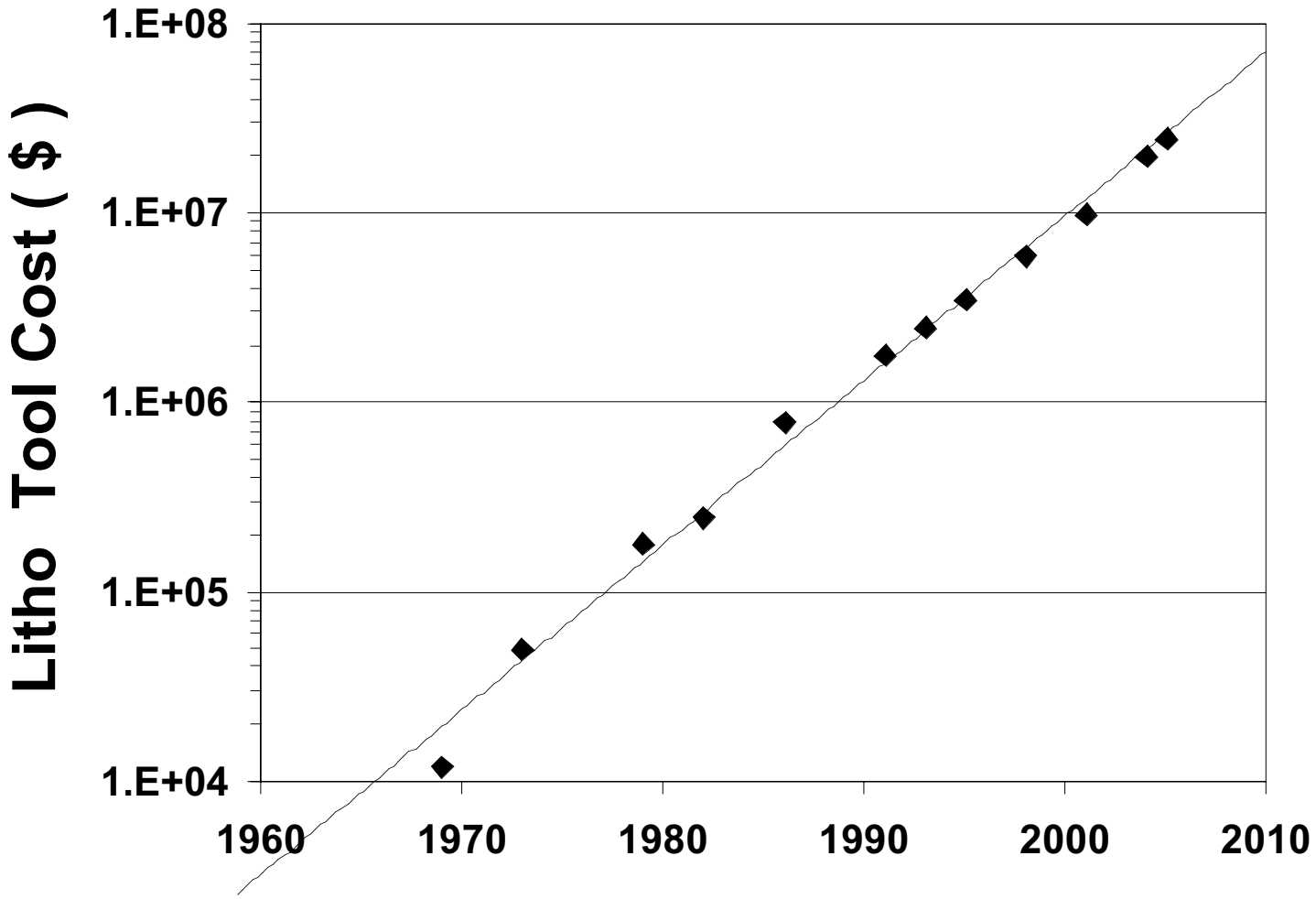

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