International Technology Roadmap for Semiconductors

2008 ITRS ORTC

[7/14-16 ITRS Meetings San Francisco]

A.Allan, Rev 1 (for 7/16 Public Conference Prep)

Agenda

- Moore's Law and More
- Technology Pacing Trends Update
  – Physical and Printed GL Focus
- Summary

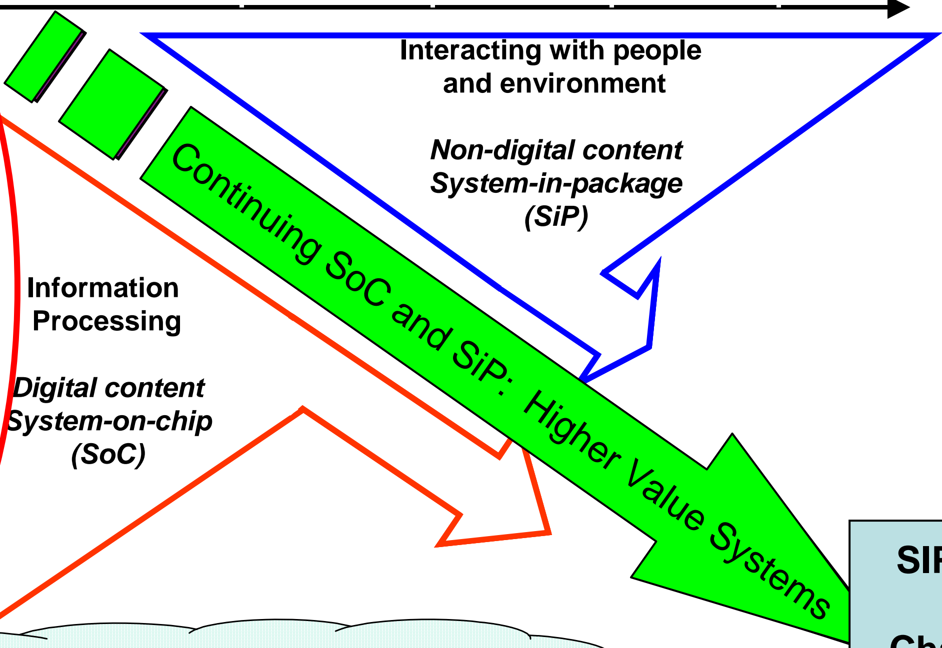
- Backup
  – Function Size, Moore's Law on Track
  – Design On-Chip Frequency
  – SICAS Technology, Wafer Generation Demand Update
  – Definitions

2008 ITRS Executive Summary Fig 5

[updated for 2007]

[2008 – Update Definitions]

Moore's Law & More



Work in Progress – Do Not Publish

2007 ITRS "Moore's Law and More" Alternative Definition Graphic

Baseline CMOS | **Memory** | **RF** | **HV Power** | **Passives** | **Sensors, Actuators** | **Bio-chips, Fluidics**

"More Moore"

"More than Moore"

Computing & Data Storage

Sense, interact, Empower

Heterogeneous Integration

System on Chip (SOC) and System In Package (SIP)

Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

Work in Progress – Do Not Publish

2008 ITRS "Beyond CMOS"

Baseline CMOS *Ultimately Scaled CMOS* *Functionally Enhanced CMOS* *Nanowire Electronics* *Ferromagnetic Logic Devices* *Spin Logic Devices*

32nm 22nm 16nm 11nm 8nm

Multiple gate MOSFETs
Channel Replacement Materials
Low Dimensional Materials Channels

New State Variable
New Devices
New Data Representation
New Data Processing Algorithms

"More Moore" *"Beyond CMOS"*

Computing and Data Storage Beyond CMOS

Source: Emerging Research Device Working Group

Work in Progress – Do Not Publish

2007 - PIDS/FEP - Simplified Transistor Roadmap

[Examples of "Equivalent Scaling" from ITRS PIDS/FEP TWGs] – Update in 2009

poly
SiON
metal
high k
gate stack

electrostatic control
bulk
planar
PDSOI
FDSOI
MuGFET
MuCFET
3D

stressors
+ substrate engineering
+ high μ materials

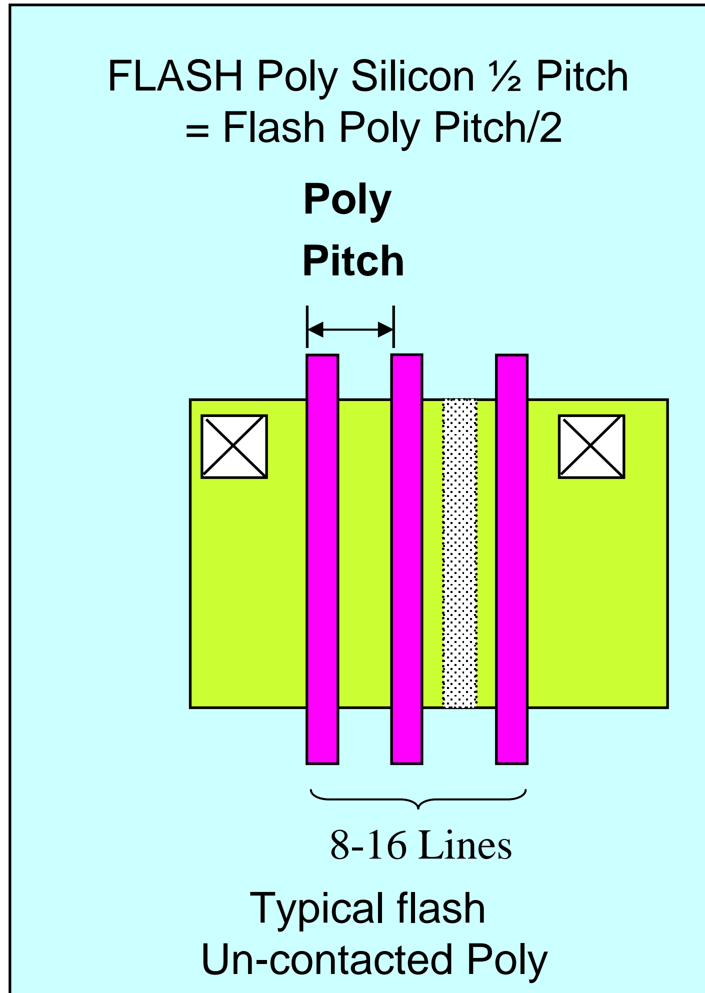
65nm	45nm	32nm	22nm
[ITRS DRAM/MPU Timing: 2007[7.5]	2010	2013	2016]

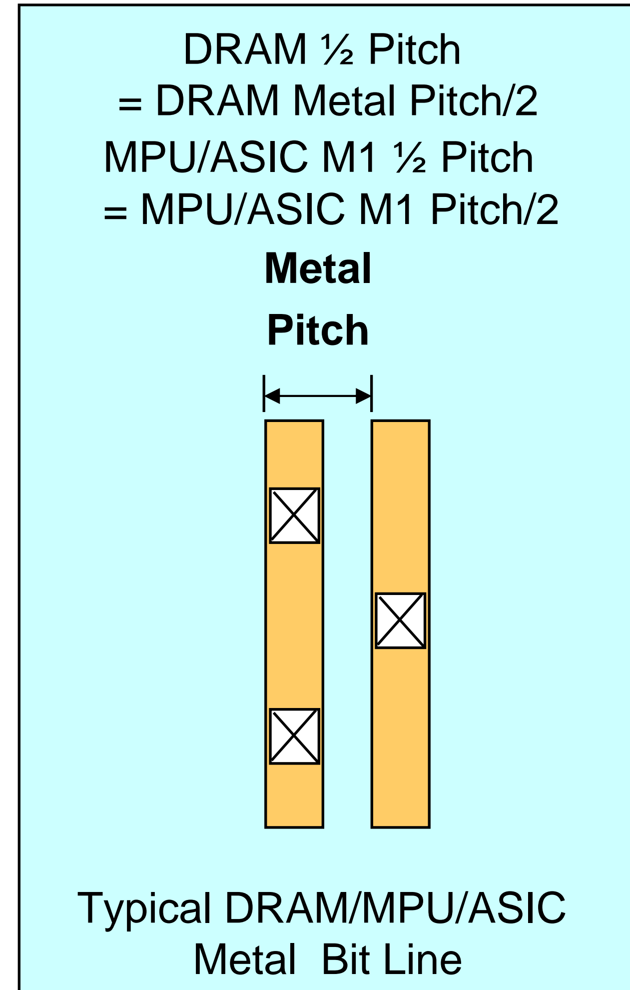
Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

Work in Progress – Do Not Publish

2007 Definition of the Half Pitch – 2008 unchanged

[No single-product "node" designation; DRAM half-pitch still litho driver; however, other product technology trends may be drivers on individual TWG tables]





Source: 2005 ITRS - Exec. Summary Fig 2

Fig 3

2008 - Unchanged

Production Ramp-up Model and Technology Cycle Timing

Source: 2005 ITRS - Exec. Summary Fig 3

Work in Progress – Do Not Publish

2007 ITRS Product Technology Trends - Half-Pitch, Gate-Length

[WAS]

Label	Trend
Before 1998	.71X/3YR
After 1998	.71X/2YR
MPU M1	.71X/2.5YR
MPU & DRAM M1 & Flash Poly	.71X/3YR
Flash Poly	.71X/2YR
Gate Length	.71X/3YR

GLpr IS = 1.6818 x GLph

Nanotechnology (<100nm) Era Begins -1999

Y-axis: Product Half-Pitch, Gate-Length (nm) — 1.0, 10.0, 100.0, 1000.0

X-axis: Year of Production — 1995, 2000, 2005, 2010, 2015, 2020, 2025

Legend:
- DRAM M1 1/2 Pitch
- MPU M1 1/2 Pitch (2.5-year cycle)
- Flash Poly 1/2 Pitch
- MPU Gate Length - Printed
- MPUGate Length - Physical

2007 - 2022 ITRS Range

Work in Progress – Do Not Publish

2008 ITRS Update - Technology Trends vs Actuals and Survey

nanometers (1e-9)

1000

100

10

2000

2025

2.5-year Cycle [.5^(1/5yrs)]

"More Moore" Functional Density Complemente d by "Equivalent Scaling" Performance/ Power Mgt [Copper IC; Strain Si; Metal Gate/ Hi-K; UTB/FDSOI; MUG; etc.]

Printed GL = Physical GL After 2019

3-year Cycle

GLprinted = [decreasing Etch ratio]

GLphysical = ~0.71x/ 3.8yrs

“32nm” 2yr GLph delay

“20nm” 3yr GLph delay

“10nm” 5yr GLph delay

“45nm” 1yr GLph delay

Work in Progres Not Publish

Work in Progress - Do Not Publish!

Jeff Butterbaugh/FEP GLphys Actuals (leading):

Kwok Ng/PIDS GLphys Survey (leading):

Glpr(nm) MPU (ITRS 05-07) 2008 Update

Glph(nm) MPU (ITRS 05-07) 2008 Update

M1 Half Pitch(nm) MPU (ITRS 05-07) **[also DRAM M1 in 2008 Update]**

M1 Half Pitch(nm) DRAM (ITRS 05-07)

Poly Half Pitch(nm) Flash (ITRS 07) **[Litho Driver after 2007]**

GLph Proposal 2008 Update

- GLphysical 2008 Update IS: 3.8yr cycle after 2007; enabled by “Equiv. Scaling”
- FEP and PIDS have proposed shifted/interpolated tables; full model redo in ‘09
- GLprinted parallel to MPU/DRAM M1 Half-Pitch; shrinking etch ratio to GLphy

Work in Progress – Do Not Publish

ORTC Summary – 2008 Update Status

- ✓ **Flash** Model un-contacted poly half-pitch trend
  - **Unchanged** 2-year cycle* through 2008/45nm, then 3-year cycle* (2014/22.5; 2020/11.25); ;
  - **Unchanged**: Cell Design Factor; Array Efficiency; Bits/Chip
  - PIDS Flash Survey Team to report status of survey data update and proposals in July meetings.
- ✓ **DRAM** Model stagger-contacted **M1 half-pitch updated to the MPU 2.5-year cycle* through 2010/45nm [affects 2007, 2008, 2009], then**
  - **Unchanged** 3-year cycle* beginning 2010/45nm (2016/22.5; 2022/11.25);
  - **Unchanged**: Cell Design Factor; Array Efficiency; Bits/Chip
- ✓ **DRAM function size, function density, and chip size models have been updated to latest Product 2.5-year cycle scaling rate;**
  - **Only 2007-2009 years affected** in 2008 Table Update.
  - **Unchanged 2010-2022**
- ✓ **MPU** Model M1 stagger-contact half-pitch **unchanged** from 2007
  - 2.5-year cycle* through 2010/45nm, then 3-year cycle* (2016/22.5; 2022/11.25).

- **MPU/ASIC Printed Gate Length Updated**
  - **1.6818 Etch Ratio in 2007;**
  - **Then variable Gpr/Gphy Etch Ratio (parallel to DRAM/MPU M1 Contacted Half Pitch) '07-'22.**
- **MPU/ASIC High-Performance Physical Gate Length**
  - **3.8-year cycle* beginning 2007 Performance and Power needs manage.**
  - **FEP and Litho TWGs** have agreed on new **annual variable GLprinted/GLphysical ratio targets**
  - Slower On-Chip Frequency trend (**8% trend**) was set by Design TWG in 2007 ITRS ORTC) - **need updated transistor and design model alignment by PIDS, FEP, and Design – 2009 Renewal.**
  - **New drivers will be Ion/Width, CV/I** – possibly add to ORTC - **2009 Renewal ORTC** line items.

* ITRS Cycle definition = time to .5x linear scaling every two cycle periods]

Work in Progress – Do Not Publish

ORTC Summary – **2008 Update Status (cont.)**

- **MPU/ASIC Low Operating Power Printed Gate Length**
  - **TBD**
- **MPU/ASIC Low Standby Power Physical Gate Length [add to ORTC 1a,b]**
  - **No Change 2007, 2008; two-year delay 2009-2011 from High Performance; one-year delay in 2012; and no delay 2013-2022.**

- **New 2008 "Moore's Law and More" Working Groups and Definitions Work :**
  - **"More Moore"** ("Moore's Law;" typically digital computing) Functional and Performance scaling is enabled by both "Geometrical" and also "Equivalent" scaling technologies; **Design "Equivalent Scaling" to be added in 2008**
  - **More than Moore "Functional diversification" text will be impacted** (typically non-digital sensing, interacting) system board-level migration/miniaturization is enabled by system-in-package and system-on-chip
  - **"Beyond CMOS" definition will be added, focused on the Computing and Storage Logic Switch transition and consensus options at "Ultimately Scaled CMOS"**

- The average of the industry product **"Moore's Law"** (2x functions/chip per 2 years) **rate forecast to continue** throughout the latest 2007-2022 ITRS timeframe
- **Total MOS Capacity** (SICAS) **growing at >16% CAGR** (SICAS); **new "<80nm" data split** out; and **300mm Capacity Demand has ramped to over 40%** of Total MOS
- Industry **Technology Capacity Demand** (SICAS) – 1Q08 published status] **continues on a on 2-year cycle* rate** at the leading edge.

* ITRS Cycle definition = time to .5x linear scaling every two cycle periods]

Work in Progress – Do Not Publish

Backup

- Function Size; Moore's Law on track
- Design Frequency (2007)
- SICAS Update (1Q08 data)
- Definitions

Work in Progress – Do Not Publish

Figure 9['07] ITRS Product Function Size

2008 Update:
[NO CHANGE to MPU and Flash; Small change '07-'09 to DRAM]

2007 ITRS Product Function Size Trends - Cell Size, Logic Gate(4t) Size

Past ←→ Future

Logic Gate: NO Design Area Factor Improvement (Only Scaling)

SRAM: gradual Design Area Factor Improvement

DRAM - Small Adjustments In 2008

DRAM 6f2 Pull-in to '06

DRAM: 6f² is last Design Area Factor Improvement

Flash: 4f² Last Design Physical Area Factor Improvement

Flash cell area Reduced due to 2YR cycle Extension

Flash: (MLC @ 2 bits/cell = 2f² Equivalent Area Factor)

Flash 4 bits/cell 1f² Beginning 2010

Cell, Logic Gate Size (um2)

1.E+01, 1.E+00, 1.E-01, 1.E-02, 1.E-03, 1.E-04

2000, 2005, 2010, 2015, 2020, 2025

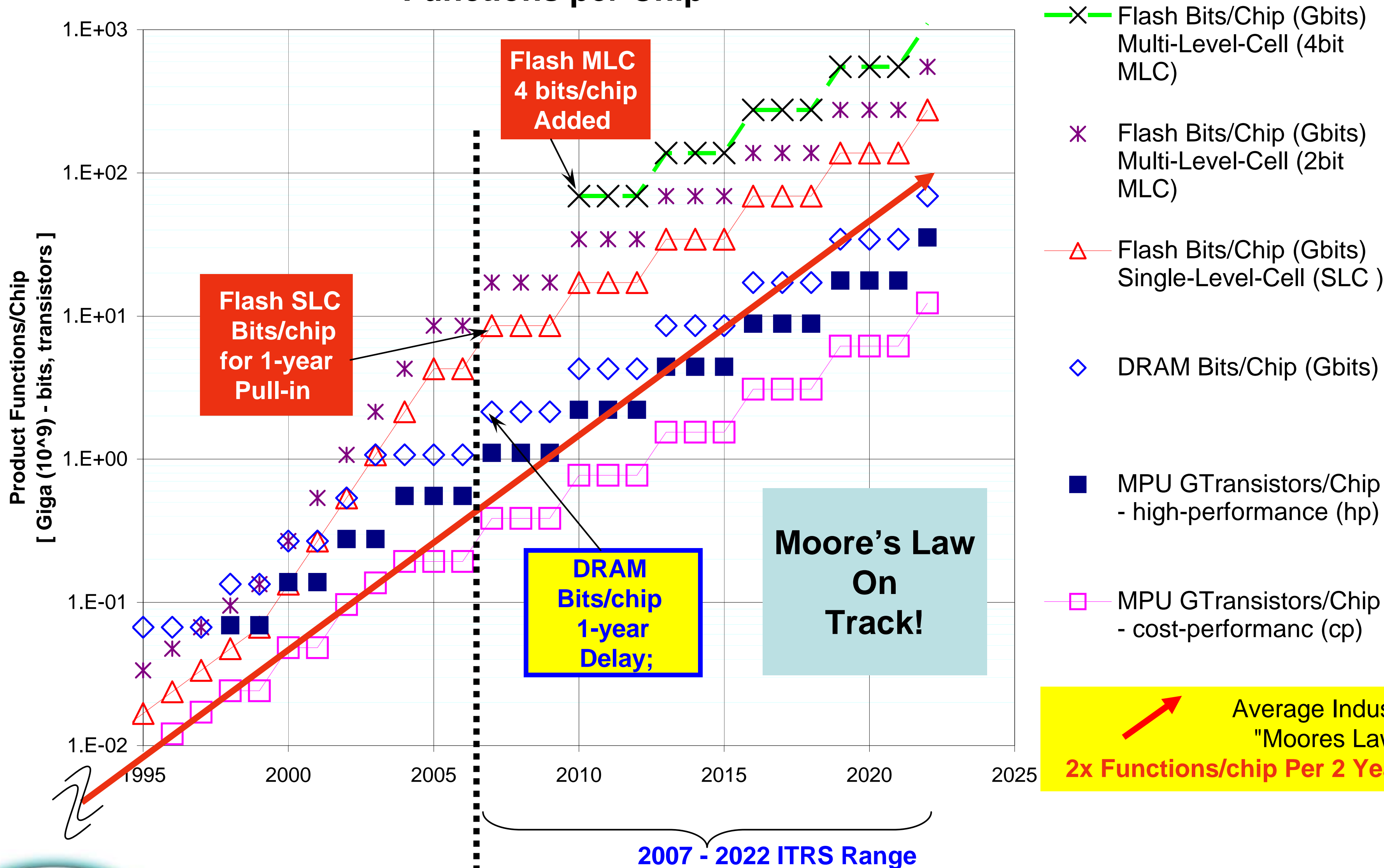
Year of Production

- DRAM Cell Size (u2)
- MPU SRAM Cell Size (6t)(u2)
- MPU Gate Size (4t)(u2)
- Flash Cell Size (u2) SLC
- Flash Eqv.bit Size(u2) 2bit MLC (@ 2 MLC bits/physical cell area)
- Flash Eqv.bit Size(u2) 4bit MLC - New (@ 4 MLC bits/physical cell area)

2007 - 2022 ITRS Range

Work in Progress – Do Not Publish

Figure 10 ITRS Product Functions per Chip



Past ← → Future

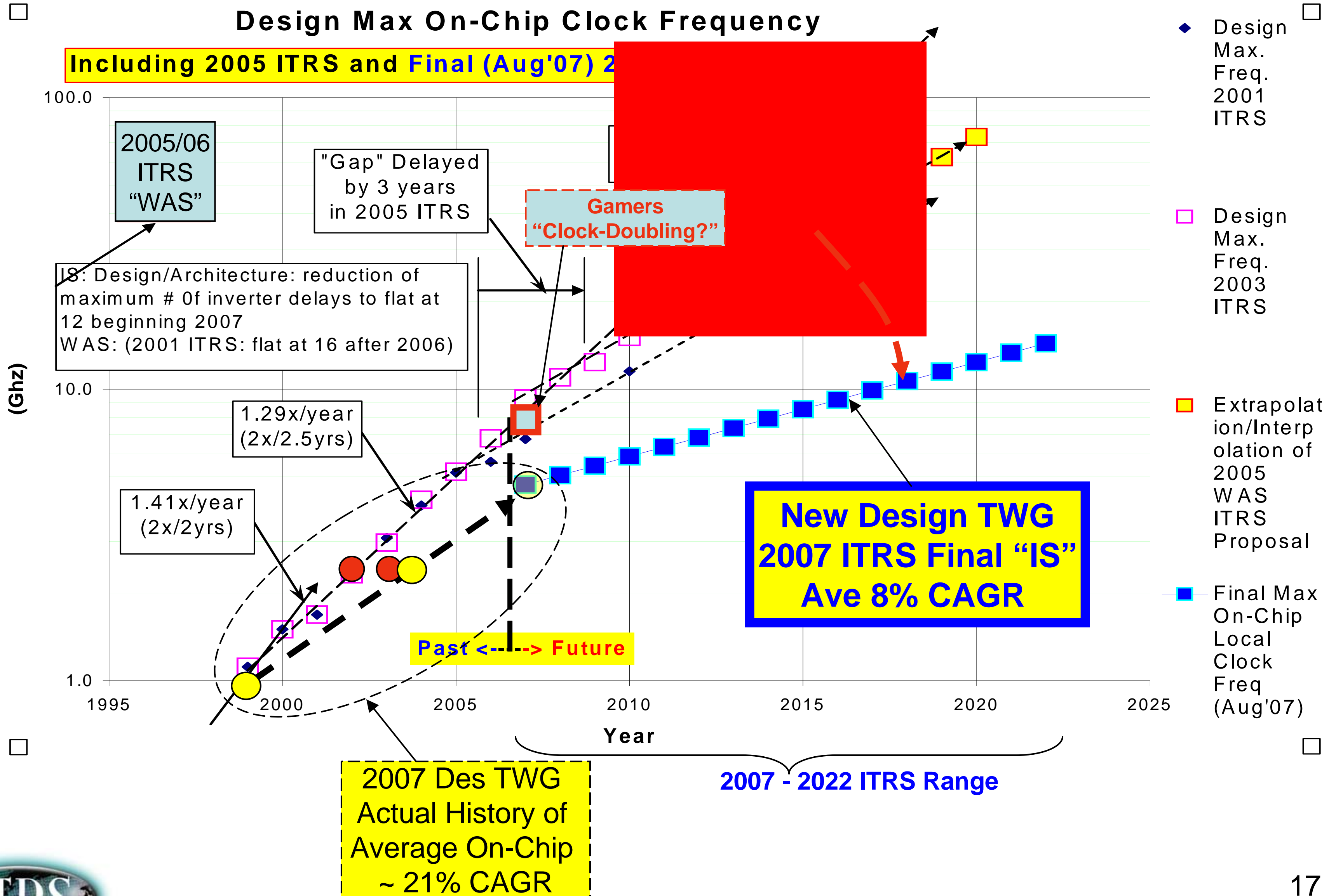
Work in Progress – Do Not Publish

New Design TWG 2007 ITRS Frequency Historical Data vs 2005 ITRS And Proposed* Trend Ave ~8% CAGR

* Source: Various, per ITRS Design TWG ca August 2007

Work in Progress – Do Not Publish

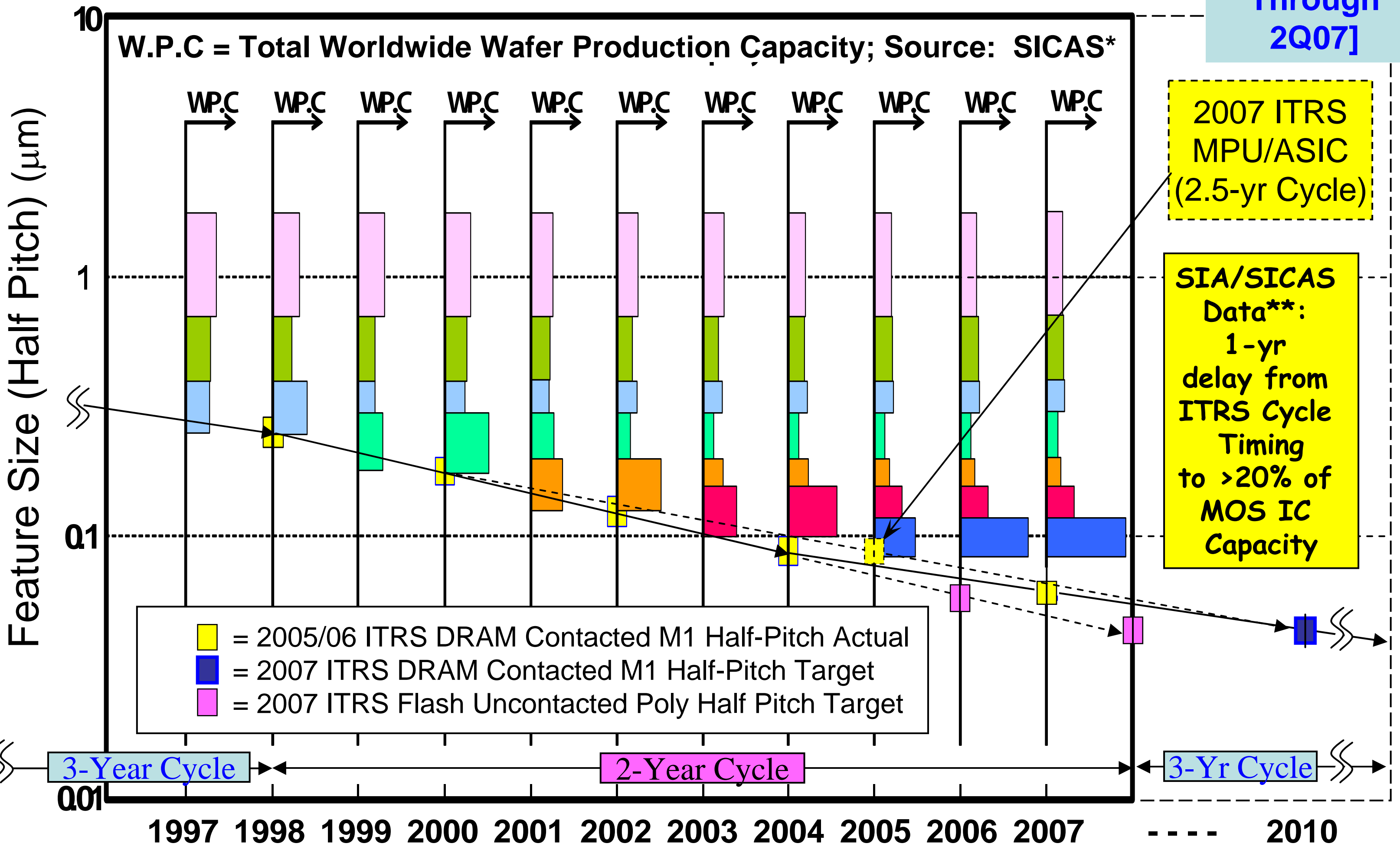
Performance and Power Management Enabled by "Equivalent Scaling"



Work in Progress – Do Not Publish

2007 “Fig 4” Technology Cycle Timing Compared to Actual Wafer Production Technology Capacity Distribution

[Updated Through 2Q07]



ITRS Technology Cycle

Range	ITRS Technology Cycle
>0.7μm	720nm
0.7-0.4μm	510nm
0.4-0.3μm	360nm
0.3- 0.2μm	255nm
0.2- 0.16μm	180nm
0.16-.12μm	127nm
<0.12μm	90nm

Note: Includes <80nm split-out (ITRS 65nm) to be added In the 2008 ITRS Upcate

Note: The wafer production capacity data are plotted from the Semiconductor Industry Association (SIA) Semiconductor Industry Capacity Statistics (SICAS) 4Q data for each year, except 2Q data for 2007.
The width of each of the production capacity bar corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.

** *Source: The data for the graphical analysis were supplied by the Semiconductor Industry Association (SIA) from their Semiconductor Industry Capacity Statistics (SICAS). The SICAS data is collected from worldwide semiconductor manufacturers (estimated >90% of Total MOS Capacity) and published by the Semiconductor Industry Association (SIA), as of August, 2007. The detailed data are available to the public online at the SIA website, http://www.sia-online.org/pre_stat.cfm .*

SICAS 1Q08 Update (www.sia-online.org)

MOS Capacity by Dimensions

WSpW x1000

100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

2Q 05 | 3Q 05 | 4Q 05 | 1Q 06 | 2Q 06 | 3Q 06 | 4Q 06 | 1Q 07 | 2Q 07 | 3Q 07 | 4Q 07 | 1Q 08

~33%

~33%

2yr Cycle

>=0.7μ
<0.7μ >=0.4μ
<0.4μ >=0.3μ
<0.3μ >=0.2μ
<0.2μ >=0.16μ
<0.16μ >=0.12μ
<0.12μ
<0.12μ >=0.08μ
<0.08μ

~0.7x

Work in Progress – Do Not Publish

SICAS 1Q08 Update (www.sia-online.org)

MOS Capacity by Wafer-size

>16% CAGR

~27Bcm2

~39Bcm2

~4Bcm2/16%

~5Bcm2/14%

~17Bcm2/62%

~18Bcm2/46%

~6Bcm2/22%

~16Bcm2/41%

WSpW x1000 (8 inch equivalents)

100%, 90%, 80%, 70%, 60%, 50%, 40%, 30%, 20%, 10%, 0%

2Q 05, 3Q 05, 4Q 05, 1Q 06, 2Q 06, 3Q 06, 4Q 06, 1Q 07, 2Q 07, 3Q 07, 4Q 07, 1Q 08

< 200m

200m

300m

Work in Progress – Do Not Publish

2007 ITRS Definitions: “More Moore” and “More than Moore”

1. **Scaling (“More Moore”)**
    a. **Geometrical (constant field) Scaling** refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
    b. **Equivalent Scaling** which occurs in conjunction with, and also enables, continued Geometrical Scaling, refers to 3-dimensional device structure (“Design Factor”) Improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.

2. **Functional Diversification (“More than Moore”)**

    Functional Diversification refers to the incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (*e.g.* RF communication, power control, passive components, sensors, actuators) **to migrate from the system board-level** into a particular package-level (SiP) or chip-level (SoC) potential solution.

ORTC Summary – 2008 Update Status

Design TWG Proposed "More Moore" and "MtM" Text, 3 Apr 2008 Plenary v2a [discussion leader – Andrew Kahng] – Proposal accepted at Koenigswinter.

- **1 = More Moore**
  - 1a = geometric scaling
  - 1b = equivalent scaling
  - **1c = Design equivalent scaling**
  - NEED: quantifiable, specific Design Technologies that deal with More Moore
  - "Design equivalent scaling occurs in conjunction with Equivalent Scaling and continued Geometric Scaling, and refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity."
  - "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-VDD, ...); and homogeneous and heterogeneous multicore SOC architectures."
  - Request: Please remove "b) Multi-core MPU architecture" from 2 (MTM Functional Diversification)
- **2 = More than Moore**
  - NEED: Design technologies to enable functional diversification
  - "Design technologies enable new functionality that takes advantage of More than Moore technologies."
  - "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology."

“Beyond CMOS” Definition

“Beyond CMOS” refers to emerging research devices, focused on a “new switch*” used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc.

***The “New Switch” refers to an “information processing element or technology”, which is associated with compatible storage or memory and interconnect functions.**

Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switch, NEMS switches, etc.