Interconnect Working Group

2008 Draft Edition
16 July 2008
SEMICON
San Francisco

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Agenda

- Scope, structure and 10 year synopsis
- Technology requirements
- Difficult challenges
- Cu resistivity effects
- Energy and performance
- Low κ roadmap
- Interconnect for memory
  - DRAM wiring roadmap
  - Non-volatile interconnect requirements
- Beyond metal/dielectric systems
  - 3D, optical and carbon nanotubes (CNT)
  - 3D roadmap proposal
- Last words

Interconnect scope

- Conductors and dielectrics
  - Starts at contact
  - Metal 1 through global levels
  - Includes the pre-metal dielectric (PMD)
- Associated planarization
- Necessary etch, strip and cleans
- Embedded passives
- Reliability and system and performance issues
- Ends at the top wiring bond pads
- “Needs” based replaced by – scaled, equivalently scaled or functional diversity drivers

Typical MPU cross section

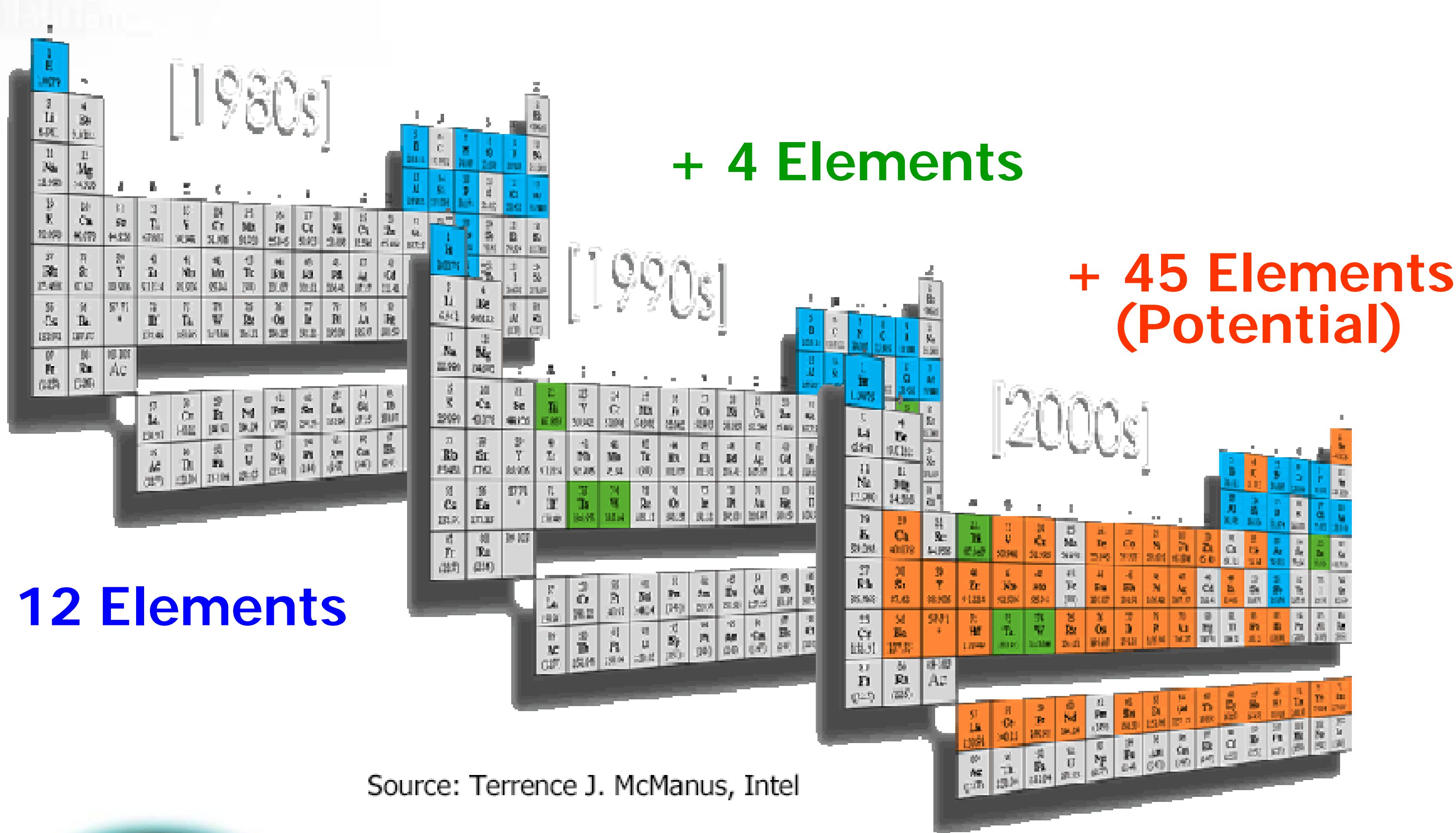
Technology Requirements (1/2)

- Tables for HP MPU and ASIC plus DRAM
- Wiring levels including "optional levels"
- Reliability metrics
- Minimum wiring/via pitches by level
- Performance figure of merit and capacitance
- Planarization requirements
- Conductor resistivity with and without scattering
- Barrier thickness
- Dielectric metrics including effective k (UPDATED)
- Crosstalk metric
- Metal 1 variability due to CD and scattering
- Power Index

Technology Requirements (2/2)

- Now restated and organized as
  - **General requirements**
    - Resistivity
    - Dielectric constant
    - Metal levels
    - Reliability metrics
  - **Level specific requirements** (M1, intermediate, global)
    - Geometrical
      - Via size and aspect ratio
      - Barrier/cladding thickness
      - Planarization specs
    - Materials requirements
      - Conductor effective resistivity and scattering effects
    - Electrical characteristics
      - Delay, capacitance

The March of Materials



Difficult challenges (1 of 3)

- *Meeting the requirements of **scaled** metal/dielectric systems*
  - Managing RC delay and power
    - New dielectrics (including air gap)
    - Controlling conductivity (liners and scattering)
  - Filling small features
    - Liners
    - Conductor deposition
  - Reliability
    - Electrical and thermo-mechanical
- Engineering a manufacturable interconnect stack compatible with new materials and processes
  - Defects
  - Metrology
  - Variability

Difficult challenges (2 of 3)

- *Meeting the requirements with **equivalent scaling***
  - Interconnect design and architecture (includes multi-core benefits)
  - Alternative metal/dielectric assemblies
    - 3D with TSV
  - Interconnects beyond metal/dielectrics
    - 3D
    - Optical wiring
    - CNT/Graphene
  - Reliability
    - Electrical and thermo-mechanical
- Engineering a CMOS-compatible manufacturable interconnect system
  - Non-traditional materials (for optical, CNT etc.)
  - Unique metrology (alignment, chirality measurements, turning radius etc)

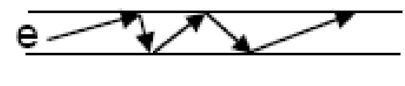
Difficult challenges (3 of 3)

- *Adding **functional diversity***
  - Mixed technologies
    - Si, GaAs, HgCdTe together
  - Mixed signalling approaches
    - RF
    - Passive devices
  - *Intelligent Interconnect* (active devices, sensors, MEMS, biochips, fluidics, etc. in interconnect)
    - Repeaters in interconnect, combined metallic/semiconducting CNT interconnects
    - Back-end memory
    - Variable resistor via
  - Reliability
    - Electrical and thermo-mechanical
- Engineering a CMOS-compatible manufacturable interconnect system
  - Non-traditional materials III/V, II/VI
  - Deposition (low temperature epi)
  - Unique metrology (composition)

Size matters

- 2003 – the impending impact of Cu resistivity increases at reduced feature sizes (due to scattering) - first noted
- 2004 – metrics introduced to highlight the impact of width dependent scattering on the effective resistivity and impact on RC delay
  - Models have been refined to more accurately predict the resistivity due to changes in aspect ratio, shape and metal thickness
- 2007 - Metrics updated – managed architecture
- Adapt the same methodology for DRAM when Cu is introduced (2007)

Bulk scattering



Surface scattering

Size matters

Resistivity [μΩ cm]

5
4
3
2
1
0

side wall

grain boundary

bulk resistivity

10
100
1000

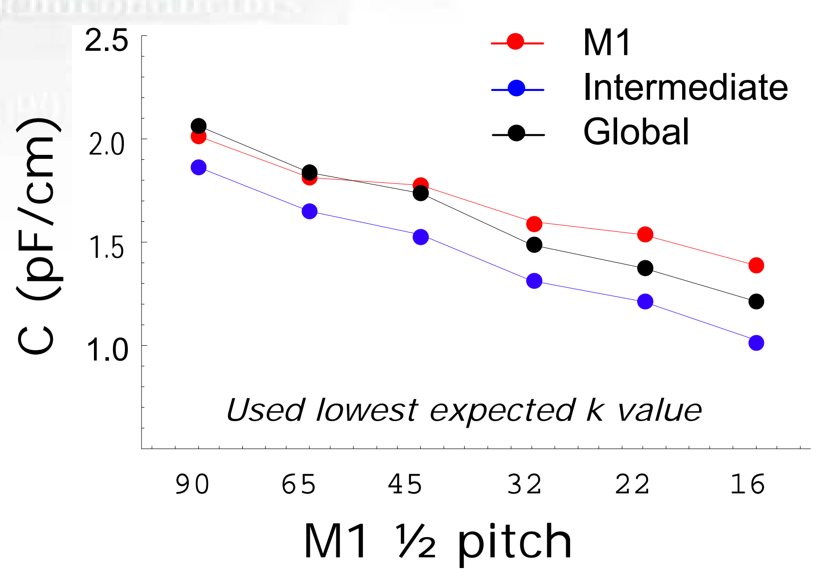
Linewidth (nm)

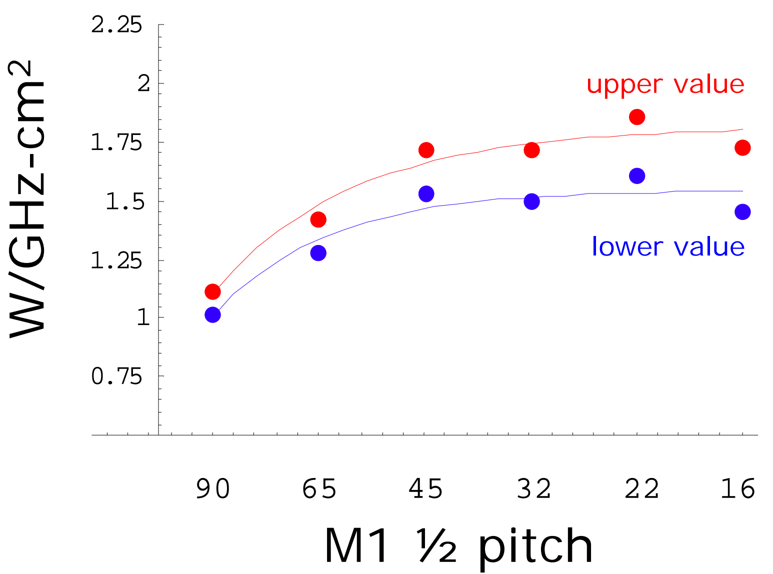
Figure From Infineon

Dynamic Power

- Increasing concern about rising dynamic power in the interconnect stack
  - Interconnects make a significant contribution to total dynamic power
- Impacts effective k roadmap
  - Drives reduction in parasitic capacitance
- Dynamic power is a key constraint for high performance MPUs
- Alternative interconnect technologies (optical, CNT, RF, etc.) should be performance competitive in terms of delay and power
- Influence of number of functions (N), activity (A) and frequency (F): $P = (NAF)CV^2$

Capacitance and Power Index





$$P_{layer}\left[\frac{W}{GHz-cm^2}\right] = C \cdot V^2 \cdot a \cdot (1\ GHz) \cdot \left(e_w \cdot \frac{1\ cm^2}{p}\right) = \text{Power per GHz per cm}^2 \text{ of metal layer.}$$

C = capacitance per unit length.

$V = V_{dd}$, p = pitch, e_w = wiring efficiency, a = average activity factor of interconnects.

Table 80a ("*MPU and ASIC Interconnect Technology Requirements—Near-term Years*")

M1_half_pitch	65	59	52	45	40	36	32	28	25
Power index ($W/GHz\text{-}cm^2$) [x]	1.4-1.6	1.4-1.6	1.4-1.6	1.6-1.8	1.8-2.0	1.6-1.8	1.7-2.0	2.0-2.3	1.5-1.8

Power index = $C\,V_{dd}^2\,a\,(1\ GHz)\,e_w\,(1\ cm^2)/p$; p = pitch; V_{dd} = supply voltage; e_w = wiring efficiency = 1/3; a = activity factor = 0.03.

The calculated values are an approximation for the "power per GHz per cm^2 of metallization layer".

This index scales with the critical parameters that determine the interconnect dynamic power.

NOTES: the values provided are an average for M1, Intermediate and Global interconnects. The range of values results from the maximum and minimum effective dielectric constants.

R and C variability

Effect of few % variations in different variability sources

(Speed) RC [s/mm2] vs. (Energy) C [F/mm]

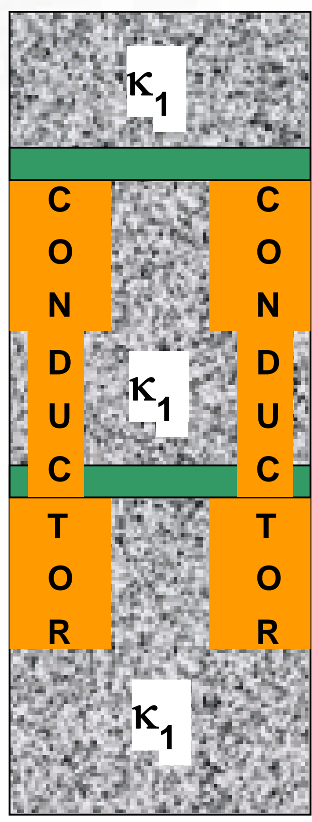
Y axis: 0.00E+00, 2.00E-10, 4.00E-10, 6.00E-10, 8.00E-10, 1.00E-09, 1.20E-09, 1.40E-09

X axis: 1.00E-13, 1.20E-13, 1.40E-13, 1.60E-13, 1.80E-13, 2.00E-13, 2.20E-13

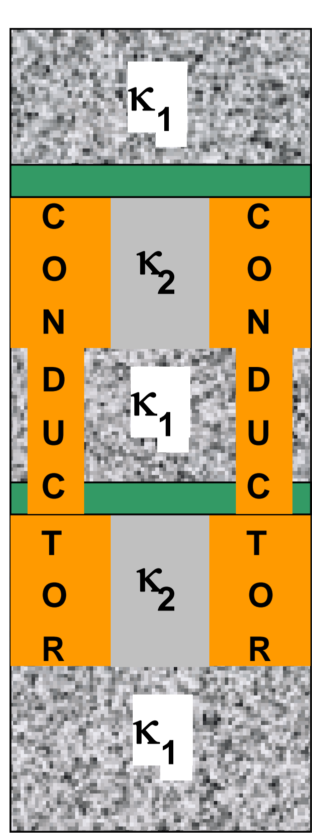
Annotations: w=80nm t =70nm; w=80nm t =150nm; w=100nm t =200nm; w=250nm t =200nm

Metal width	± 6nm
Metal thk	± 4nm
Barrier thk	± 2nm
Keff	± 0.1
ILD thk	± 4nm

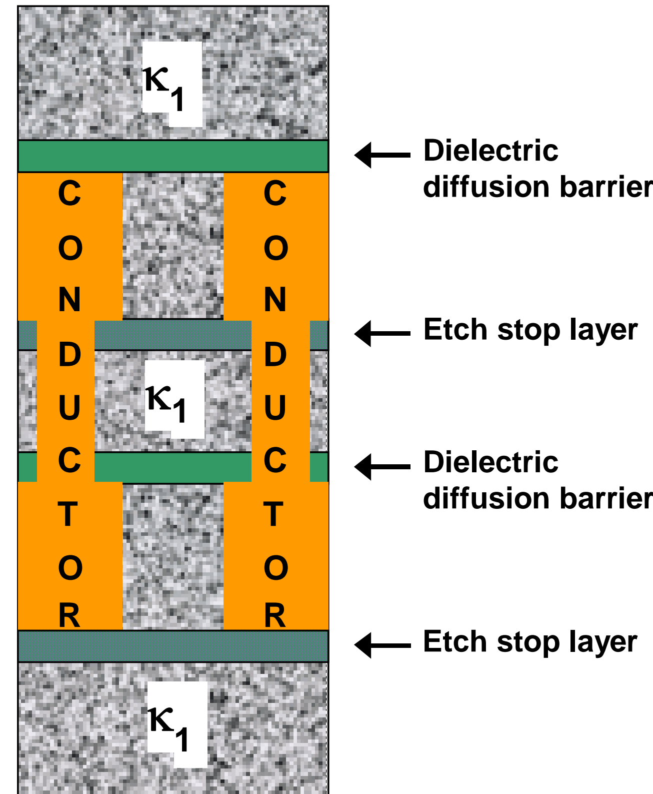
Integration Schemes



Homogeneous ILD
without trench etch stop



Embedded low κ ILD
($\kappa_1 > \kappa_2$)



Homogeneous ILD
with trench etch stop

Low-k Trend from Conference Papers (2003-2007 IITC, IEDM, VL, AMC)

Company	90 nm	65 nm	45 nm	32nm
I	CVD SiOC DD (k=2.9)	CVD SiOC DD (k=2.9)	–	–
I	CVD SiOC DD (k=3.0)	CVD SiOC DD (k=2.75)	CVD SiOC DD (k=2.45)	–
T	CVD SiOC DD (k=3.0)	CVD SiOC DD (k=2.7)	CVD SiOC DD (k=2.55)?	CVD SiOC DD (k=2.2-2.3)?
R	CVD SiOC DD (k=2.9)	CVD SiOC stack DD (k=2.6/3.0)	CVD SiOC DD (k=2.65)	–
F	CVD SiOC DD (k=2.9)	NCS/CVD SiOC stack DD (k=2.25/2.9)	NCS/NCS stack DD (k=2.25/2.25)	NCS/NCS stack DD (k=2.25/2.25)?
T	CVD SiOC DD (k=2.9)	PAr/SiOC hybrid DD (k=2.6/2.5)	P-PAr/p-SiOC hybrid DD (k=2.3/2.3)	ULK-PAr/SiOC hybrid DD (k=2.0/2.0)

Slow down of low-k technology development speed and large variation of k values among device companies

Actual Low-k Trend from Introduction in Manufacturing

	90 nm	65 nm	45 nm	32nm
	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=2.55)? →	CVD SiOC DD (k=2.2-2.3)?
	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=2.8) →	CVD SiOC DD (k=2.6)
	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=2.8) →	CVD SiOC DD (k=2.4)
	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=2.75) →	CVD SiOC DD (k=2.4)
	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=2.75) →	CVD SiOC DD (k=2.4)
	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=3.0) →	CVD SiOC DD (k=2.8) →	CVD SiOC DD (k=2.4)?

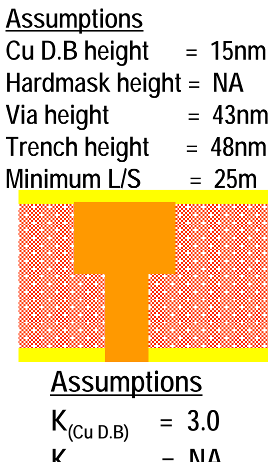
Actual introduction in manufacturing of low-k material is one generation delayed and a variation of bulk k range among device makers is narrowing compared with trend from conference papers

Progress – Do Not Publish

Bulk k Value Update for ITRS2008 (Realistic Case)

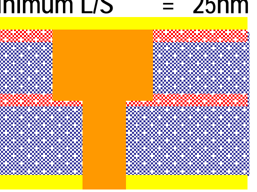
< 2015,2016,2017 >

Assumptions
Cu D.B height = 15nm
Hardmask height = NA
Via height = 43nm
Trench height = 48nm
Minimum L/S = 25m



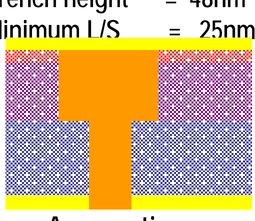
Assumptions
$K_{(Cu\ D.B)}$ = 3.0
$K_{(Hardmask)}$ = NA
$K_{(via)}$ = 2.2(-0.1)
$K_{(trench)}$ = 2.2(-0.1)
K_{eff} =2.36(2.48)

Assumptions
Cu D.B height = 15nm
Hardmask height = 15nm
Via height = 43nm
Trench height = 48m
Minimum L/S = 25nm



Assumptions
$K_{(Cu\ D.B)}$ = 3.0
$K_{(Hardmask)}$ = 2.4
$K_{(via)}$ = 2.1
$K_{(trench)}$ = 2.1
$K_{(Middle-STP)}$ = 3.0
K_{eff} =2.50

Assumptions
Cu D.B height = 15nm
Hardmask height = 15nm
Via height = 43nm
Trench height = 48nm
Minimum L/S = 25nm



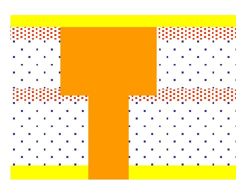
Assumptions
$K_{(Cu\ D.B)}$ = 3.0
$K_{(Hardmask)}$ = 2.4
$K_{(via)}$ = 2.1
$K_{(trench)}$ = 2.1
K_{eff} =2.40

< 2018,2019,2020 >

Assumptions
Cu D.B height = 10nm
Hardmask height = NA
Via height = 32nm
Trench height = 36nm
Minimum L/S = 18nm

Assumptions
$K_{(Cu\ D.B)}$ = 2.6
$K_{(Hardmask)}$ = NA
$K_{(via)}$ = 2.0 (-0.1)
$K_{(trench)}$ = 2.0 (-0.1)
K_{eff} =2.12(2.27)

Assumptions
Cu D.B height = 10nm
Hardmask height = 10nm
Via height = 32nm
Trench height = 36nm
Minimum L/S = 18nm



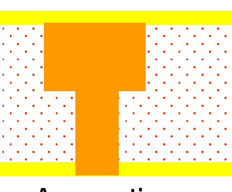
Assumptions
$K_{(Cu\ D.B)}$ = 2.6
$K_{(Hardmask)}$ = 2.3
$K_{(via)}$ = 1.9
$K_{(trench)}$ = 1.9
$K_{(Middle-STP)}$ = 2.6
K_{eff} =2.27

Assumptions
Cu D.B height = 10nm
Hardmask height = 10nm
Via height = 32nm
Trench height = 36nm
Minimum L/S = 18nm

Assumptions
$K_{(Cu\ D.B)}$ = 2.6
$K_{(Hardmask)}$ = 2.3
$K_{(via)}$ = 1.9
$K_{(trench)}$ = 1.9
K_{eff} =2.20

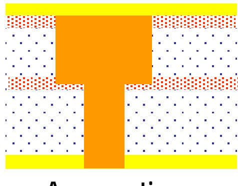
< 2021,2022,2023 >

Assumptions
Cu D.B height = 7nm
Hardmask height = NA
Via height = 22nm
Trench height = 25nm
Minimum L/S = 13nm



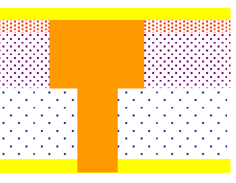
Assumptions
$K_{(Cu\ D.B)}$ = 2.4
$K_{(Hardmask)}$ = NA
$K_{(via)}$ = 1.8 (-0.1)
$K_{(trench)}$ = 1.8 (-0.1)
K_{eff} = 1.92(2.04)

Assumptions
Cu D.B height = 7nm
Hardmask height = 7nm
Via height = 22nm
Trench height = 25nm
Minimum L/S = 13nm



Assumptions
$K_{(Cu\ D.B)}$ = 2.4
$K_{(Hardmask)}$ = 2.1
$K_{(via)}$ = 1.7
$K_{(trench)}$ = 1.7
$K_{(Middle-STP)}$ = 2.4
K_{eff} =2.03

Assumptions
Cu D.B height = 7nm
Hardmask height = 7nm
Via height = 22nm
Trench height = 25nm
Minimum L/S = 13nm



Assumptions
$K_{(Cu\ D.B)}$ = 2.4
$K_{(Hardmask)}$ = 2.1
$K_{(via)}$ = 1.7
$K_{(trench)}$ = 1.7
K_{eff} = 1.96

ITRS2008 Low-k Roadmap Update

		Near-term					
	Year of Production	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*
Was	Interlevel metal insulator – effective dielectric constant (κ)	2.7-3.0	2.5-2.8	2.5-2.8	2.5-2.8	2.1-2.4	2.1-2.4
Is	Interlevel metal insulator – effective dielectric constant (κ)	2.9-3.3	2.6-2.9	2.6-2.9	2.6-2.9	2.4-2.8	2.4-2.8
Was	Interlevel metal insulator – bulk dielectric constant (κ)	2.3-2.7	2.1-2.4	2.1-2.4	2.1-2.4	1.8-2.1	1.8-2.1
Is	Interlevel metal insulator – bulk dielectric constant (κ)	2.5-2.8	2.3-2.6	2.3-2.6	2.3-2.6	2.1-2.4	2.1-2.4
Is	Copper diffusion barrier and etch-stopper - bulk dielectric constant (κ)	4.0-4.5	3.5-4.0	3.5-4.0	3.5-4.0	3.0-3.5	3.0-3.5

Long-term									
2014	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*
2.1-2.4	1.9-2.2	1.9-2.2	1.9-2.2	1.6-1.9	1.6-1.9	1.6-1.9			
2.4-2.8	2.1-2.5	2.1-2.5	2.1-2.5	2.0-2.3	2.0-2.3	2.0-2.3	1.7-2.0	1.7-2.0	1.7-2.0
1.8-2.1	1.6-1.9	1.6-1.9	1.6-1.9	1.4-1.7	1.4-1.7	1.4-1.7			
2.1-2.4	1.9-2.2	1.9-2.2	1.9-2.2	1.7-2.0	1.7-2.0	1.7-2.0	1.5-1.8	1.5-1.8	1.5-1.8
3.0-3.5	2.6-3.0	2.6-3.0	2.6-3.0	2.4-2.6	2.4-2.6	2.4-2.6	2.1-2.4	2.1-2.4	2.1-2.4

Change maximum bulk k value from 2.9 to 2.8 corresponding to 45nm actual introduction in manufacturing of low-k material.

2.5-2.9 → 2.5-2.8 @2007-2008

Beyond 2009, decrease maximum bulk k value by 0.1.

2.3-2.7 → 2.3-2.6 @2009-2011
2.1-2.5 → 2.1-2.4 @2012-2014
1.9-2.3 → 1.9-2.2 @2015-2017
1.7-2.1 → 1.7-2.0 @2018-2020
1.5-1.9 → 1.5-1.8 @2021-2023

Historical Transition of ITRS Low-k Roadmap

DRAM

Small changes in specific via and contact resistivity

Contact A/R (stacked capacitor) rises to >20 in 2010 - a nearby red challenge - associated with the 45 nm DRAM half pitch

Cu implemented in 2007

Low k with an effective dielectric constant of 3.1 – 3.4 pushed back one year to 2009

Plan to distinguish embedded, flash, and traditional DRAM along with alternative memory in the interconnect in the future (2009)

Revised Aspect Ratio of DRAM

Table INTC3a DRAM Interconnect Technology Requirements—Nea

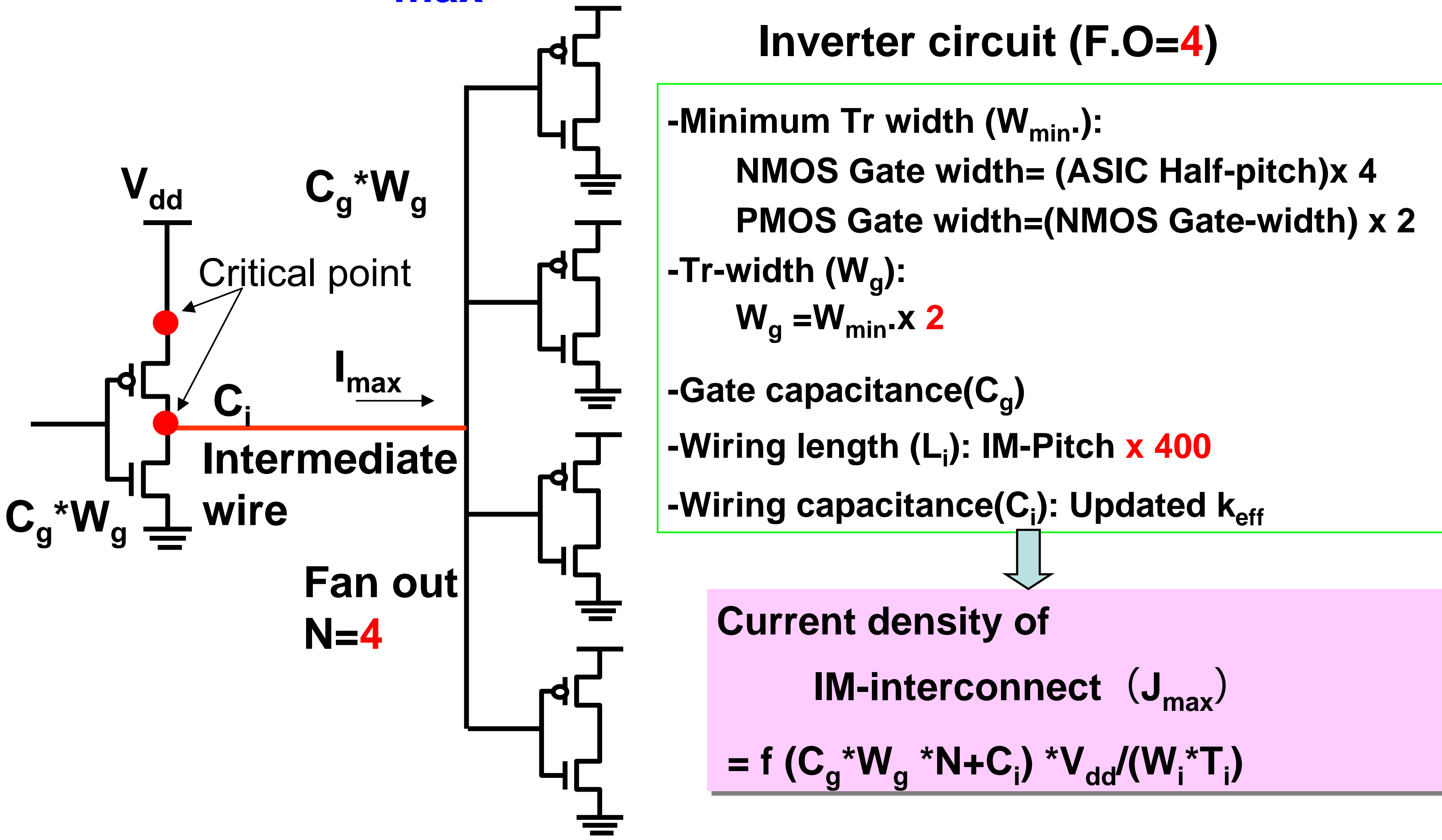
Year of Production	2007	2008	2009	2010	2011	2012
DRAM ½ Pitch (nm) (contacted)	65	57	50	45	40	36
Number of metal layers	4	4	4	4	4	4
Contact A/R – stacked capacitor	18	18	29	29	31	33
Metal 1 wiring pitch (nm)*	130	114	100	90	80	72
Specific contact resistance (Ω-cm^2) for n+ Si	2.00E-08	1.70E-08	1.40E-08	1.20E-08	9.80E-09	8.20E-09
Specific contact resistance (Ω-cm^2) for p+ Si	3.20E-08	2.70E-08	2.20E-08	1.80E-08	1.50E-08	1.30E-08
Specific via resistance (Ω-cm^2)	5.00E-10	4.00E-10	3.50E-10	2.90E-10	2.50E-10	2.10E-10

Table FEP5a DRAM Stacked Capacitor Technology Requirements—Near-term Years

Year of Production	2007	2008	2009	2010	2011	2012
DRAM ½ Pitch (nm) [A]	65	57	50	45	40	
Cell size factor a [B]	6	6	6	6	6	6
t_{eq} at 25fF (nm) [G]	1.15	0.9	0.8	0.6	0.5	0.4
Dielectric constant	40	43	49	65	78	98
SN height (μm)	1.4	1.3	1.9	1.6	1.5	1.3
t_{phy}. at 25fF (nm) [H]	11.8	10.0	10.0	10.0	10.0	10.0
A/R of SN [I]	21.6	22.0	38.3	35.4	37.4	36.9
A/R of SN (OUT) for cell plate deposition [I]	33.8	33.8	63.8	63.8	74.7	83.0
HAC diameter (μm) [J]	0.12	0.11	0.9	0.08	0.07	0.06
Total interlevel insulator and metal thickness except SN (μm) [K]	0.78	0.75	0.73	0.7	0.68	0.66
HAC depth (μm) [L]	2.2	2.0	2.6	2.3	2.2	2.0
HAC A/R	18	18	29	29	31	33

New proposal from Kore

J_{max} Calculation Model



J_{max} is a metric for EM reliability. The model for its estimation has basically been the same since 1999. But the parameters are updated in accordance with the realistic J_{max} value at the time of updating.

Aspect Ratio of DRAM

Nomenclature from FEP RM

Notes for Tables FEP5a and FEP5b:

[A] 2005 Overall Roadmap Technology Characteristics, Table 1a and b

[B] a = (cell size)/F^2 (F : minimum feature size)

[C] Cell size = aF^2 (cell shorter side = 2F)*

[D] SN size = (a/2 -1)F^2 (SN shorter side = F)*

[E] Cylinder structure increase the capacitor area by a factor of 1.5

[F] SC = (total capacitor area) / (cell size)

*[G] teq = 3.9*E0*(total capacitor area)/25fF*

*[H] t_{phy} = t_{eq}*E_r/3.9 If polysilicon is used as a bottom electrode. t_{phy} =(t_{eq}-1)*E_r/3.9*

[I] A/R of SN = (SN height)/F

[J] A/R of SN (OUT) = (SN height) / (F - 2 t_{phy})*

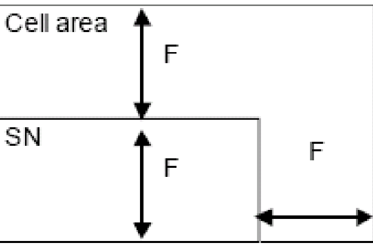
*[K] HAC diameter = 1.2*F*

[L] The thickness is assumed to be 1.05 μm at 180 nm. (10% reduction by each technology generation)

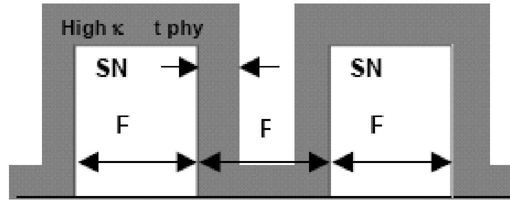
[M] HAC depth = SN height + total interlevel insulator and metal thickness

[N] DRAM retention time (PIDS)

*[O] (Sense Limit*C*V_{dd}/2)/(Retention Time * MARGIN) (Sense limit=30% leak, MARGIN=100)*



Notes[C] & [D] Cell area and Projected SN area



Note [I] A/R of SN (OUT)

DRAM low k

Table INTC3a DRAM Interconnect Technology Requirements—Near-term Years

Year of Production	*2007*	*2008*	*2009*	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
DRAM ½ Pitch (nm) (contacted)	*65*	*57*	*50*	*45*	*40*	*36*	*32*	*28*	*25*
Number of metal layers	4	4	4	4	4	4	4	4	4
Contact A/R – stacked capacitor	16	17	17	>20	>20	>20	>20	>20	>20
Metal 1 wiring pitch (nm)*	130	114	100	90	80	72	64	56	50
Specific contact resistance (Ω-cm²) for n+ Si	2.00E-08	1.70E-08	1.40E-08	1.20E-08	9.80E-09	8.20E-09	6.90E-09	5.80E-09	4.80E-09
Specific contact resistance (Ω-cm²) for p+ Si	3.20E-08	2.70E-08	2.20E-08	1.80E-08	1.50E-08	1.30E-08	1.10E-08	9.20E-09	7.40E-09
Specific via resistance (Ω-cm²)	5.00E-10	4.00E-10	3.50E-10	2.90E-10	2.50E-10	2.10E-10	1.70E-10	1.40E-10	1.20E-10
Conductor effective resistivity (μΩ-cm) assumes no scattering for Cu	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Interlevel metal insulator – effective dielectric constant (κ)	3.6–4.1	3.6–4.1	3.1–3.4	3.1-3.4	2.7–3.0	2.7–3.0	2.7–3.0	2.5–2.8	2.5–2.8

Discussion on dielectric constant value for 2009 ongoing
Question: change value to 3.6 - 4.1 ?
=> I guess major chip makers don't move to 3.1~3.4 k-value at this node.
So, I think it's reasonable to change this value to 3.6~4.1.

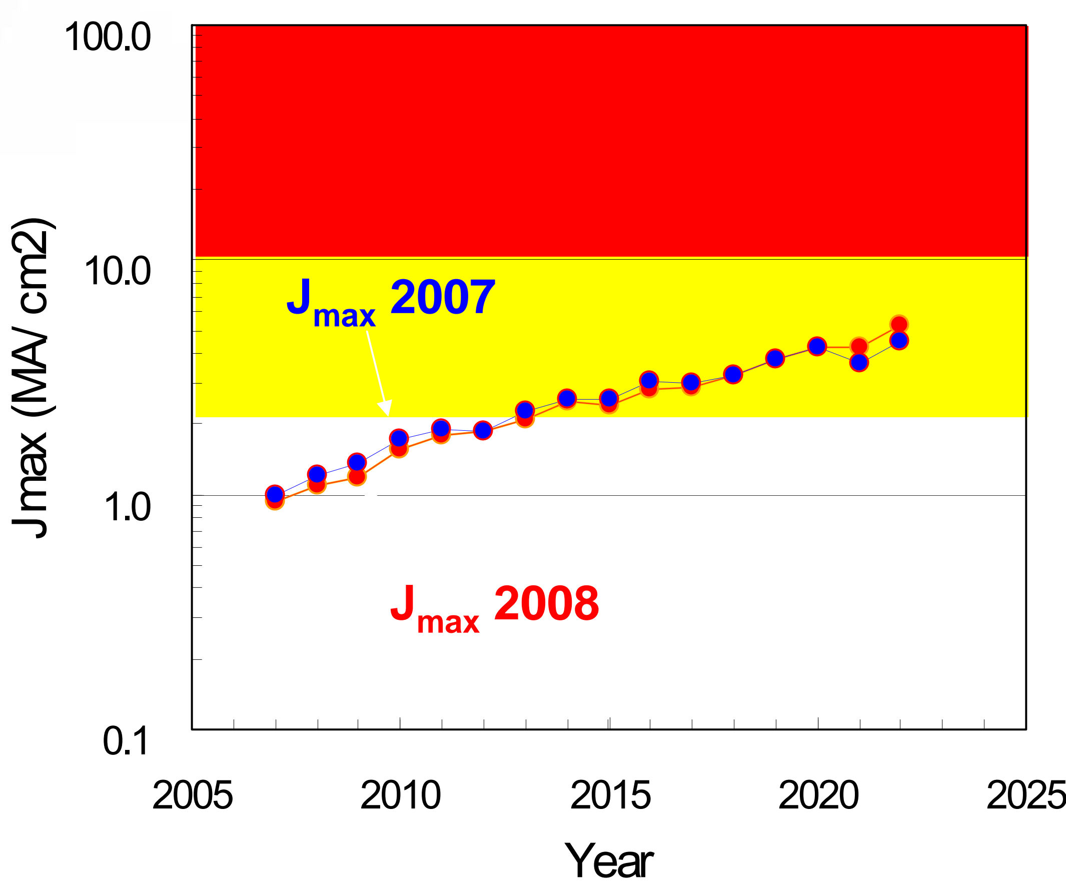
2008 DRAM Table - n^+Si, p^+Si and Via

Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022
DRAM ½ Pitch (nm) (contacted)	65	57	50	45	40	36	32	28	25	22	20	18	16	14	13	11
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	68	59	52	45	40	36	32	28	25	22	20	18	16	14	13	11
MPU Physical Gate Length (nm)	25	22	20	18	16	14	13	11	10	9	8	7	6	6		
Number of metal layers	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
Contact A/R – stacked capacitor	16	17	17	>20	>20	>20	>20	>20	>20	>20	>20	>20	>20	>20	>20	>20
Metal 1 wiring pitch (nm) *	130	114	100	90	80	72	64	56	50	44	40	36	32	28	26	22
Specific contact resistance (Ω-cm²) for n+ Si	2.00E-08	1.70E-08	1.40E-08	1.20E-08	9.80E-09	8.20E-09	6.90E-09	5.80E-09	4.80E-09	4.00E-09	3.40E-09	2.80E-09	2.34E-09	1.96E-09	1.65E-09	1.37E-09
Specific contact resistance (Ω-cm²) for p+ Si	3.20E-08	2.70E-08	2.20E-08	1.80E-08	1.50E-08	1.30E-08	1.10E-08	9.20E-09	7.40E-09	6.20E-09	5.10E-09	4.30E-09	3.60E-09	3.01E-09	2.52E-09	2.11E-09
Specific via resistance (Ω-cm²) old	5.00E-10	4.00E-10	3.50E-10	2.90E-10	2.50E-10	2.10E-10	1.70E-10	1.40E-10	1.20E-10	1.00E-10	8.40E-11	7.00E-11	5.88E-10	4.90E-10		
Specific via resistance (Ω-cm²) new	5.00E-10	4.00E-10	3.50E-10	2.90E-10	2.50E-10	2.10E-10	1.70E-10	1.40E-10	1.20E-10	1.00E-10	8.40E-11	7.00E-11	5.81E-11	4.82E-11	4.00E-11	3.32E-11
Conductor effective resistivity (μΩ-cm) assumes no scattering for Cu	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
Interlevel metal insulator – effective dielectric constant (κ) old	3.6–4.1	3.1–3.4	3.1–3.4	3.1-3.4	2.7–3.0	2.7–3.0	2.7–3.0	2.5–2.8	2.5–2.8	2.5–2.8	2.3–2.6	2.3–2.6	2.3–2.6	2.3–2.6		
Interlevel metal insulator – effective dielectric constant (κ) new	3.6–4.1	3.6–4.1	3.1–3.4	3.1-3.4	2.7–3.0	2.7–3.0	2.7–3.0	2.5–2.8	2.5–2.8	2.5–2.8	2.3–2.6	2.3–2.6	2.3–2.6	2.3–2.6	2.3–2.6	2.3–2.6

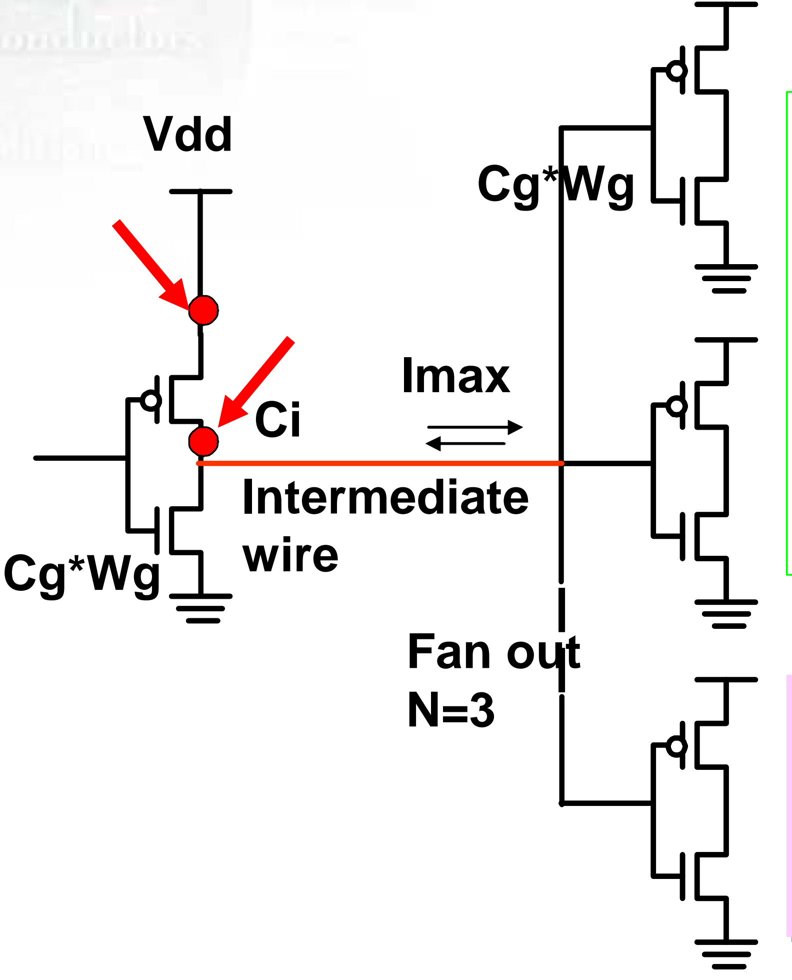
Calculated values by using the scaling factor of 0.83

1. Values for Contact and Vias are basically consistent with measured data up to 2009
2. Beyond 2009 the values are extrapolated as proposed previously by Japan TWG: Based on contact CD scaling assumption, 30 % every 2 years (factor = 0,83/year) is between compensation of width scaling (factor = 0,89/year) and area scaling (factor = 0,79/year); 30 % every 2 years is a good approach to keep the contact Rs below a certain limit.
3. Values 2010 to 2022 should stay in red

J_{max} Update - 2008



Jmax 2008



Inverter circuit (F.O=3)

- -Minimum Tr width (Wmin.):
  - NMOS Gate width= (ASIC Half-pitch)x 4
  - PMOS Gate width=(NMOS Gate-width) x 2
- -Tr-width (Wg):
  - Wg =Wmin.x 8
- -Gate capacitance(Cg)
- -Wiring length (Li): IM-Pitch x 200
- -Wiring capacitance(Ci): Updated keff

Average current density of IM-interconnect （J_{max}）

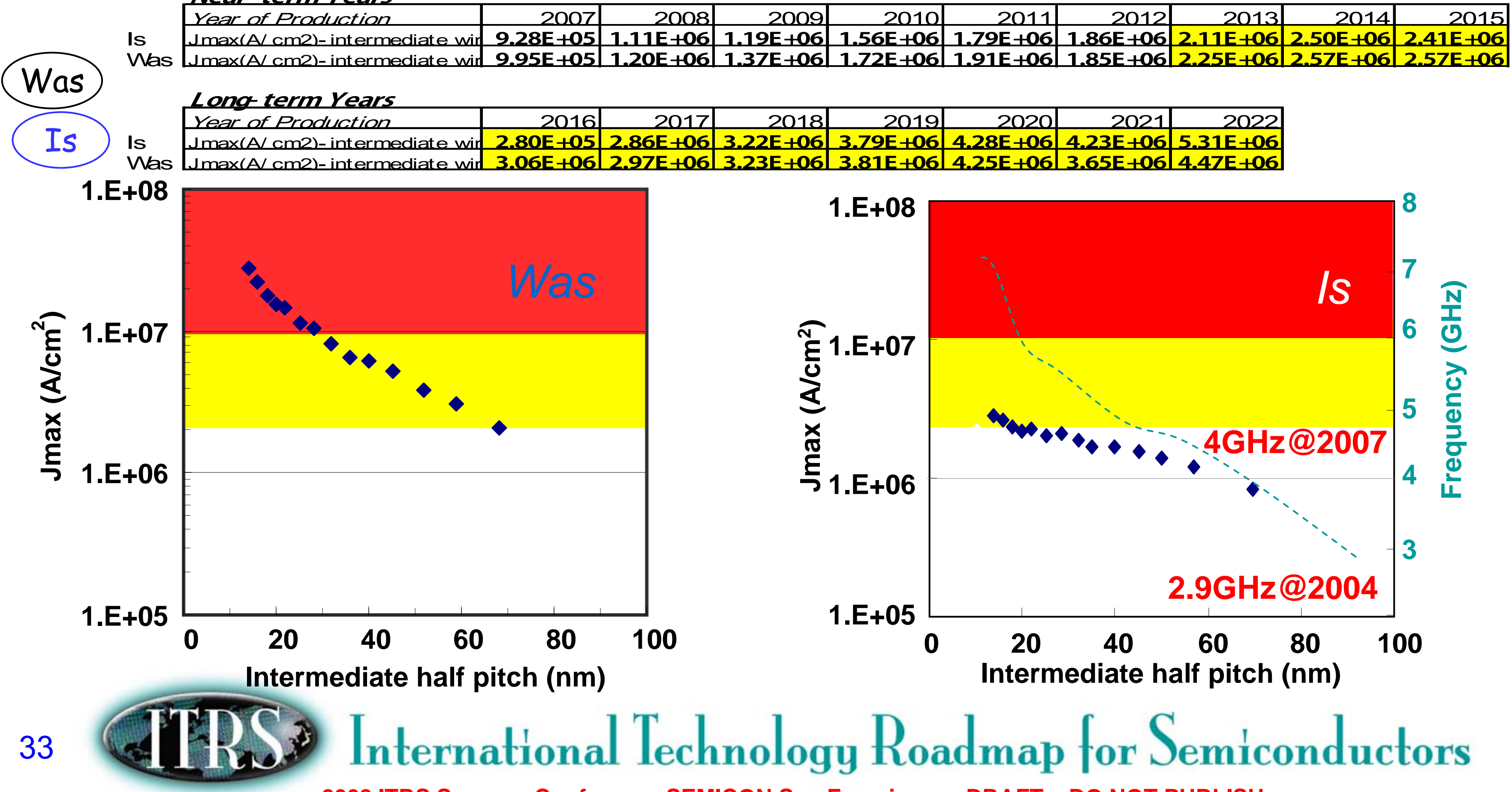
= f (Cg*Wg *N+Ci) *Vdd/(Wi*Ti)

● : Critical points for the DC pulse current, where the minimum pitch and via-size are used for high density.

International Technology Roadmap for Semiconductors

Jmax Change - Table 80

- EM improvement technologies such as **$CuSiN_x$** and **Cu-alloy** (CuAl etc.) have become manufacturable technologies.
- **More than 20 times EM lifetime** (T) improvements lead to **about 5 times Jmax** improvements assuming $T \propto J^{-2}$



Near-term Years

	Year of Production	2007	2008	2009	2010	2011	2012	2013	2014	2015
Is	Jmax(A/cm2)-intermediate wir	9.28E+05	1.11E+06	1.19E+06	1.56E+06	1.79E+06	1.86E+06	2.11E+06	2.50E+06	2.41E+06
Was	Jmax(A/cm2)-intermediate wir	9.95E+05	1.20E+06	1.37E+06	1.72E+06	1.91E+06	1.85E+06	2.25E+06	2.57E+06	2.57E+06

Long-term Years

	Year of Production	2016	2017	2018	2019	2020	2021	2022
Is	Jmax(A/cm2)-intermediate wir	2.80E+05	2.86E+06	3.22E+06	3.79E+06	4.28E+06	4.23E+06	5.31E+06
Was	Jmax(A/cm2)-intermediate wir	3.06E+06	2.97E+06	3.23E+06	3.81E+06	4.25E+06	3.65E+06	4.47E+06

Multi-core Impact on Interconnect

- Wiring lengths change
  - Critical path reduced (in core)
  - Mechanical integrity challenges will change
  - Jmax changes
  - Hierarchical structure may no longer be necessary
    - Converge to more fine pitch local/intermediate wires
    - Power and ground delivered through grid
  - Global delay challenge relaxed
  - 3D may include multi-core

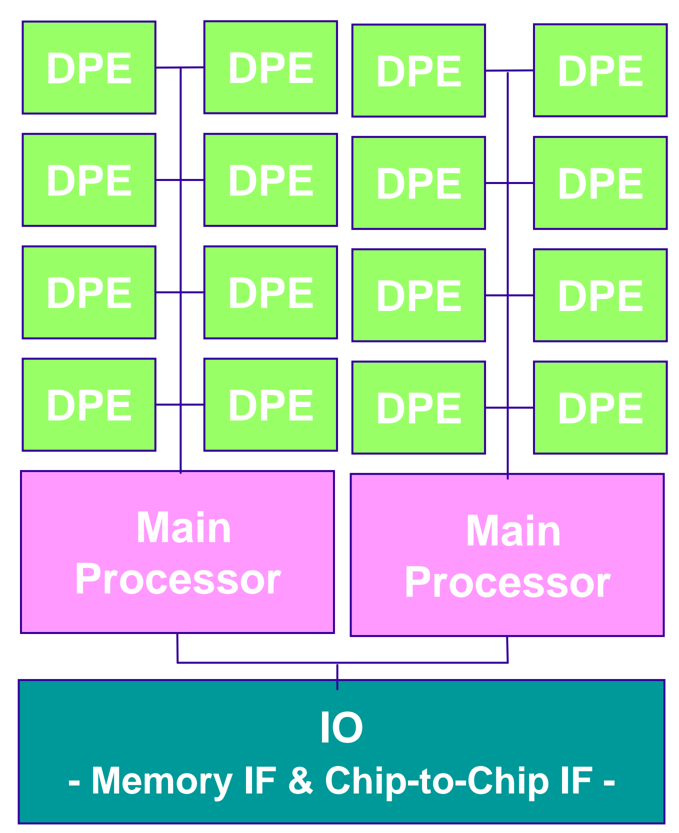


Figure From ITRS 2006 Design TWG

- Need to consider splitting metrics into:
  - In-core (intra-tile) and Inter-core (inter-tile)
    - New bandwidth requirements

Emerging Interconnect (1/2)

- Use geometry
  - 3D
  - Air gap
- Use different signaling methods
  - Signal design
  - Signal coding techniques
- Use innovative design and package options
  - Interconnect - centric design
  - Package intermediated interconnect
  - Chip-package co-design

Optical Devices
Analog/RF
Repeaters
Distributed Memory
Logic

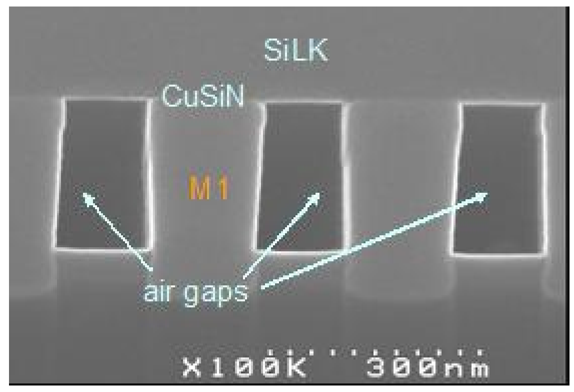
Figure From Stanford

Emerging interconnect (2/2)

- Use different physics
  - Optics (waveguides, emitters, detectors, free space, trans-impedance amps, modulators)
  - RF/microwaves (transmitters, receivers, free space, waveguides)
  - Terahertz photonics
- Radical solutions
  - Nanowires/nanotubes/graphene
  - Molecules
  - Spintronics
  - Quantum wave functions

From low-κ to no κ - air gaps

- Introduction of air gap architectures
  - Creation of air gaps with non-conformal deposition
  - Removal of sacrificial materials after multi-level interconnects

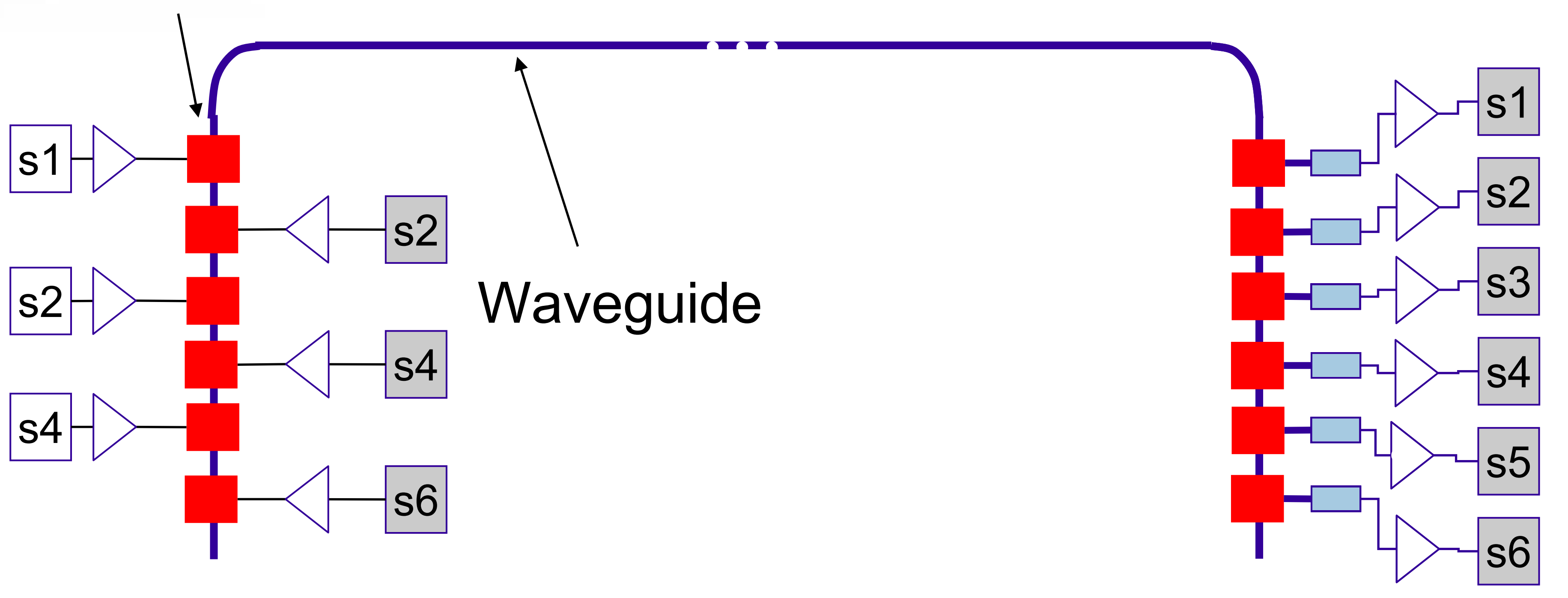


⇒ Values of effective k-value down to 1.7 with low crosstalk levels

⇒ Localized air gaps to maintain good thermal and mechanical properties

Ultra-low κ and Air gap (κ<1.7) (CVD and Spin-on)

Hypothetical On-die Optical Interconnects with WDM

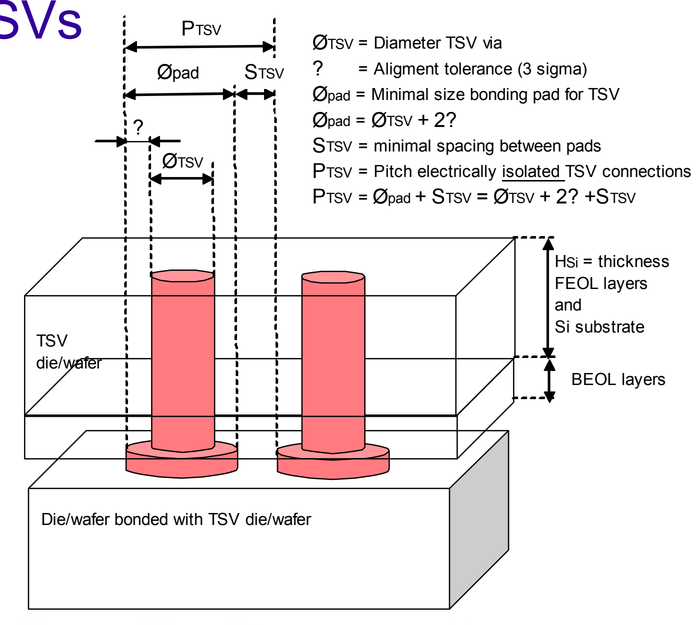


Intel Technology Journal, Volume 8, Issue 2, 2004

Interconnect HDTSV Roadmap “enabling terabits/sec at picojoules”

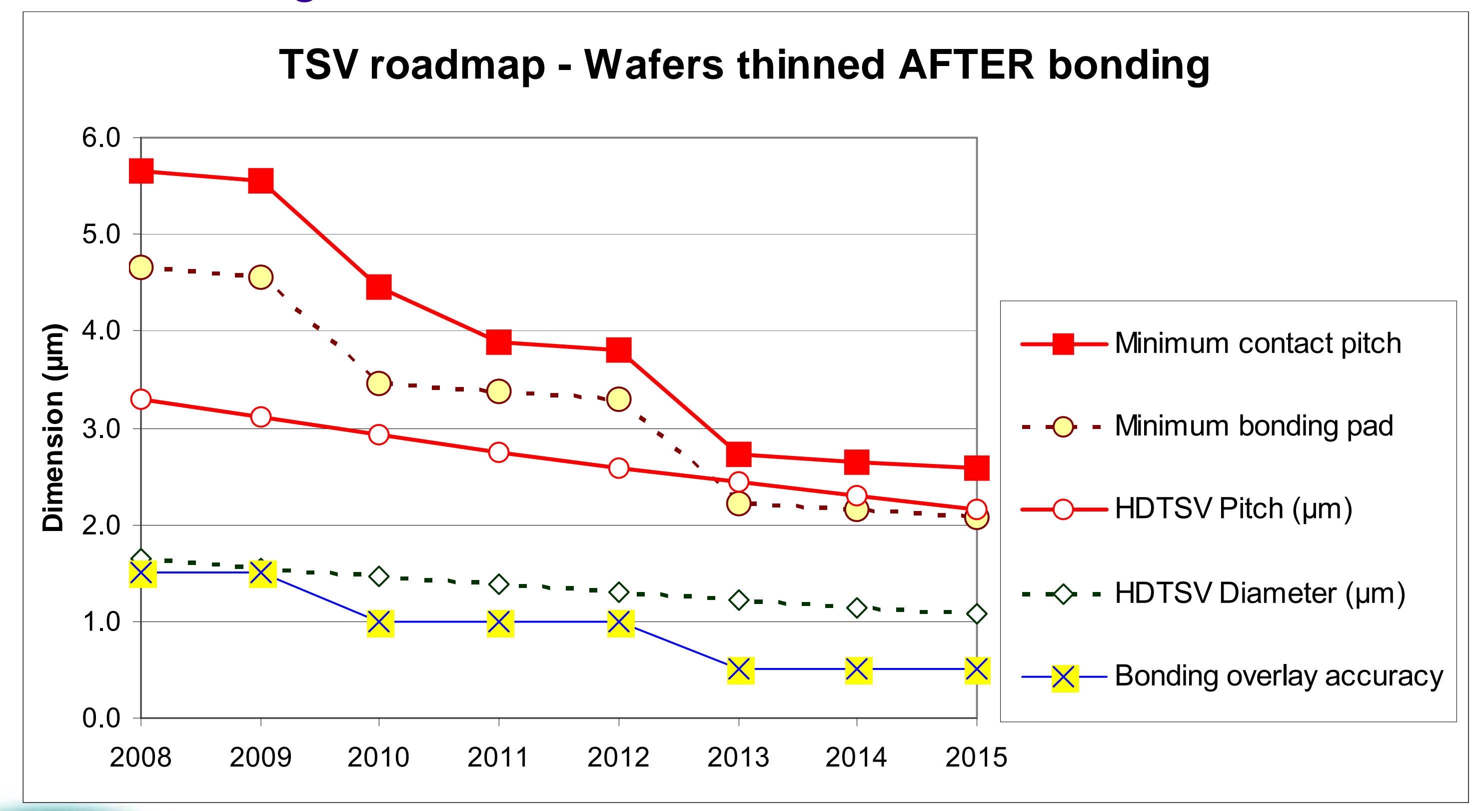
- The Interconnect perspective - examples:
  - High bandwidth/low energy interfaces between memory and logic
  - Heterogeneous integration with minimal parasitics (analog/digital, mixed substrate materials, etc)
  - “Re-architect” chip by placing macros (functional units) on multiple tiers (wafers) and connect using HDTSVs

- Model assumptions:
  - TSV diameter limited by silicon thickness and TSV Aspect Ratio:
  - Pitch limited by TSV diameter, misalignment tolerance, minimum pad spacing



DRAFT HDTSV Roadmap

- Represents devices that could appear in production, using at least one approach to 3D integration
  - ≤10 μm Si thickness, wafer-to-wafer integration, wafers thinned after bonding



2008 last words

- Metal 1 design rule concerns
  - Staggered contacted pitch used for definition
    - 68 nm half pitch for 2007
    - High performance MPU pitches scaling at ~0.75/2 years until 2009
    - Returning to 0.7/3 years 2010
- Convergence of MPU/ASIC and DRAM pitch in 2010
  - Commonality in the back-end (Cu based)

Summary of Notable 2008 changes

- Low-k slowdown
  - New range for bulk κ and κ_{eff}
- New Technology Introduction
  - ALD barrier processes and metal capping layers for Cu are lagging in introduction.
- No solutions seen for Cu resistivity rise
- Power Metric
  - Capacitance per unit length decreases due to decreases of the dielectric constant.
  - The dynamic power is expected to increase because of the increased number of metallization layers, larger chip size and increased frequency.

Last words

- Must manage the power envelope
- More Moore
  - Must continue to meet requirements of scaled metal/dielectric systems while developing CMOS-compatible equivalent scaling solutions
  - Cu resistivity impact real but manageable
  - materials solutions alone cannot deliver performance - end of traditional scaling
- More than Moore
  - integrated system approach required
  - Functional diversity enhances value