

CSE 140 Homework Five

March 5, 2007

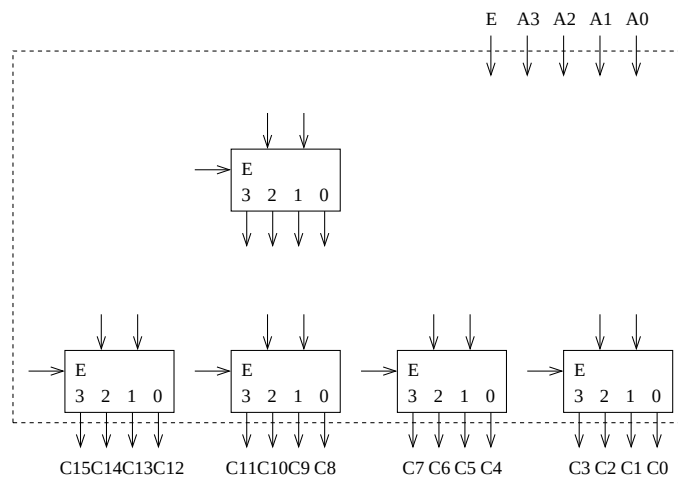
*Only **Problem Set Two** will be graded. Turn in only solutions to **Problem Set Two** which will be due on March 13 2007 at 1:00pm*

1 Problem Set One

- textbook 5.3
- textbook 5.7
- textbook 5.9
- textbook 5.10
- textbook 5.13(c)
- textbook 5.15
- textbook 5.17(c)(d)
- textbook 5.21

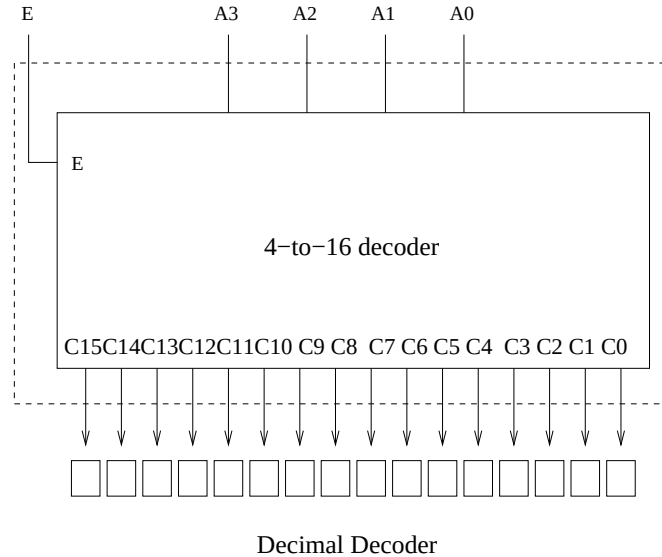
2 Problem Set Two

1 (Part A) The following is a partial depiction of a 4-to-16 decoder. It has 4 input lines, A_3, A_2, A_1, A_0 , and 16 output lines, $C_{15}, C_{14}, \dots, C_1, C_0$, as well as a control input, E . The 4-to-16 decoder is composed of four 2-to-4 decoders. Please fill in the missing connections in order to complete the schematic of the 4-to-16 decoder.



Implementing 4-to-16 decoder with 2-to-4 decoders

(Part B) A 4-to-16 decoder can be used to implement an **Excess-3** decoder, as shown in the figure below. In this case, the input $A_3A_2A_1A_0$ is an Excess-3 decimal code, and 10 of the original 16 output lines, $C_{15}, C_{14}, \dots, C_1, C_0$, are going to be specified as the output lines of the decimal decoder, denoted $D_9, D_8, \dots, D_1, D_0$. The output line D_i will be valid **iff** the enable signal E is valid **and** the input $A_3A_2A_1A_0$ represents a decimal digit i in Excess-3 representation. Please specify the 10 output lines $D_9, D_8, \dots, D_1, D_0$ in the boxes on the bottom of the figure below to complete the schematic of the **Excess-3 decoder**. Since there are 16 empty boxes but only 10 output signals, you can leave 6 boxes blank.



2 For this question, consider a 16-bit adder implemented in different design styles.

(Part A) For the table given below, indicate the order in which the corresponding terms will appear. If a term is not generated by a certain design style, indicate this by putting a N/A entry.

design style	$g_{(4,7)} (G_4)$	c_{11}	c_4	$p_{(0,3)} (P_0)$	p_3	s_4	g_2	c_{16}	s_{12}
carry ripple									
4-bit CLA units connected in carry ripple fashion									
2-level CLA									

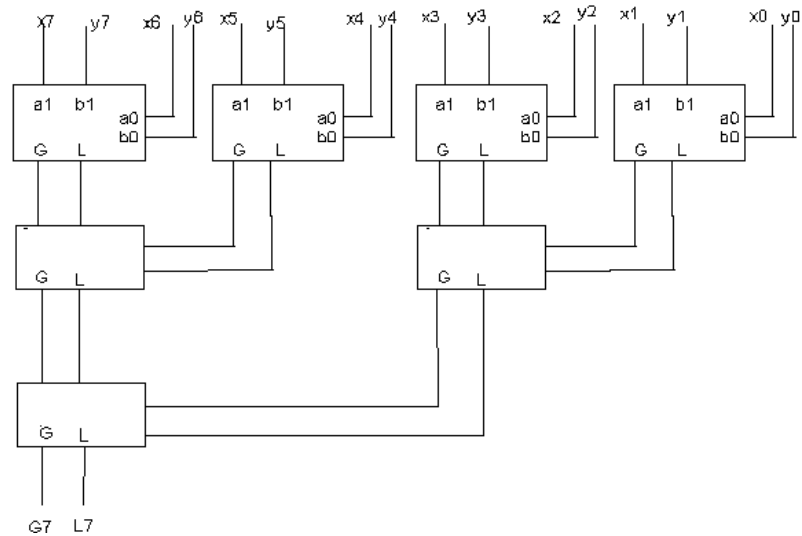
(Part B) You are given that a 4-bit CLA unit has a delay of 4ns, a 1-bit full adder has a delay of 3ns, and that XOR and AND gates have respective delays of 2ns. For the CLA unit, assume all the outputs appear at the same time. Find the input to output delay of the 16 bit adder designed in the following styles:

1. carry ripple
2. 4-bit CLA units connected in carry ripple fashion
3. 2 level CLA

(Part C) Which of the design styles in part 2 has the smallest area, which has the largest?

3 (Part A) Provide a *minimized* gate level implementation of a 2-bit magnitude comparator capable of providing *greater-than-or-equal-to* and *less-than-or-equal-to* indicators.

(Part B) Recall the parallel 8-bit magnitude comparator from your book composed of 2-bit magnitude comparators; the circuit is given below. Propose a parallel implementation of the 8-bit magnitude comparator that utilizes the previously designed 2-bit magnitude comparator block so that *greater-than-or-equal-to* and *less-than-or-equal-to* indicators can be generated.



(Part C) If you had a *different* 2-bit magnitude comparator, producing as outputs *greater-than-or-equal-to* and *less-than* indicators, could you design an 8-bit magnitude comparator capable of selecting among:

- less-than
- greater-than
- equal-to

indicators, by utilizing this new block only? If yes, please show an implementation. If not, please explain why not.