

Altera Quartus II Tutorial

CSE140L – WI06

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CSE Dept. UCSD

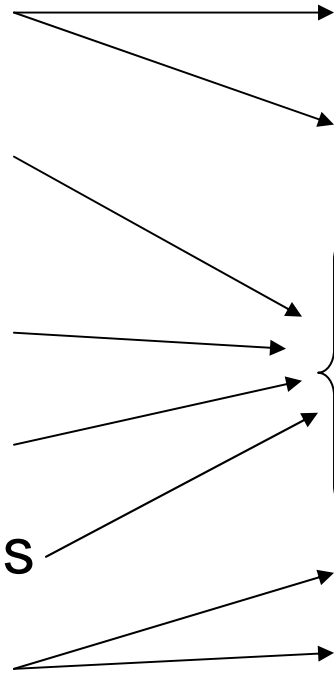
Altera Quartus II

- The Quartus II development software provides a *complete design environment* for FPGA designs.
- Design entry using schematics, block diagrams, VHDL, and Verilog HDL .
- Design analysis and synthesis, fitting, assembling, timing analysis, simulation.

Altera Quartus II

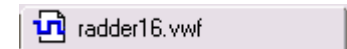
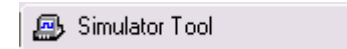
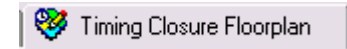
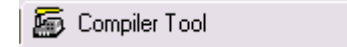
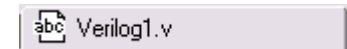
Design flow

- Design entry
- Analysis and synthesis
- Fitting
- Assembling
- Timing analysis
- Simulation



Quartus II

- HDL editor
- Block diagram, schematic editor
- Compiler tool
- Compilation report
- Timing closure floorplan
- Simulator tool
- Waveform editor



Tutorial Outline

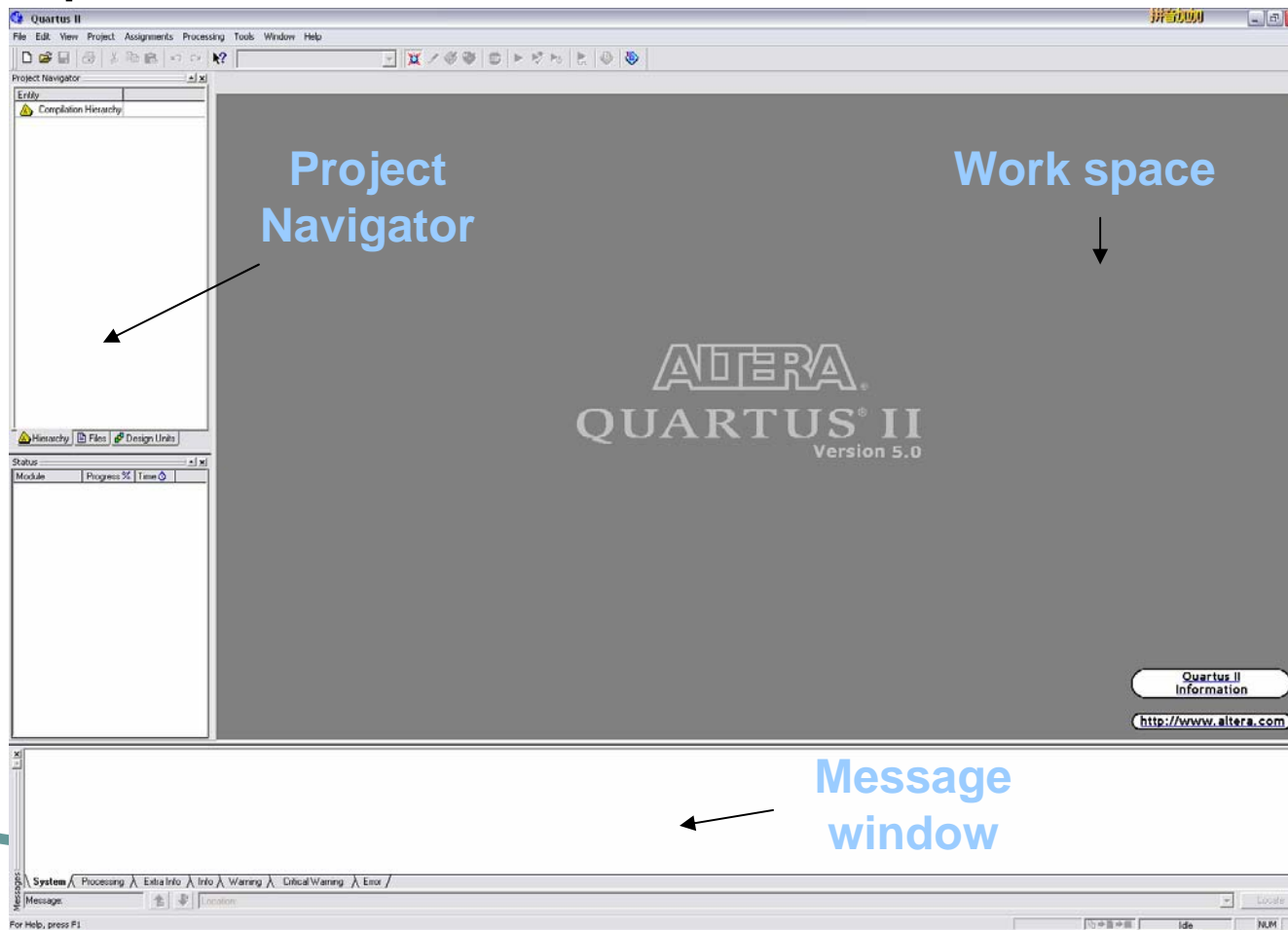
- Open Quartus II and pick a device.
- Build a full adder. (*Block/Schematic*)
 - Add components
 - Add ports
 - Add connections (*single wire connection*)
- Build a 4-bit adder.
 - Create a block for full adder
 - Use conduit and port mapping

Tutorial Outline

- Compile the 4-bit adder.
 - Open compiler tool
 - Read compilation report
 - Open timing closure floorplan
- Simulate the 4-bit adder.
 - Open simulator tool
 - Edit simulation waveform
 - Observe simulation results
- Schematic for 16-bit Multiplexer
 - Use connections by name

Start Quartus II

- Open Quartus II, click on the icon



Create a new project

- Menu → File → New Project Wizard

New Project Wizard: Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?
D:\users\jhliu\TA\cse140L_w106\labs\lab1\adder4

What is the name of this project?
adder4

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
adder4

Use Existing Project Settings ...

< Back Next > Finish Cancel

New Project Wizard: Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Family: Stratix

Target device

Auto device selected by the Filter from the 'Available devices' list

Specific device selected in 'Available devices' list

Available devices:

- EP1S10B672C6
- EP1S10F484C5
- EP1S10F672C6
- EP1S10F780C5
- EP1S10F780C5ES
- EP1S20B672C6
- EP1S20F484C5
- EP1S20F672C6
- EP1S20F780C5
- EP1S25B672C6
- EP1S25F672C6
- EP1S25F780C5
- EP1S25F1020C5
- EP1S25F672C6_HARDCOPY_FPGA_PROTO
- EP1S30B956C5
- EP1S30F780C5
- EP1S30F1020C5

Filters

Package: Any

Pin count: Any

Speed grade: Fastest

Core voltage: 1.5V

Show Advanced Devices

Companion device:

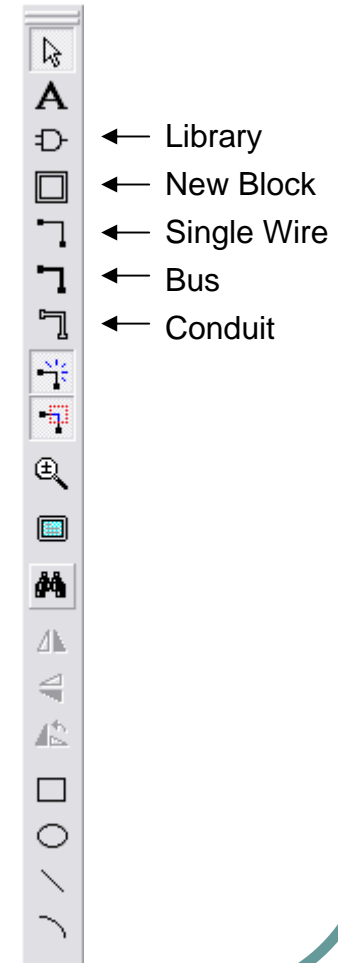
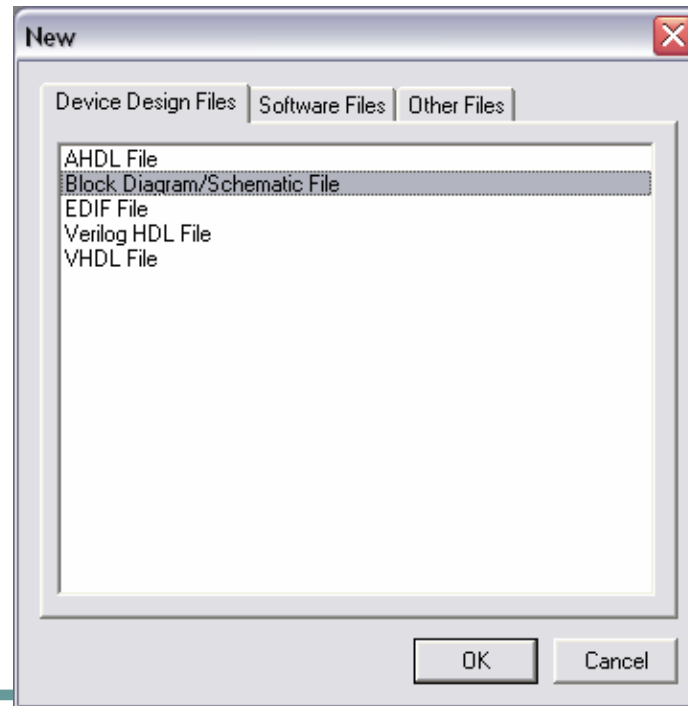
HardCopy II:

Limit DSP & RAM to HardCopy II device resources


< Back Next > Finish Cancel

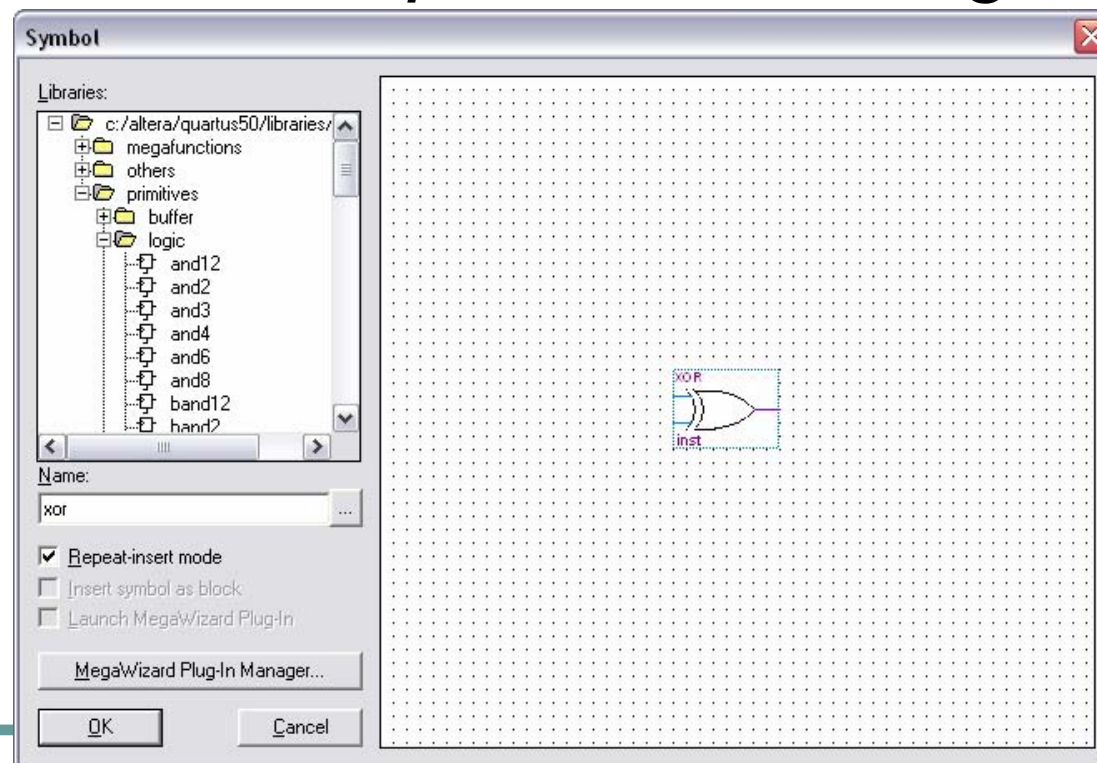
Build a full adder

- Menu → File → New
- Create a Block Diagram/Schematic File
- Menu → File → Save As: fadder.bdf



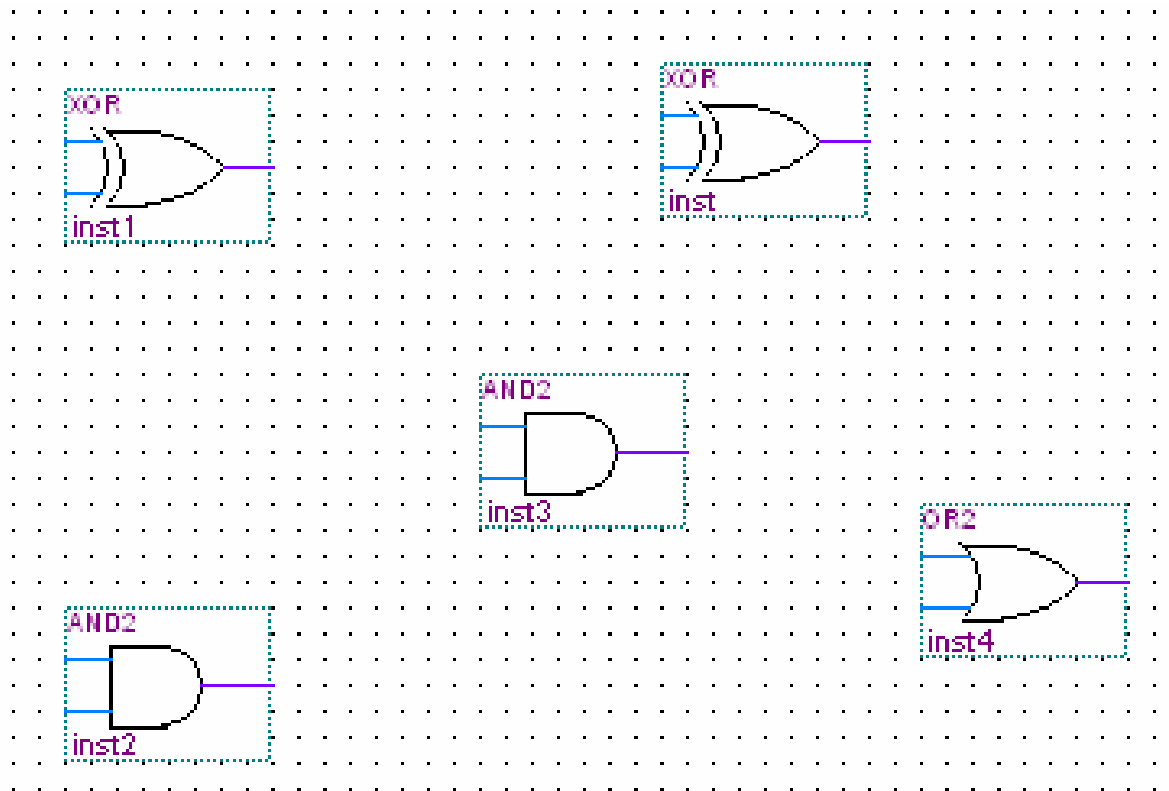
Build a full adder

- Click on library 
- Find *xor* under *primitives* → *logic*



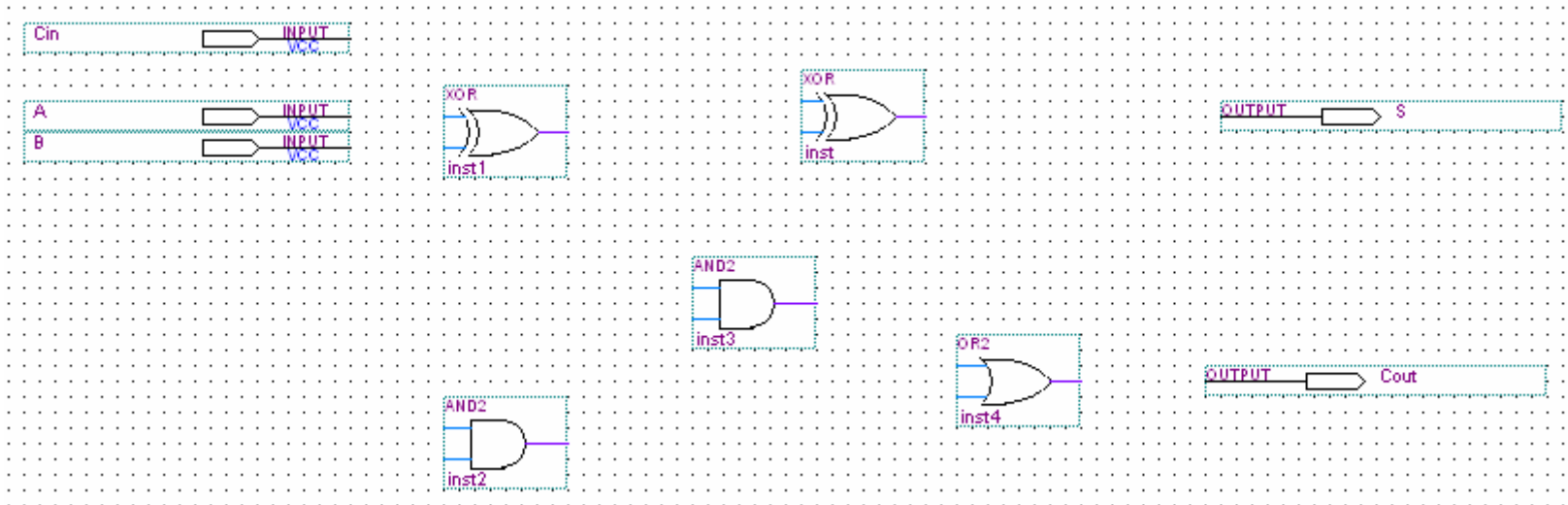
Build a full adder

- Place two *xor*, two *and2* and one *or2*.



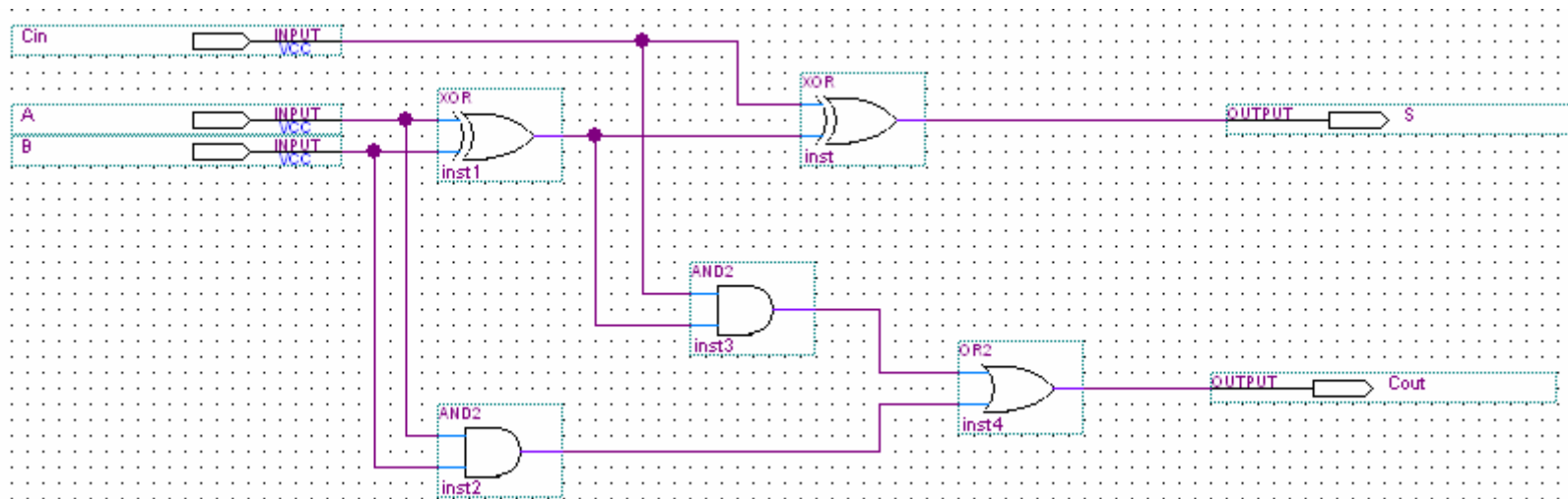
Build a full adder

- Find *input* and *output* under *primitives* → *pin*, and place three *input* and two *output*
- Double click on each pin, to change pin name.



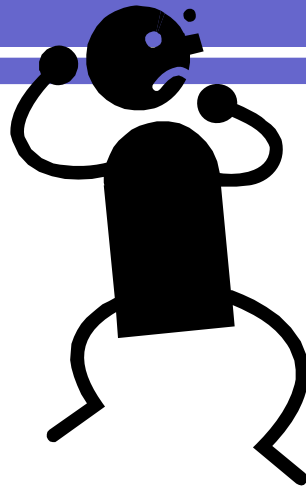
Build a full adder

- Connect them by single wire 




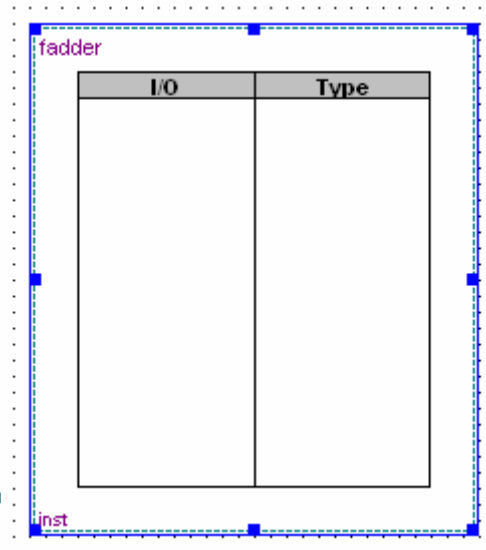
- Save the file

Questions



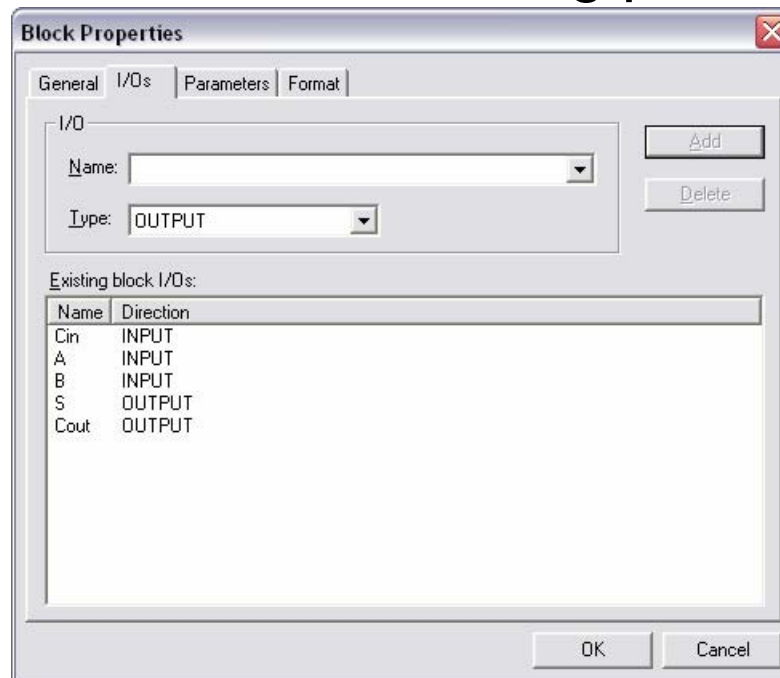
Build a 4-bit adder

- Menu → File → New
- Create a Block Diagram/Schematic File
- Menu → File → Save As: adder4.bdf
- Click on new block , and draw a block.
- Double click on the block name, change it to *fadder*



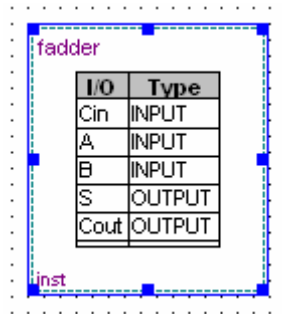
Build a 4-bit adder

- Right click on the block, and select *Block Properties* in the pop-up menu.
- In the tag *I/Os*, add the following ports:

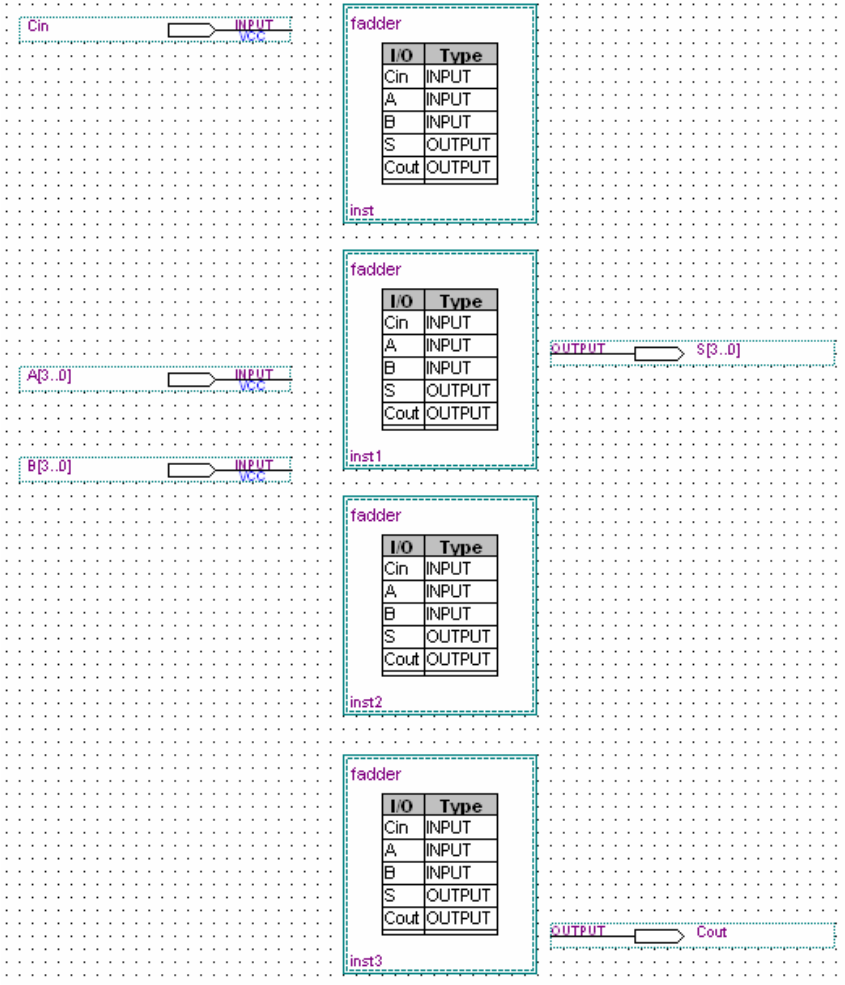


Build a 4-bit adder

- Click on *OK* to dismiss the properties window.
- Right click on the block, and select *AutoFit* in the pop-up menu.

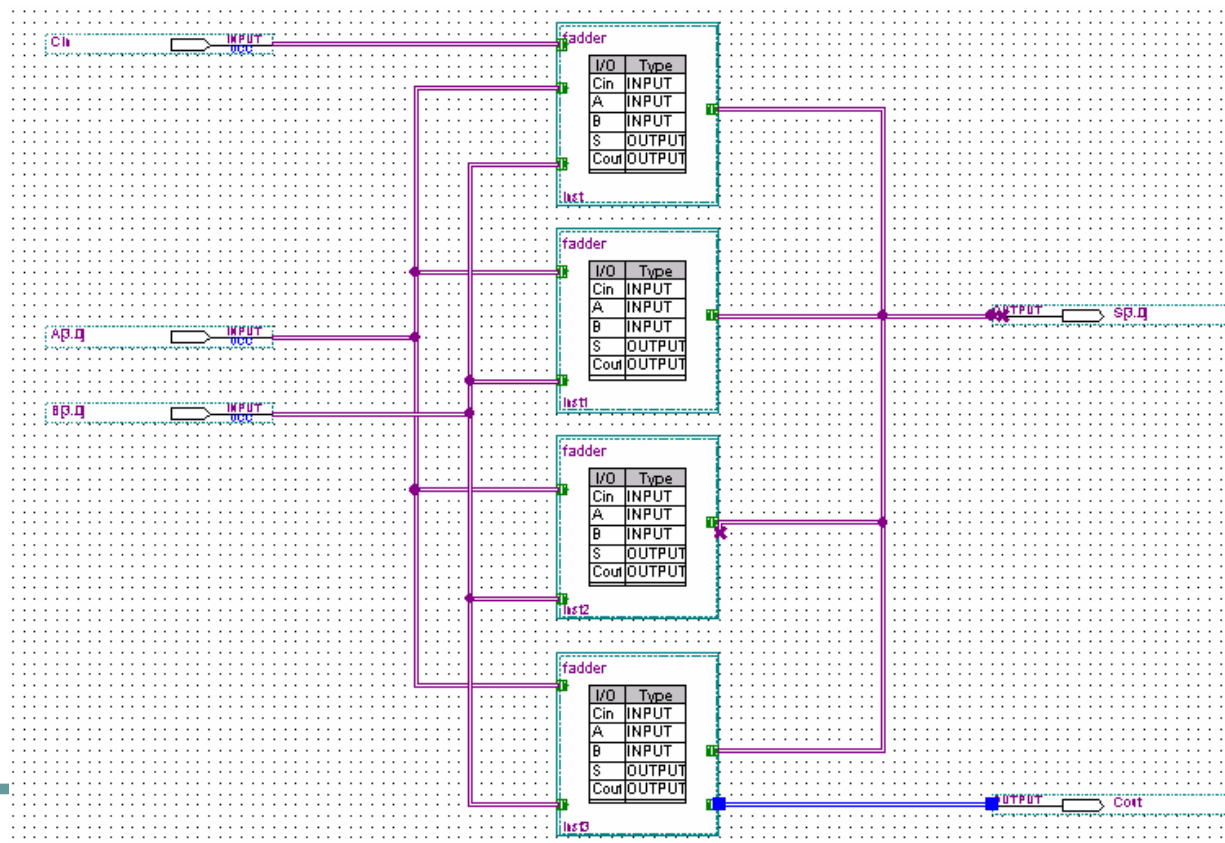


- Select the block, make four copies by copy/paste.
- Add 3 inputs and 2 outputs.



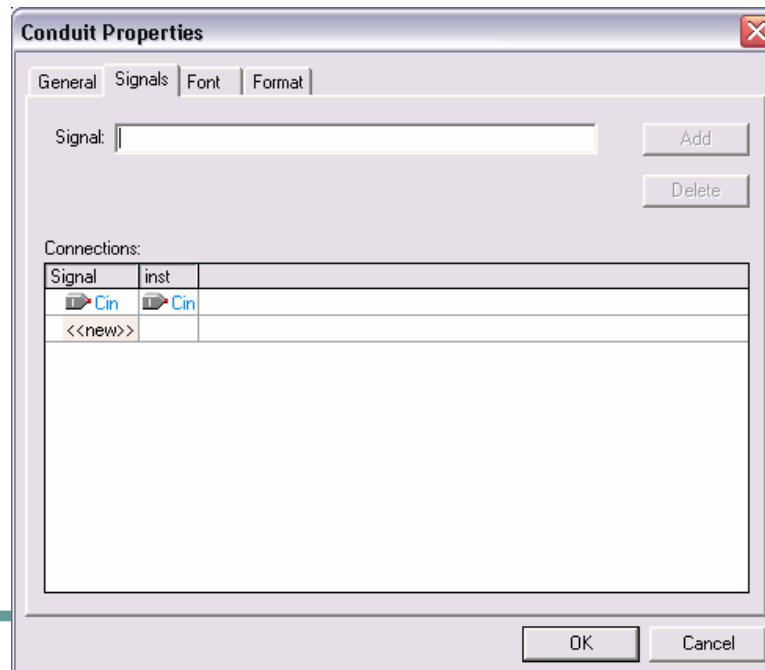
Build a 4-bit adder

- Use conduit tool to connect each *fadder* to inputs and outputs. Conduit can stop at any point on a block border.



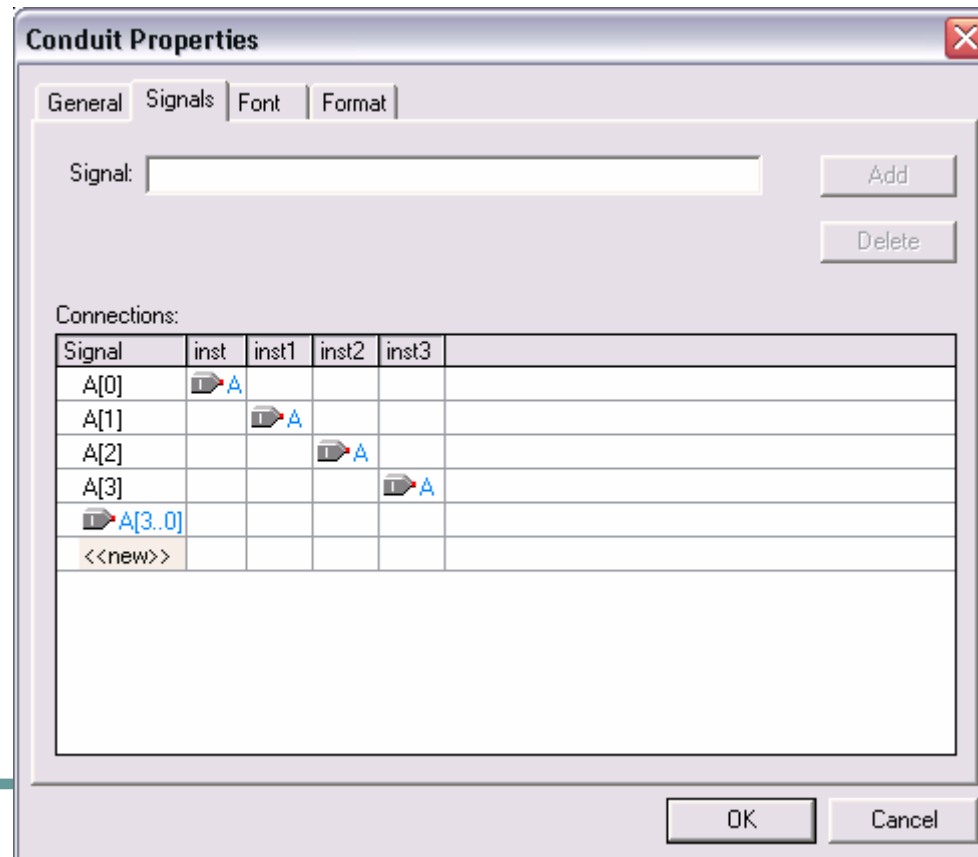
Build a 4-bit adder

- The primary input *Cin* is automatically connected to the *Cin* port of *inst* by the same name.
- Right click on the conduit, select *properties*, the connection can be found in the tab *Signals*.



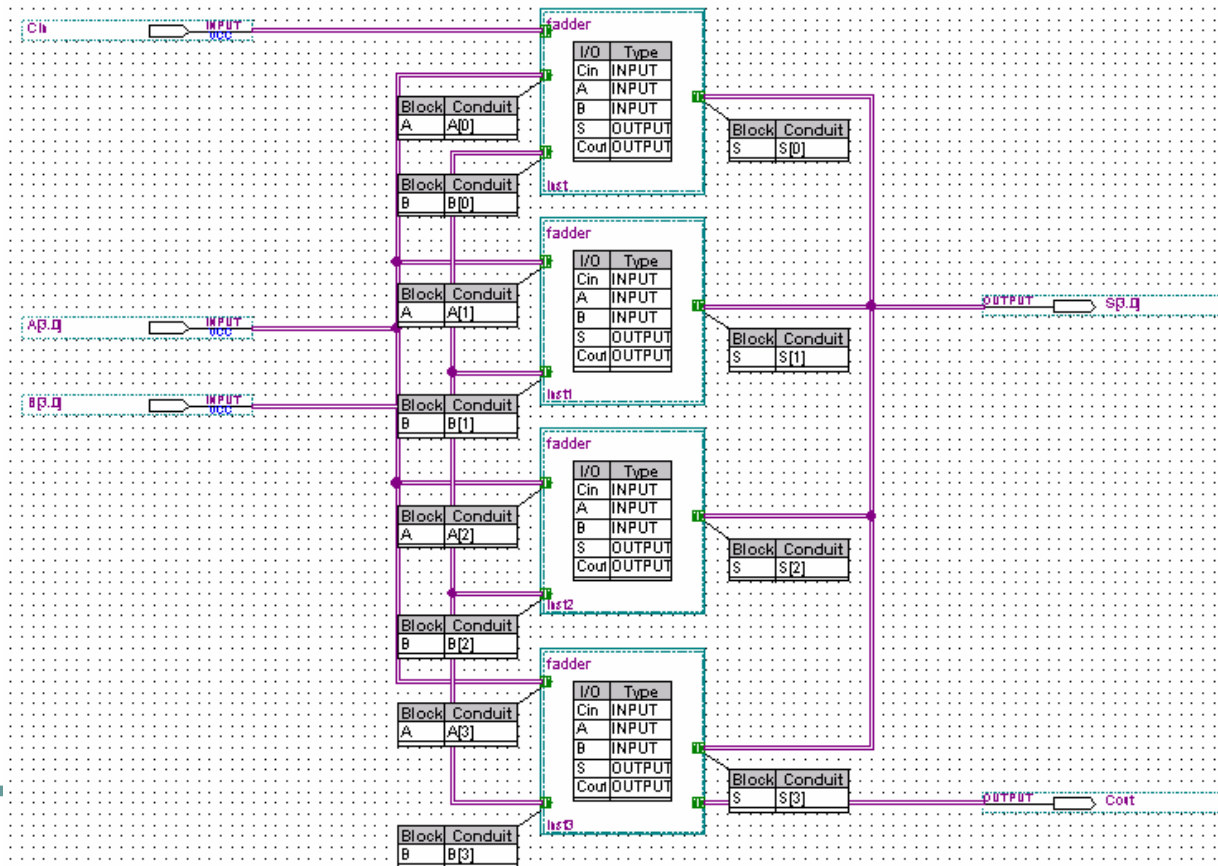
Build a 4-bit adder

- For $A[3..0]$, $B[3..0]$ and $S[3..0]$, port mapping should be manually defined. Edit the *signals* property for $A[3..0]$ like this:



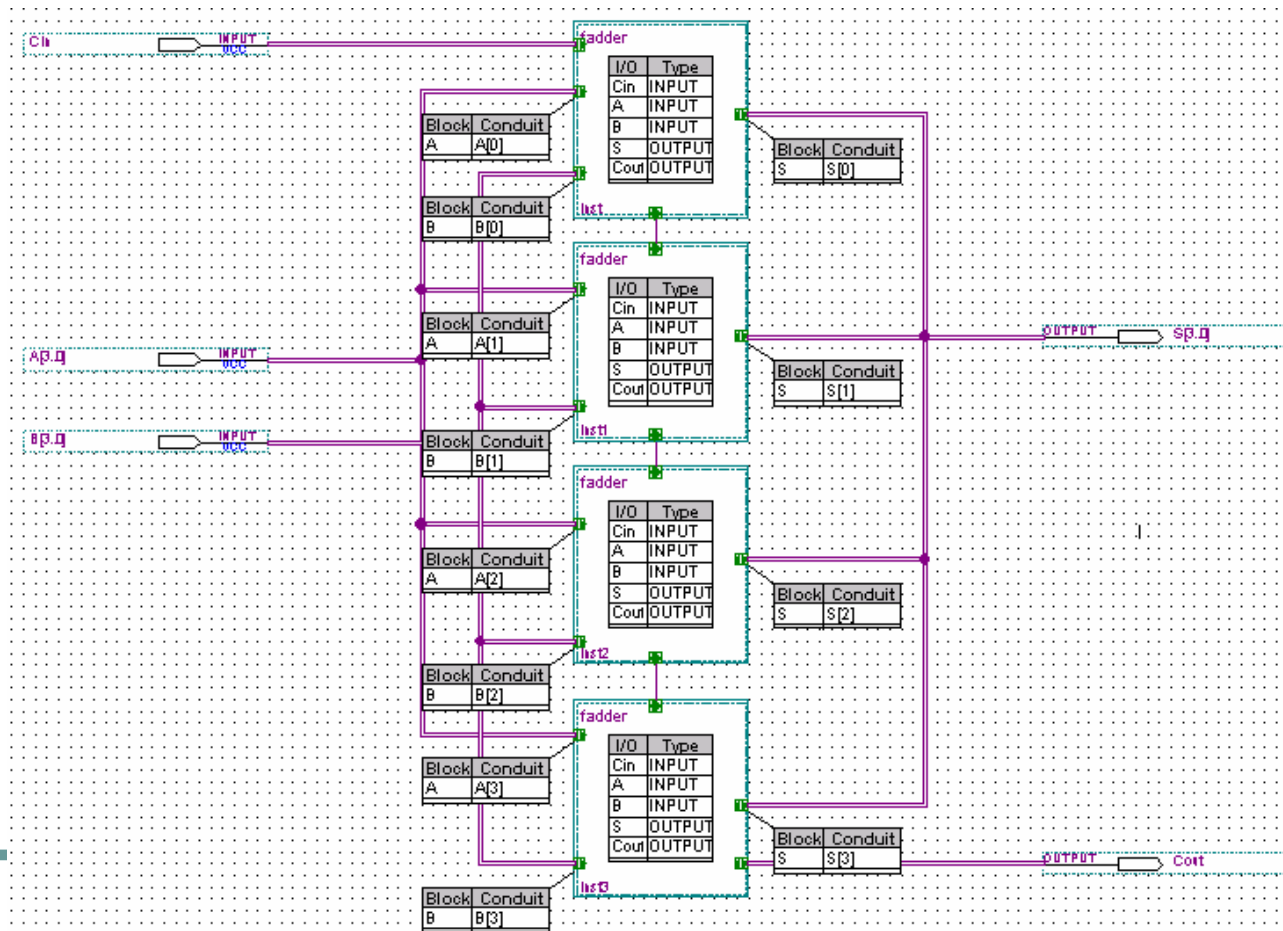
Build a 4-bit adder

- After port mapping for A[3..0], B[3..0] and S[3..0], you will see this:




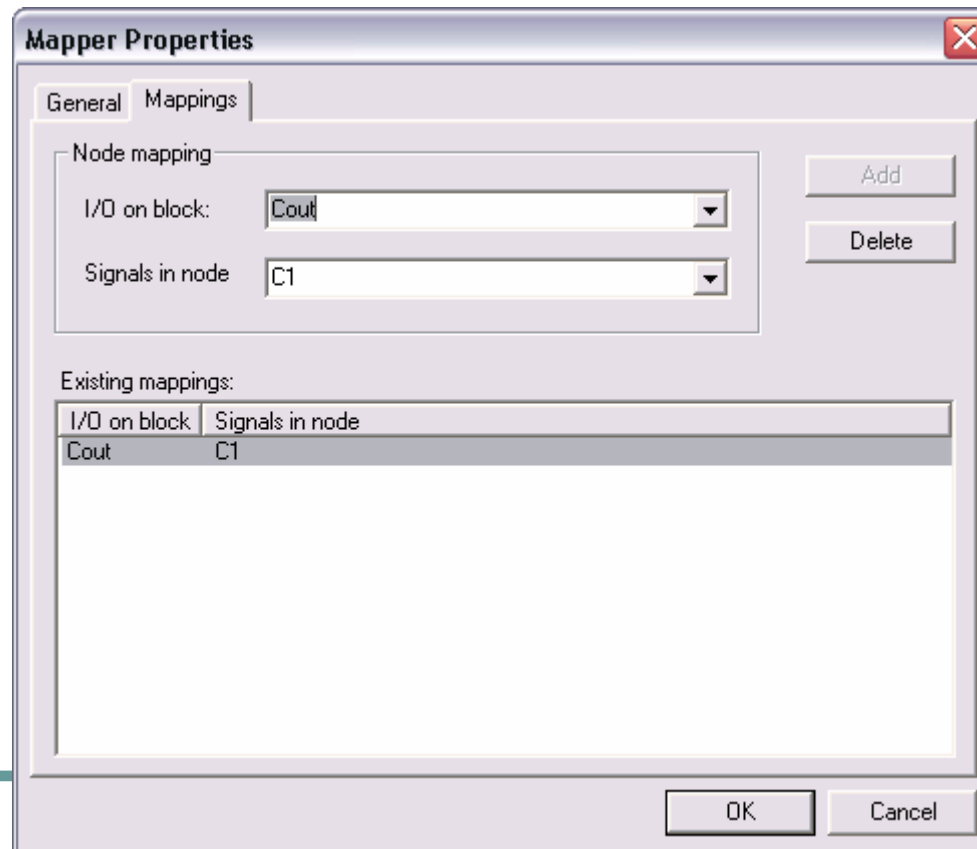
Build a 4-bit adder

- Place single wires for carry signals.



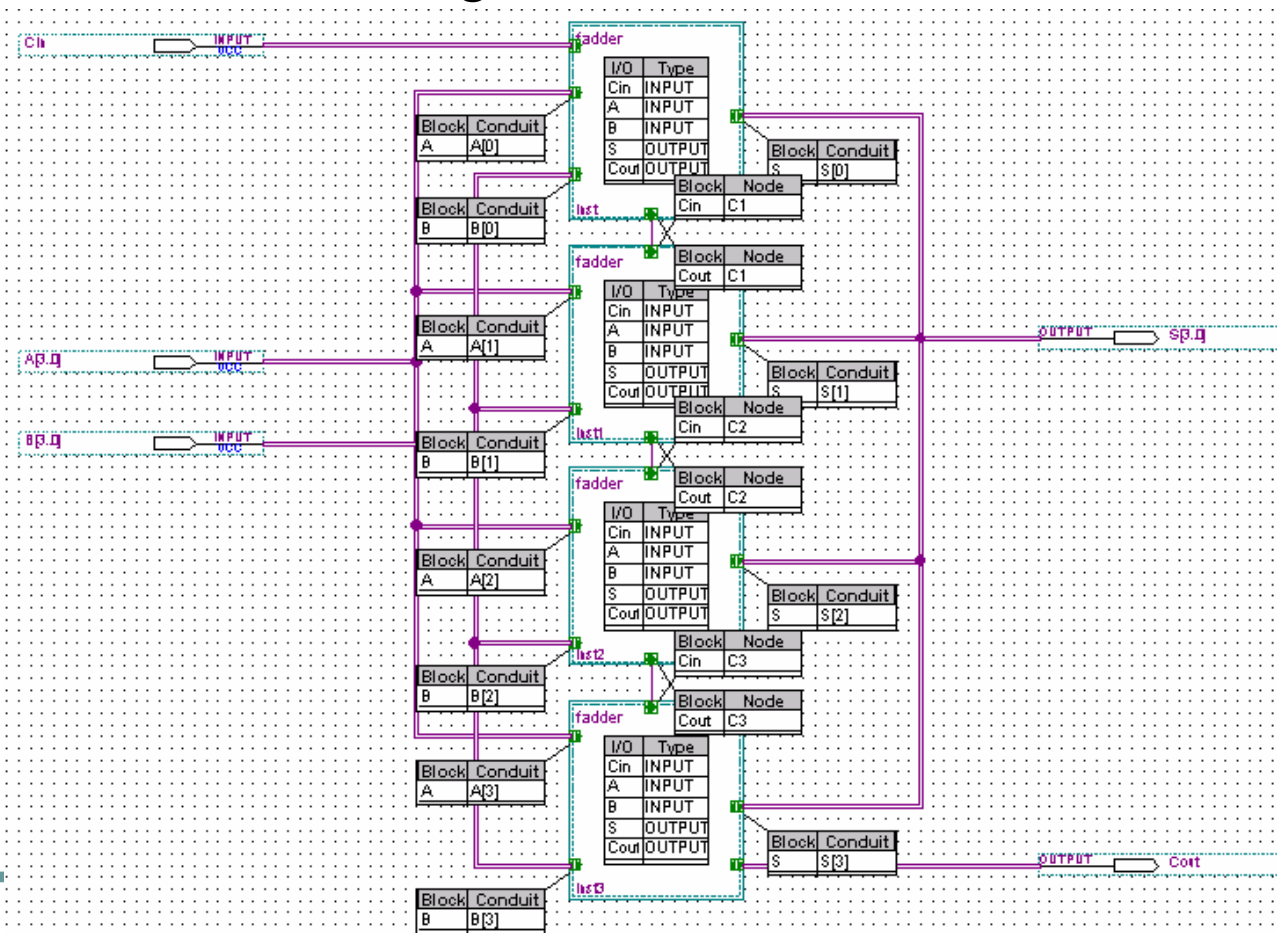
Build a 4-bit adder

- Double click on a port mapper , and define port mapping in the tab Mappings. For example, map *Cout* to signal *C1*.

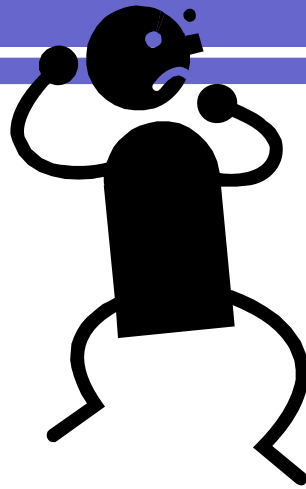


Build a 4-bit adder

- Here's the final diagram.

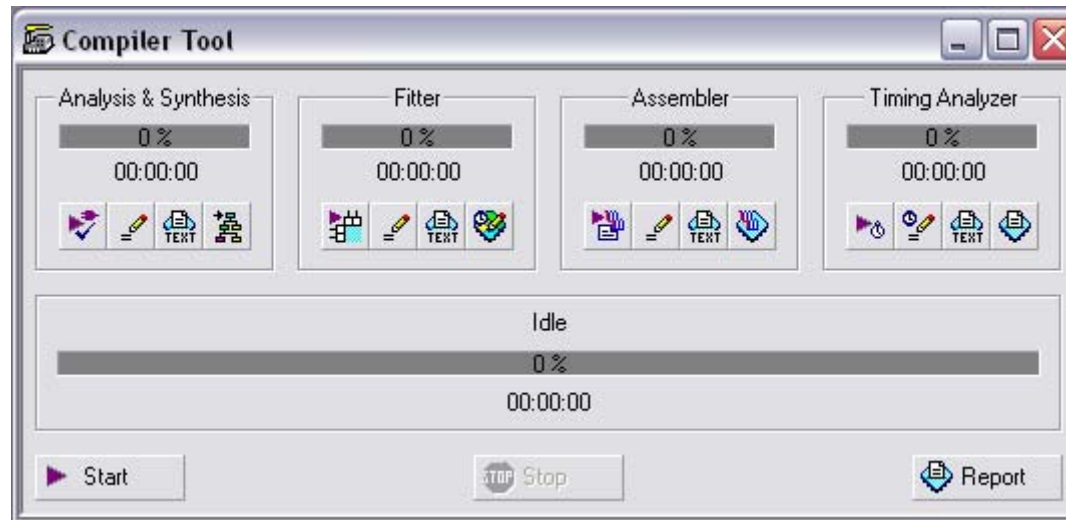


Questions



Compile the design

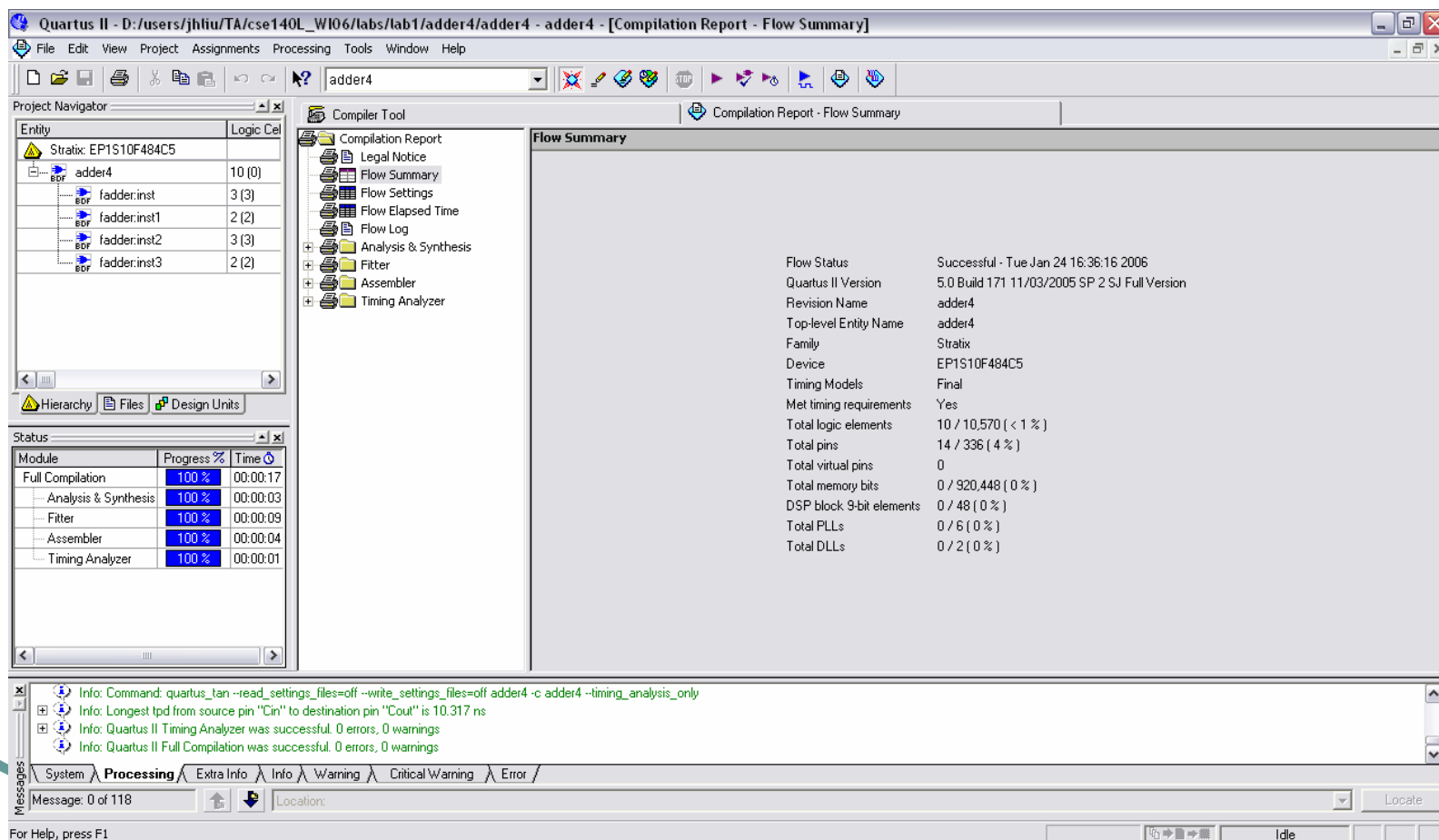
- Menu → Tools → Compiler Tool



- Click on *Start*. The design will be compiled automatically.

Compile the design

- Click on *Report* button  after compilation.



The screenshot displays the Quartus II software interface during a compilation process. The main window is titled "Quartus II - D:/users/jhliu/TA/cse140L_WI06/labs/lab1/adder4/adder4 - adder4 - [Compilation Report - Flow Summary]". The interface is divided into several panes:

- Project Navigator:** Shows the project hierarchy with entities like "adder4" and its instances "fadder.inst1", "fadder.inst2", and "fadder.inst3".
- Status:** A table showing the progress of various compilation modules.
- Compiler Tool:** A tree view showing the compilation flow, including "Analysis & Synthesis", "Fitter", "Assembler", and "Timing Analyzer".
- Flow Summary:** A detailed report of the compilation process, including flow status, version information, and resource usage.
- Messages:** A log of messages from the compilation process, including the command used and the successful completion of the timing analysis and full compilation.

The **Status** pane contains the following data:

Module	Progress %	Time
Full Compilation	100 %	00:00:17
Analysis & Synthesis	100 %	00:00:03
Fitter	100 %	00:00:09
Assembler	100 %	00:00:04
Timing Analyzer	100 %	00:00:01

The **Flow Summary** pane displays the following information:

- Flow Status: Successful - Tue Jan 24 16:36:16 2006
- Quartus II Version: 5.0 Build 171 11/03/2005 SP 2 SJ Full Version
- Revision Name: adder4
- Top-level Entity Name: adder4
- Family: Stratix
- Device: EP1S10F484C5
- Timing Models: Final
- Met timing requirements: Yes
- Total logic elements: 10 / 10,570 (< 1 %)
- Total pins: 14 / 336 (4 %)
- Total virtual pins: 0
- Total memory bits: 0 / 920,448 (0 %)
- DSP block 9-bit elements: 0 / 48 (0 %)
- Total PLLs: 0 / 6 (0 %)
- Total DLLs: 0 / 2 (0 %)

The **Messages** pane shows the following log entries:

- Info: Command: quartus_tan -read_settings_files=off -write_settings_files=off adder4 -c adder4 -timing_analysis_only
- Info: Longest tpd from source pin "Cin" to destination pin "Cout" is 10.317 ns
- Info: Quartus II Timing Analyzer was successful. 0 errors, 0 warnings
- Info: Quartus II Full Compilation was successful. 0 errors, 0 warnings

Compile the design

- Worst delay can be found in Timing Analyzer report

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tpd	N/A	None	10.317 ns	Cin	Cout			0
2	Total number of failed paths								

Context Menu Options:

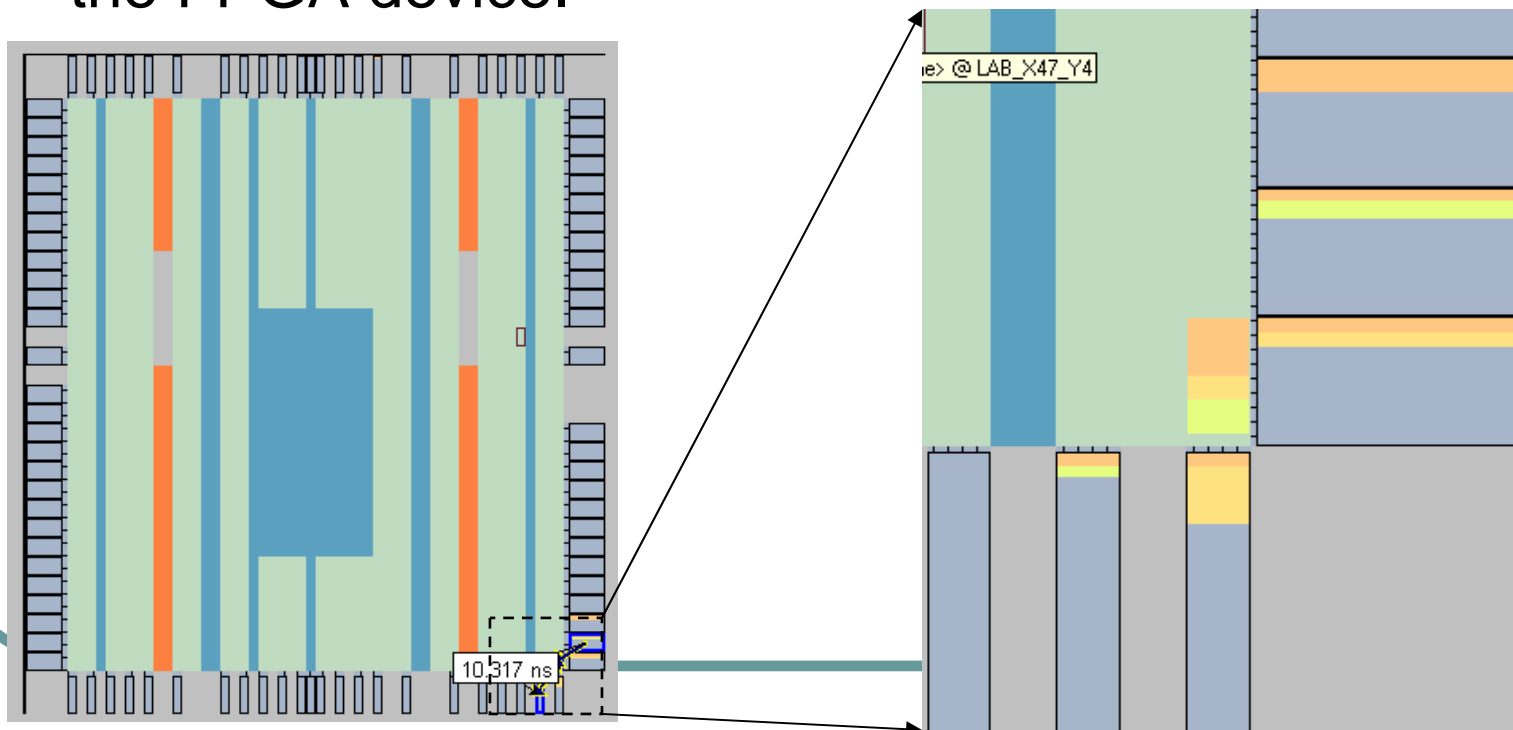
- Copy (Ctrl+C)
- Select All (Ctrl+A)
- Align Left
- Align Right
- List Paths
- Locate (highlighted)
- Timing Settings...
- Save Current Report Section As...

Sub-menu for 'Locate':

- Locate in Assignment Editor
- Locate in Pin Planner
- Locate in Timing Closure Floorplan (highlighted)
- Locate in Chip Editor
- Locate in Resource Property Editor
- Locate in Technology Map Viewer
- Locate in RTL Viewer
- Locate in Design File

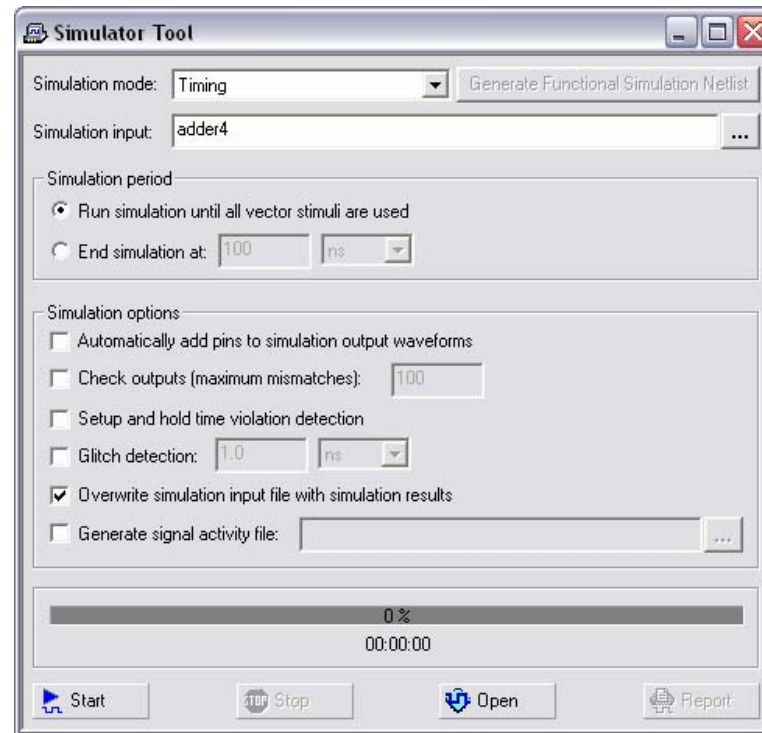
Compile the design

- Select the worst delay, right click on it, and select *locate* in the pop-up menu → Locate in Timing Closure Floorplan. You can see the design implementation in the FPGA device.



Simulate the design

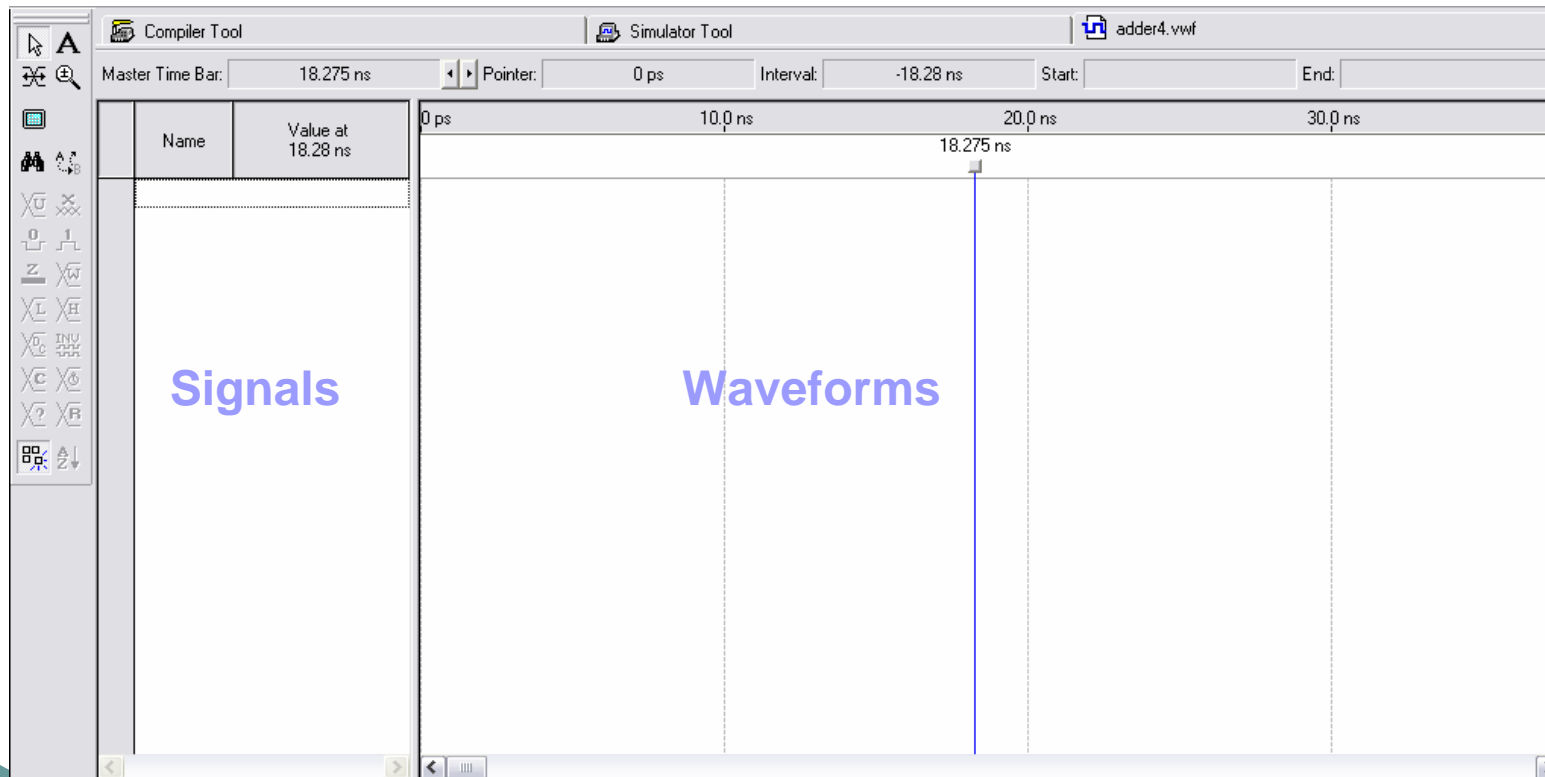
- Menu → Tools → Simulator Tool



- Type *adder4* for *Simulation input*

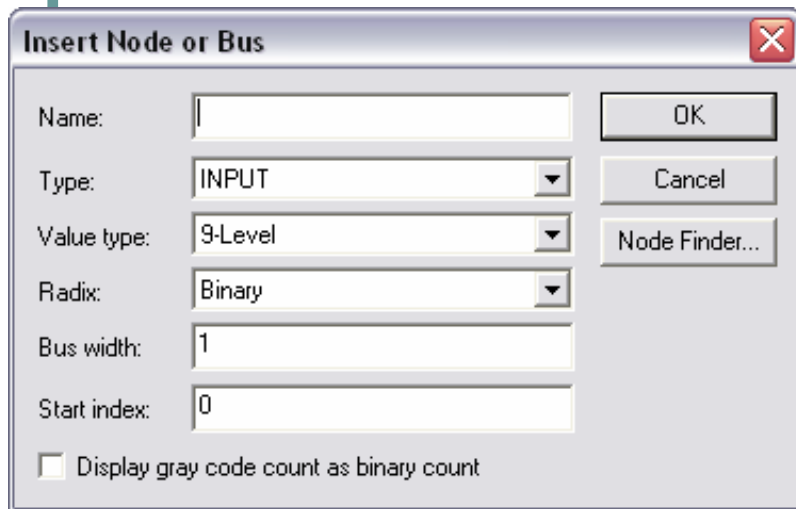
Simulate the design

- Click on *Open* button  *Open* , and save the file as *adder4.vwf*



Simulate the design

- Double click on signals area, and click the button *Node Finder*
- List all the pins and select the primary inputs and outputs, then click *OK*.



Insert Node or Bus

Name:

Type:

Value type:

Radix:

Bus width:

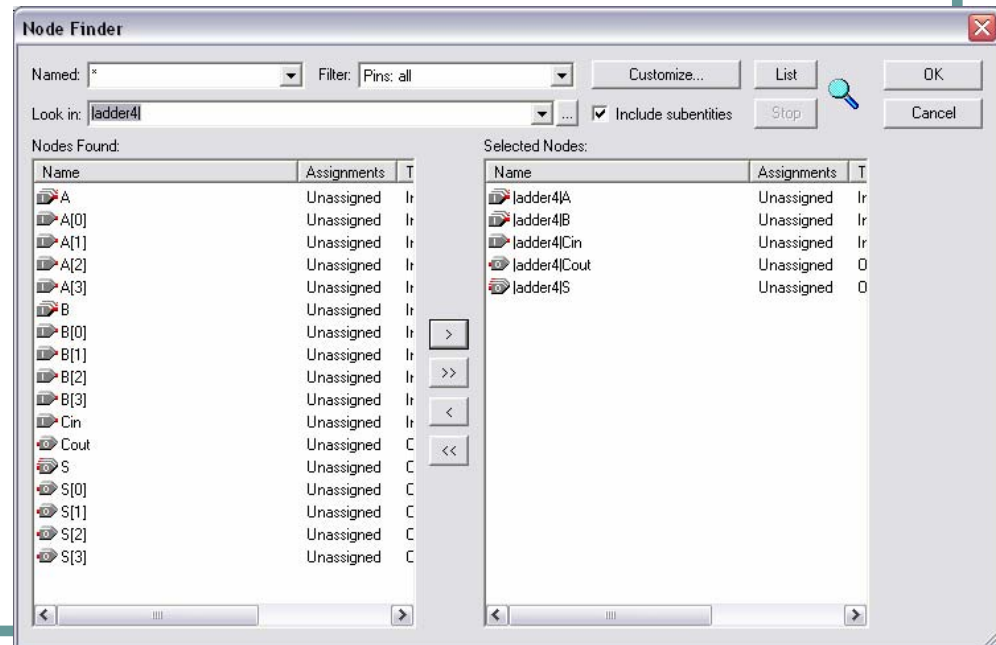
Start index:

Display gray code count as binary count

OK

Cancel

Node Finder...



Node Finder

Named: * Filter: Pins: all

Look in: ladder4

Include subtities

Nodes Found:

Name	Assignments	T
A	Unassigned	Ir
A[0]	Unassigned	Ir
A[1]	Unassigned	Ir
A[2]	Unassigned	Ir
A[3]	Unassigned	Ir
B	Unassigned	Ir
B[0]	Unassigned	Ir
B[1]	Unassigned	Ir
B[2]	Unassigned	Ir
B[3]	Unassigned	Ir
Cin	Unassigned	Ir
Cout	Unassigned	C
S	Unassigned	C
S[0]	Unassigned	C
S[1]	Unassigned	C
S[2]	Unassigned	C
S[3]	Unassigned	C

Selected Nodes:

Name	Assignments	T
ladder4A	Unassigned	Ir
ladder4B	Unassigned	Ir
ladder4Cin	Unassigned	Ir
ladder4Cout	Unassigned	0
ladder4S	Unassigned	0

OK

Cancel

Simulate the design

- To change the value of each input, right click on the input and select *value* in the pop-up menu.

The screenshot displays a digital logic simulator interface. On the left, a table lists signals and their values at 20.0 ns:

Name	Value at 20.0 ns
A	B 0000
B	B 0000
Cin	B 0
Cout	B X
S	B XXXX

The main area shows a waveform editor with a time axis from 0 ps to 140.0 ns. A context menu is open over the signal trace, listing various actions:

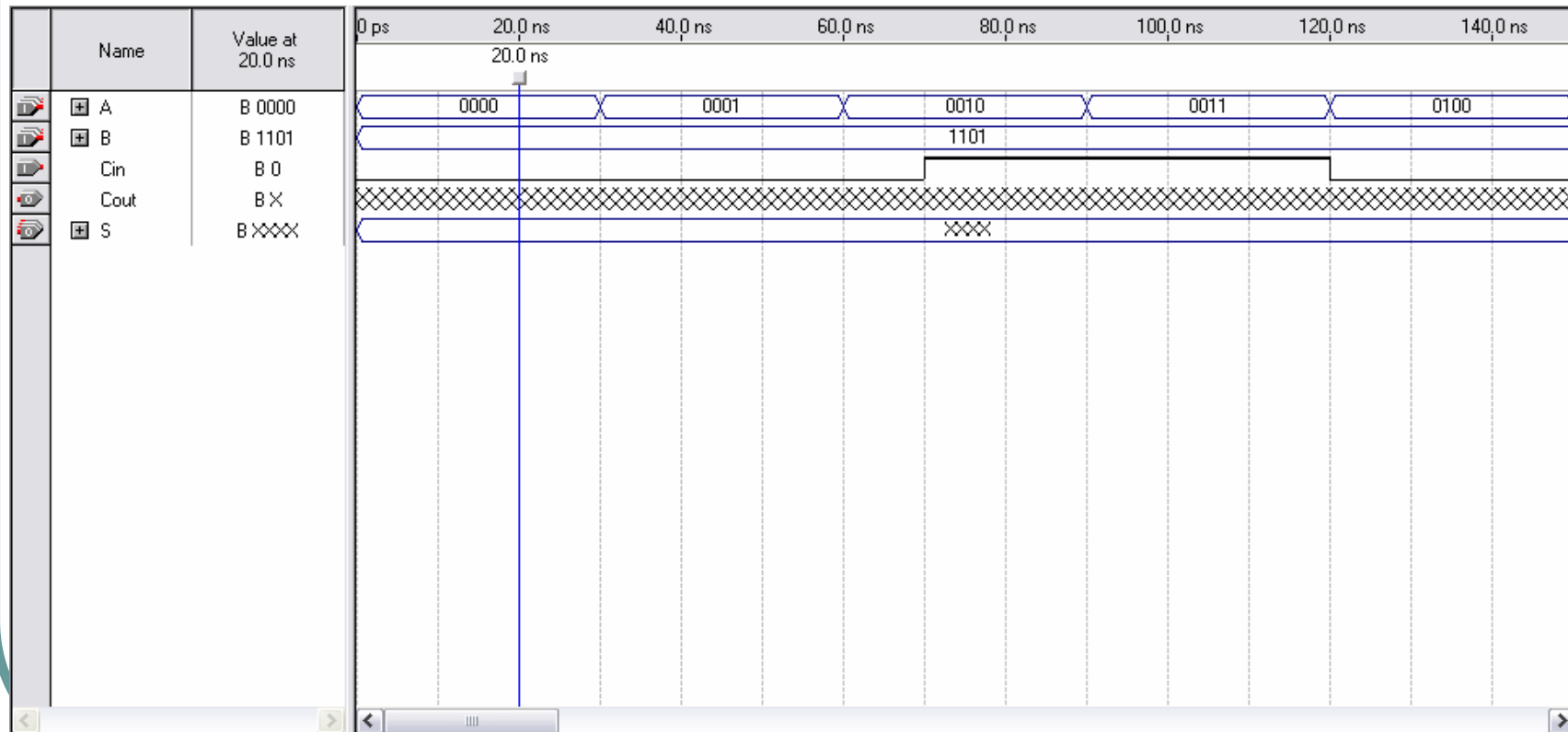
- Cut (Ctrl+X)
- Copy (Ctrl+C)
- Paste (Ctrl+V)
- Paste Special...
- Repeat Paste...
- Delete (Del)
- Insert Node or Bus...
- Select Entire Waveform Interval
- Group...
- Ungroup
- Value (with a right-pointing arrow)
- Insert Waveform Interval...
- Locate (with a right-pointing arrow)
- Zoom (with a right-pointing arrow)
- Properties

The 'Value' submenu is expanded, showing the following options:

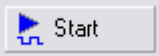
- Grow or Shrink... (Ctrl+Alt+G)
- Uninitialized (U) (Ctrl+Alt+U)
- Forcing Unknown (X) (Ctrl+Alt+X)
- Forcing Low (0) (Ctrl+Alt+0)
- Forcing High (1) (Ctrl+Alt+1)
- High Impedance (Z) (Ctrl+Alt+Z)
- Weak Unknown (W) (Ctrl+Alt+W)
- Weak Low (L) (Ctrl+Alt+L)
- Weak High (H) (Ctrl+Alt+H)
- Don't Care (DC) (Ctrl+Alt+D)
- Invert (Ctrl+Alt+I)

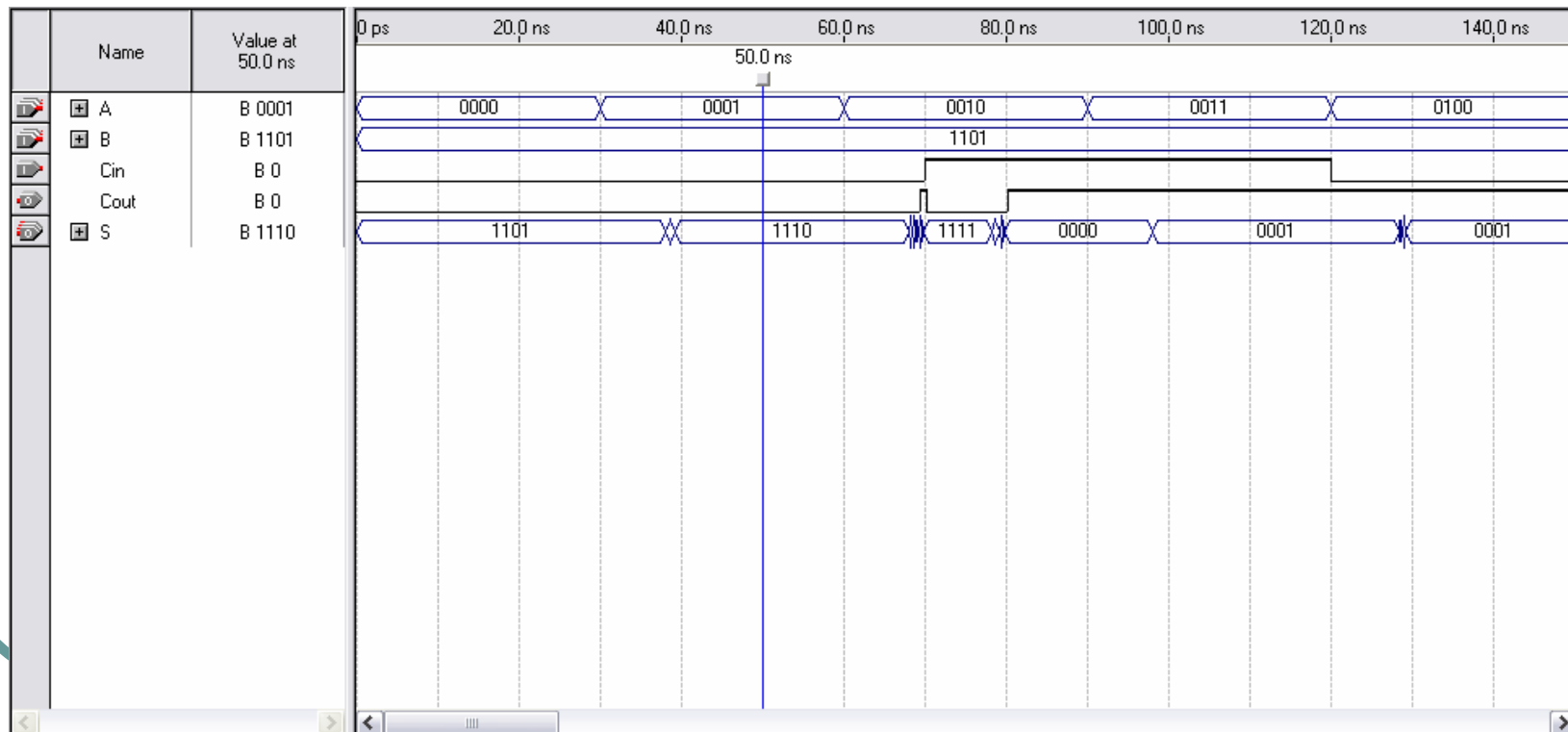
Simulate the design

- Set value to each inputs and save the file.



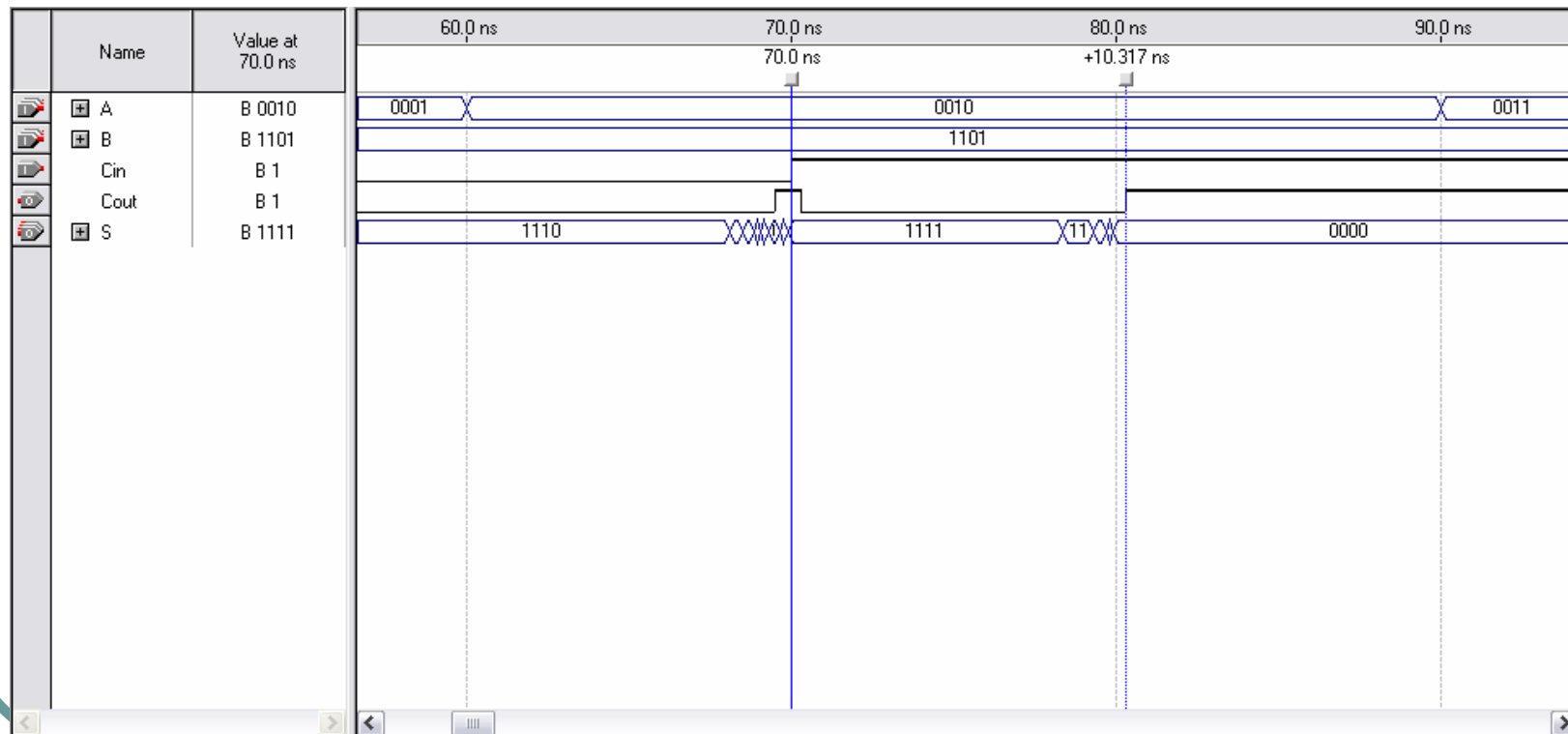
Simulate the design

- Go back to the simulator tool, and click on the button *Start* . `adder4.vwf` will be updated after the simulation.

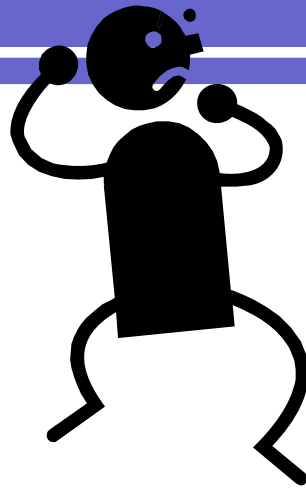


Simulate the design

- The correctness of the design is verified, and the worst delay can be identified.

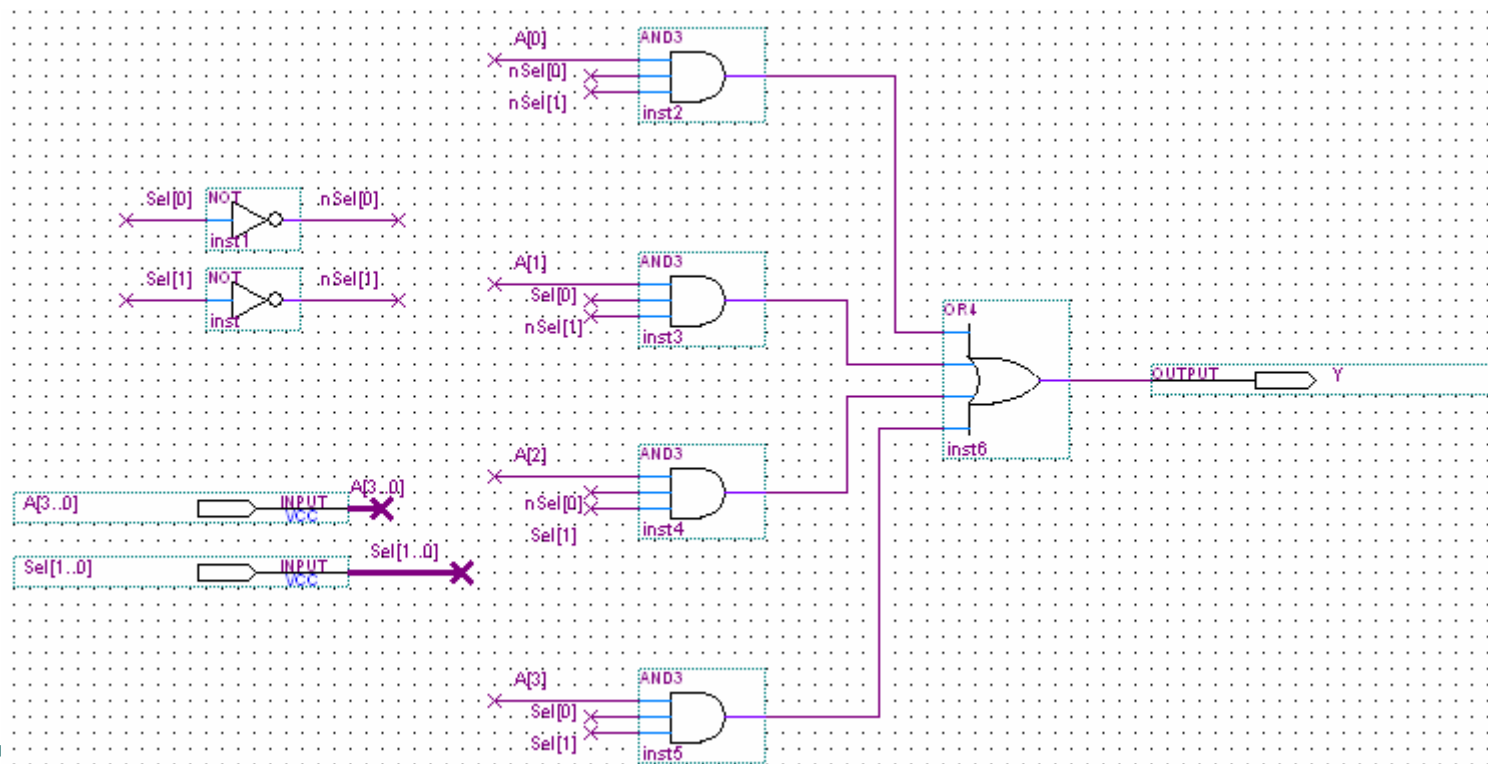


Questions



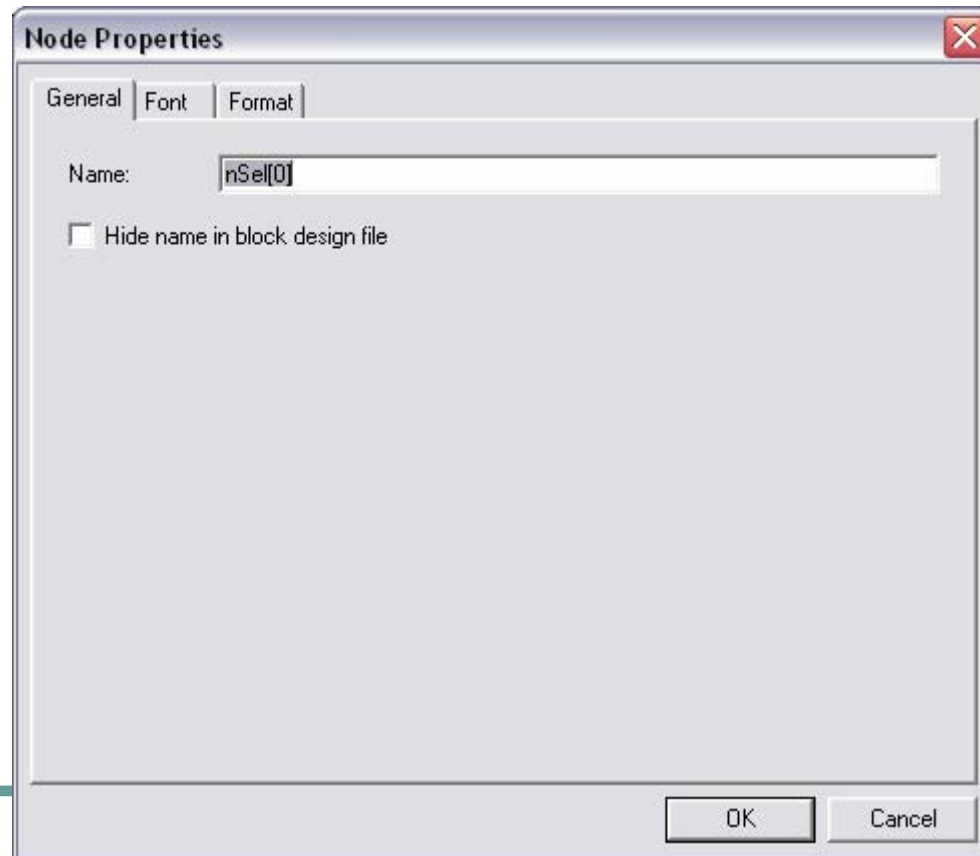
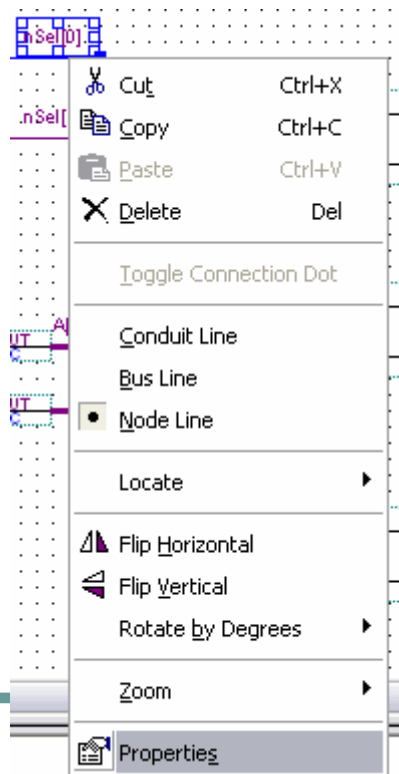
Schematic for 16-bit Multiplexer

- The schematic diagram of a 4-bit Multiplexer. Note that the wires connected by name.



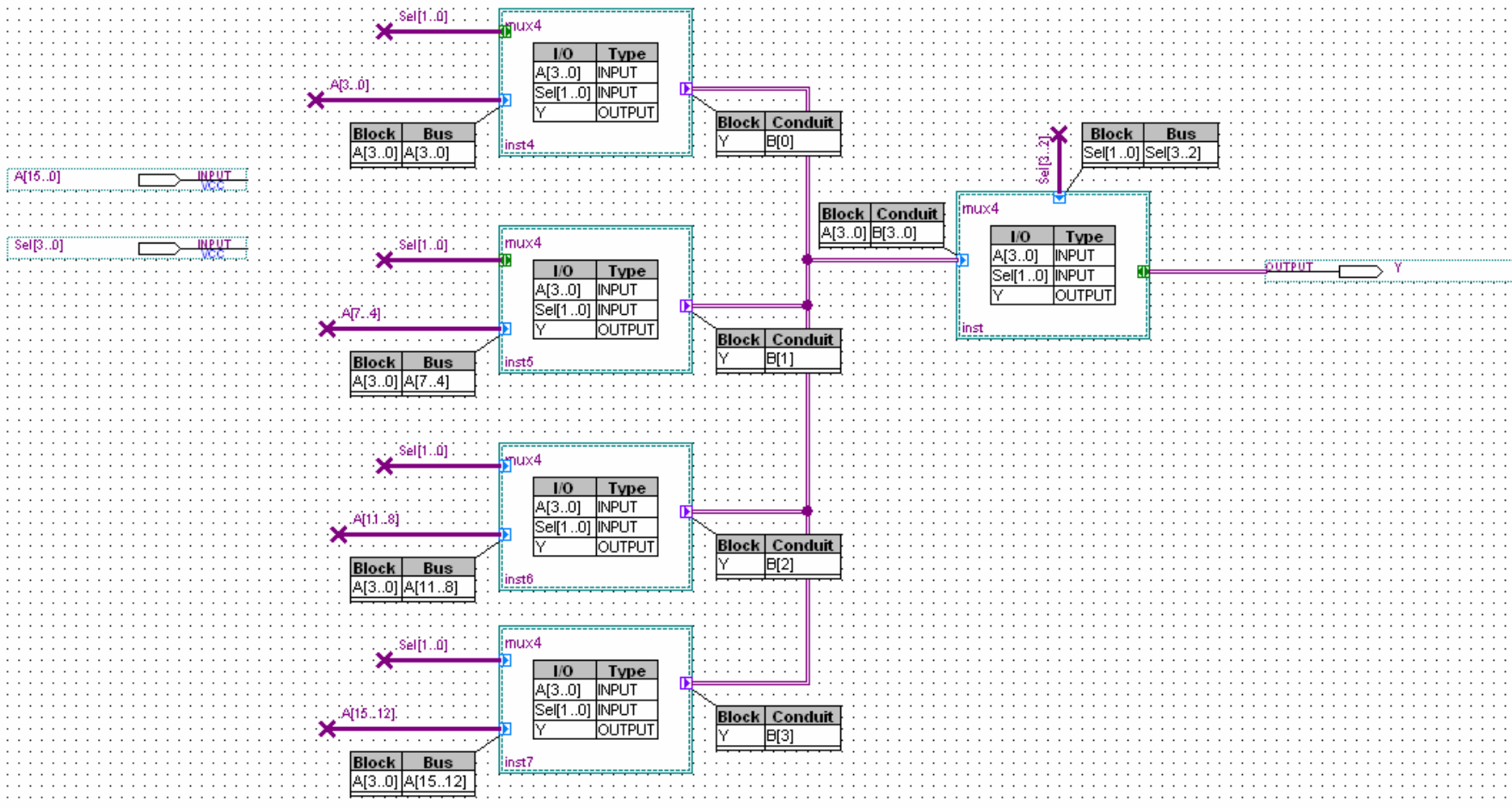
Schematic for 16-bit Multiplexer

- To name a wire/bus, right click the wire/bus, select properties in the pop-up menu, and then fill in the name.



Schematic for 16-bit Multiplexer

- The schematic diagram of a 16-bit Multiplexer.



Questions

