

CSE 140L Lab One

Winter 2006

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**Combinational Circuit Design:
Adder, Subtractor, Multiplexer**

Due time: February 1, 2006

Objective

In this lab, we will build a full-adder, a 2's complement subtractor. Likewise, we will hierarchically build a multiplexer.

We study the functions and the delay of the logics. Use ONE worst case to demonstrate the delay on the critical path. Note that in the lab, we use Altera FPGA Family: Stratix, Device Type: EP1S, Package Type: 144 pin TQFP

Part 1. Tutorial

1. Read Quartus II Installation and licensing for PCs. if you want to download Quartus II to your own PC.
2. Read "Introduction to Quartus II", (Chapter 2: Design Entry, Chapter 3, Constraint Entry, Chapter 4: Synthesis, Chapter 5: Place & Route, Chapter 6: Block-Based Design, Chapter 7: Simulation, Chapter 8: Timing Analysis, Chapter 9: Timing Closure, Chapter 10: Power Analysis)
<http://www.altera.com/products/software/products/quartus2/getting-started/qts-getting-started.html>
3. Watch FPGA Design Demonstrations from Design Entry, Static Timing Analysis, Simulation to Programming
<http://www.altera.com/education/demonstrations/online/design-software/basic/online-fpga-cpld-design.html>
4. Read "Quartus II Introduction for VHDL Users" or "Quartus II Introduction for Verilog Users"

Write a summary commenting on the overall process of using Altera devices and how to avoid the possible mistakes in less than 100 words.

Part 2. Full Adder and Subtractor

- I. Base on 2's complement arithmetic's that we learned Build a full adder/subtractor using Altera QuartusII program. Simulate the behavior of the

- logic to verify the function. Use the post-place&route simulation to demonstrate the worst delay of the circuit. Mark the amount of the delay.
- II.** Using the full adder/subtractor built in I, build a 4-bit adder/subtractor & simulate the 4-bit adder/subtractor. Verify the function and demonstrate the worst delay of the circuit. Mark the amount of the delay.
 - III.** Using the 4-bit adder/subtractor block built in II, build a 16-bit adder/subtractor & simulate the 16-bit adder/subtractor. Verify the function and demonstrate the worst delay of the circuit. Mark the amount of the delay.

Part 3. Multiplexers

- I.** Build a circuit that translates a 4-bit parallel data to a serial output (i.e., A,B,C,D data input lines, and two bits of select input lines, one output line) using only 2:1 Muxes. Define the specification for this 4-bit parallel to serial circuit. (input, output & their relationship)
- II.** Build & simulate the circuit. Verify the function and demonstrate the worst delay of the circuit. Mark the amount of the delay.
- III.** Using the 4:1 Mux block built in I, build & simulate a 16:1 Mux. Verify the function and demonstrate the worst delay of the circuit. Mark the amount of the delay. If you can't find a test bench to demonstrate the worst delay, explain why.

Part 4. Extra Credit- not mandatory, only you want to learn more about arithmetic circuit design

- I.** Try different design approaches to design the adder on a 16 bit carry bypass (or skip) adder or carry lookahead adder (input, output & their relationship) Build & simulate the circuit. Verify the function and demonstrate the worst delay of the circuit. Mark the amount of the delay.
- II.** Compare the worst case delay of this circuit with Part 2 Explain the reason of your observation.

Report

Title page:

Names of students and due date.

- Title of the lab and objective.
- A brief description of each person's contribution.

Content:

- Part 1 summary of overall process in Altera. (100 words or less!)
- Part 2: I, II, III (schematics diagram, behavior simulation diagram, timing report, post-place&route simulation diagram, as in tutorial).
- Part 3: I (function table), II (schematics diagram, behavior simulation diagram, timing report, post-place&route simulation diagram), III (schematics diagram,

behavior simulation diagram, timing report, post-place&route simulation diagram, and explanation if necessary).

- Part 4: I, II, III (schematics diagram, behavior simulation diagram, timing report, post-place&route simulation diagram) Comparison with Part 2

Grading

90% will be based on the completeness and correctness of the report.
10% will be based on the neatness, organization, and following instruction of the report format.