

CSE140L Course Overview

What is CSE140L?

CSE140L is a largely hands-on lab class, which emphasizes independent work. You will be designing digital circuits and then implementing your designs using FPGA and Altera Design tool QuartusII. The emphasis of this course is to help you to learn the digital system design on FPGA device.

There is no set lab meeting time – you have 24-hour access to the facilities and may work at any time.

What is required?

You must complete four lab projects. A written report is required with every lab. There will be one final exam during the quarter covering the lectures and the lab material.

your work must be finished by the last day of classes, **NO INCOMPLETES** will be given.

Class Time: W 10:00-11:30 a.m. (

Lecture Room: HSS.1330

Lab Room: B230,B240,B250,B260,B270

Instructor: Thomas Y. P. Lee

Email: yunparn_lee@yahoo.com (may change later)

TA Office Hours: post on web board

TA: Jinhua Liu

Office Hours: TBD

Office Hours: Hours are subject to change and will be posted on the web. Please check the web page periodically for announcements and changes to the office hours.

Exam: There will be a 1.5-hour exam given on the final week.

Required Text: There is no required text.

Grading: Projects account for 70% of the final grade and the final exam make up the remaining 30%.

Late Penalty: It is very important to stay on track with this course. There will be no free late days or extensions given.