

CSE 140L Lab Two, Winter 2006,

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The Specification and Usage of Flip-Flops

Due Date: February 15, 2006

Objective

In this lab, we learn the specification and usage of flip-flops. We design and implement a serial to parallel shift register, three different counters, and a pseudo-random sequencer.

Note that in the lab, we use Altera FPGA Altera FPGA Family: Stratix, Device Type: EP1S, Package Type: 144 pin TQFP

Part 1. Serial to Parallel Shift Register

Build a 4-bit serial to parallel shift register using four DFFs (Altera Library).

- i. Design and implement the circuit.
- ii. Observe the critical path and timing closure floorplan
- iii. Verify the correctness of the function and demonstrate the critical path by timing simulation. Show at least 8 clock cycles.

Part 2. Asynchronous Counter

Build a 4-bit asynchronous counter using four TFFEs (Altera Library) and invertors.

- i. Design and implement the circuit.
- ii. Observe the timing closure floorplan
- iii. Build an 8-bit asynchronous counter, and create a test bench as follow: Clock period: 10ns; offset: 0ns; duty cycle: 50%; CLR is valid until 40ns; the counter is enabled after 60ns. Simulate the test bench and mark the time point where the counter fails, explain why it fails.

Part 3. Synchronous Counter

Build a 4-bit synchronous counter using four DFFs and combinational gates.

- i. Design and implement the circuit.
- ii. Observe the critical path and timing closure floorplan
- iii. Verify the correctness of the function and demonstrate the critical path by timing simulation. Show at least 16 clock cycles.

Part 4. Gray Counter

Build a 4-bit Gray Counter using four TFFEs (Altera Library) and combinational gates. Design and implement the circuit.

- i. Design and implement the circuit.
- ii. Observe the critical path and timing closure floorplan
- iii. Verify the correctness of the function and demonstrate the critical path by timing simulation. Show at least 16 clock cycles.

Part 5. Pseudo Random Sequencer

Build a 4-bit Pseudo Random Sequencer using four DFFEs (Altera Library) and one XNOR gate. The initial value is "0000".

- i. Design and implement the circuit.
- ii. Observe the critical path and timing closure floorplan
- iii. Verify the correctness of the function and demonstrate the critical path by timing simulation. Show at least 16 clock cycles..

Report

Title page:

- Names of students and due date.
- Title of the lab and objective.
- A brief description of each person's contribution.

Content:

- Part 1 i (schematic diagram), ii (timing report, timing closure floorplan), iii (post-place&route simulation diagram).
- Part 2 i (schematic diagram), ii (timing closure floorplan), iii (post-place&route simulation diagram, explanation).
- Part 3 i (schematic diagram), ii (timing report, timing closure floorplan), iii (post-place&route simulation diagram).
- Part 4 i (schematic diagram), ii (timing report, timing closure floorplan), iii (post-place&route simulation diagram).
- Part 5 i (schematic diagram), ii (timing report, timing closure floorplan), iii (post-place&route simulation diagram).

- Use a table to list the advantages and disadvantages of the three counters in parts 2-4.

Grading

90% will be based on the completeness and correctness of the report.

10% will be based on the neatness, organization, and following instruction of the report format.