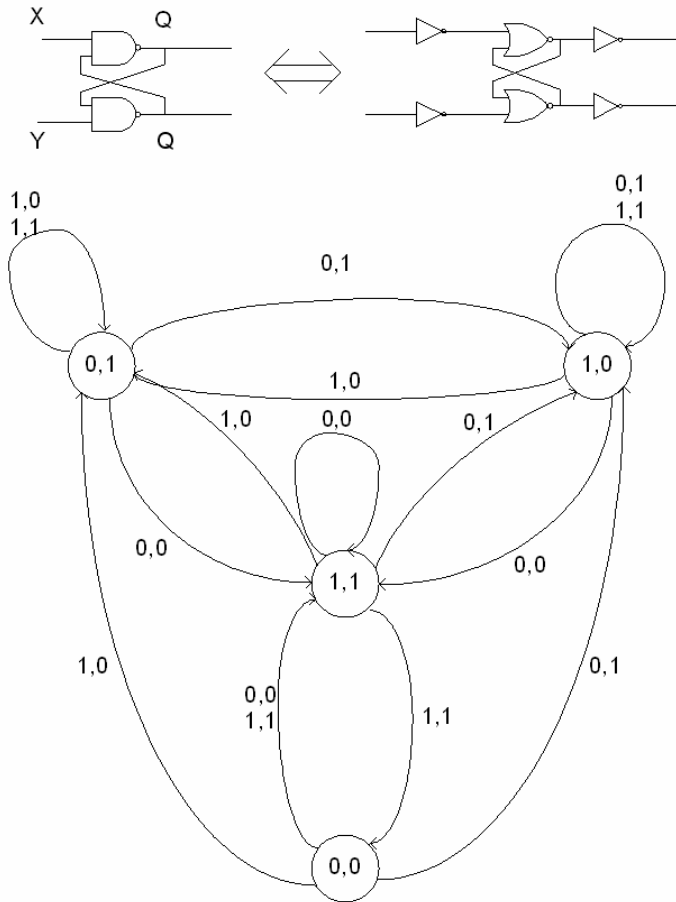


6.1



Truth table:

X	Y	Q	Q'	Q(t+1)	Q'(t+1)	Q(t+2)	Q'(t+2)	Q(t+3)	Q'(t+3)
0	0	0	0	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1
0	1	0	0	1	1	1	0	1	0
0	1	0	1	1	1	1	0	1	0
0	1	1	0	1	0	1	0	1	0
0	1	1	1	1	0	1	0	1	0
1	0	0	0	1	1	0	1	0	1
1	0	0	1	0	1	0	1	0	1
1	0	1	0	1	1	0	1	0	1
1	0	1	1	0	1	0	1	0	1
1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	1	0	1
1	1	1	0	1	0	1	0	1	0
1	1	1	1	0	0	1	1	0	0

Reset: $(X, Y) = (1, 0)$
 Hold: $(X, Y) = (1, 1)$

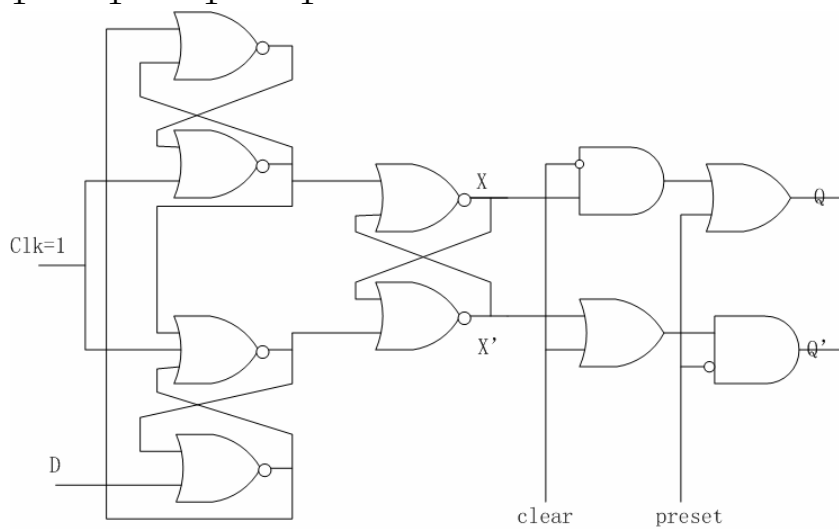
Set: $(X, Y) = (0, 1)$
 Forbidden inputs: $(X, Y) = (0, 0)$.

6.4

p: preset		c: clear	
p	c	x	Q
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

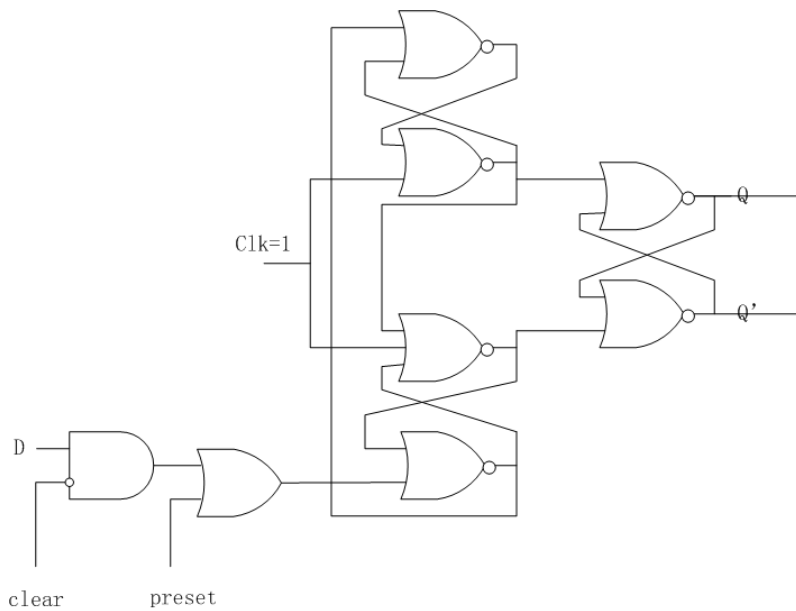
$$Q = p + c'x$$

$$Q' = p'(c + x')$$



6.5

Synchronize preset and clear with clock signal. Add combinational controlled by preset and clear before flip-flop.

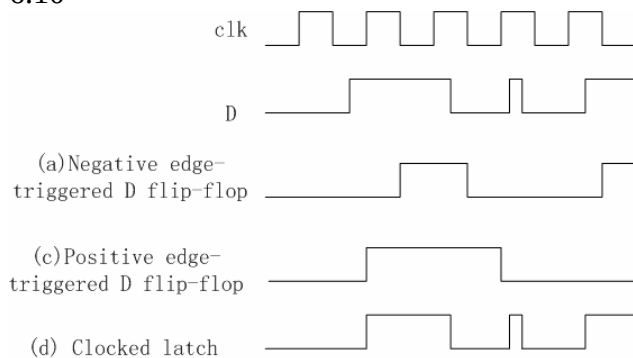


6.8

When $Q(t) = 0$, and $RS = 00$, the R-S master-slave latch should hold, that is, $Q(t+1) = 0$. However, a glitch to 1 on S temporarily changes RS to 01. As a result, current state $Q(t)$ of the master latch is changed from 0 to 1. When S goes back to 0 after the glitch, the master latch will hold the state $Q(t) = 1$ which is set by the glitch. Finally, next state $Q(t+1) = 1$, which is incorrect.

Yes. If the latches were constructed from NAND gates instead of NOR gates, it can catch 0s.

6.10



6.12

(a): (3) and (5)

(b): (8)

(c): negative edge triggered T flip-flop

(d): (1)

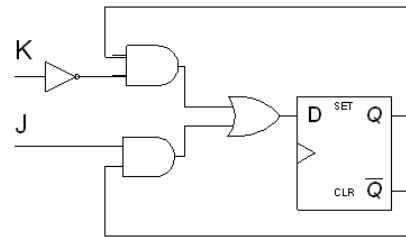
(e): (7) (logic 1 enabled)

6.13

Truth table

J	K	Q(t)	Q(t+1) = D(t)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$D = JQ' + K'Q$$



6.15

So,

D(t)	Q(t)	Q(t+1)	T(t)
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

From the above truth table, $T = D'Q(t) + DQ'(t) = D \text{ xor } Q(t)$

