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CSE 144 / 244

VLSI Testing

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Reference Text

Testing of Digital Systems
Jha + Gupta

Midterm

Final

Homeworks

Testing of Digital Circuits (Systems) ^{1.3}

Testing - an experiment
apply input (test)
analyze output (response)
determine if response
is correct.

detection

error : incorrect response

Possible causes of error

Design error (verification test)

Fabrication errors

(incorrect component
wiring)

Fabrication defects

(shorts + open circuits)

Physical faults

(which occur during
lifetime of circuit)

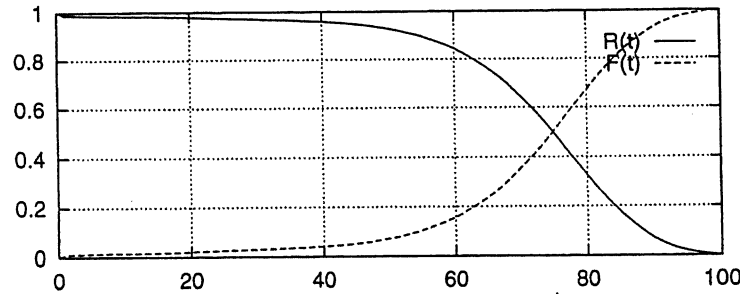
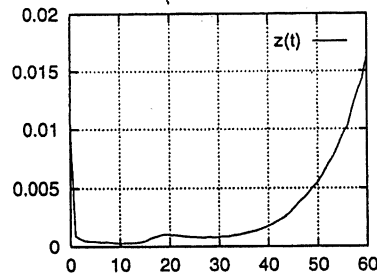
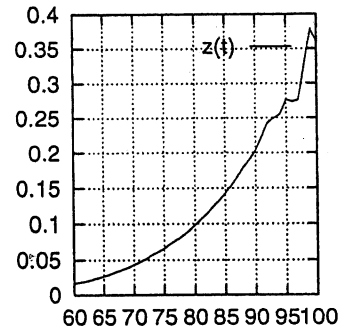
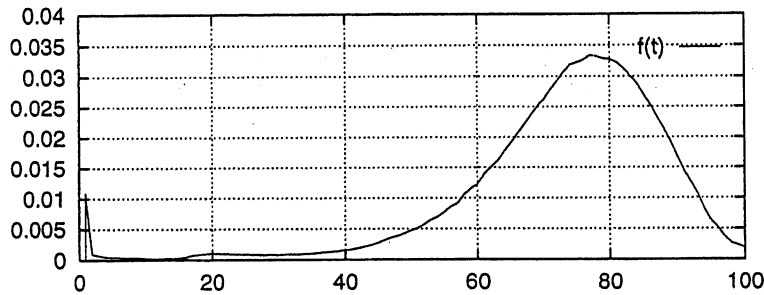
(a) $R(t)$, $F(t)$ vs years(b) $z(t)$ vs younger years(c) $z(t)$ vs older years(d) $f(t)$ vs years

Figure 1.1 Life expectancy of a human population

The Human "Machine"

$R(t)$ = probability of survival to time t

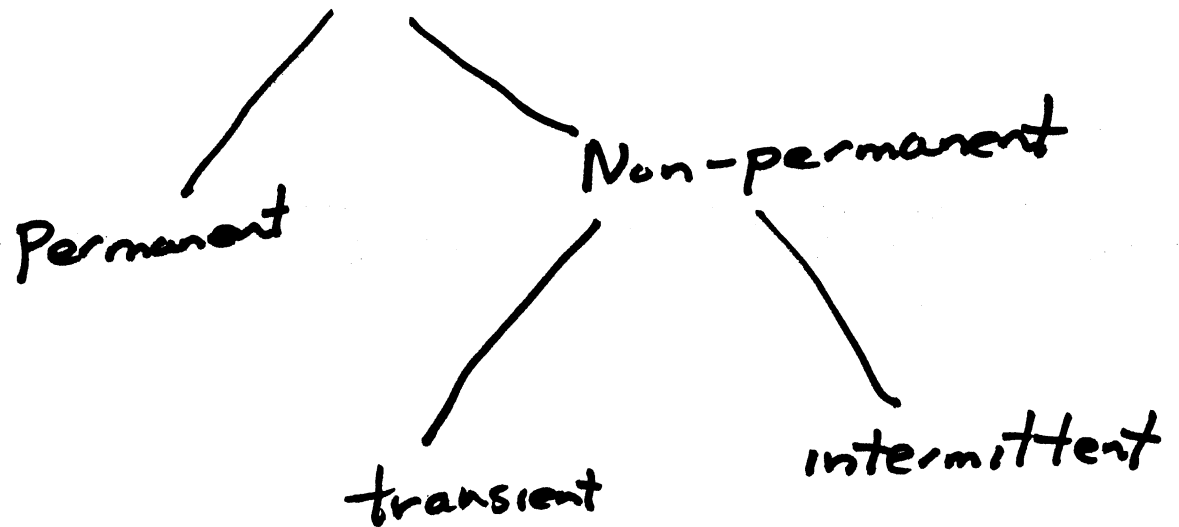
$F(t) = 1 - R(t)$ = probability of death to time t

$f(t) = \frac{dF(t)}{dt}$ (failure probability density)

$z(t) = \frac{f(t)}{R(t)}$ (failure rate)

Faults

Permanent or non-permanent



Transient - caused by environment
(solar storms, temperature, pollution)

Intermittent - non-environmental
(loose connection, aging
electronic component)

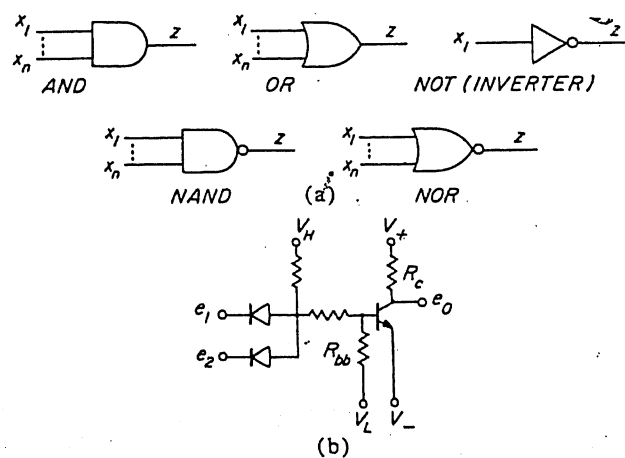
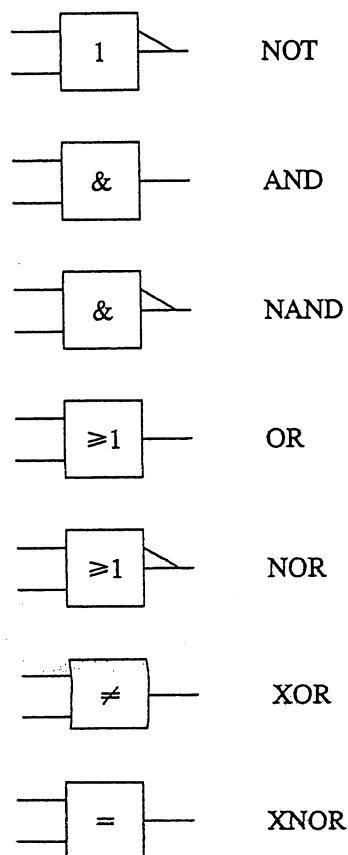


Figure 1.1 (a) Common Gate Types (b) NAND Gate Circuit.

Gate symbols



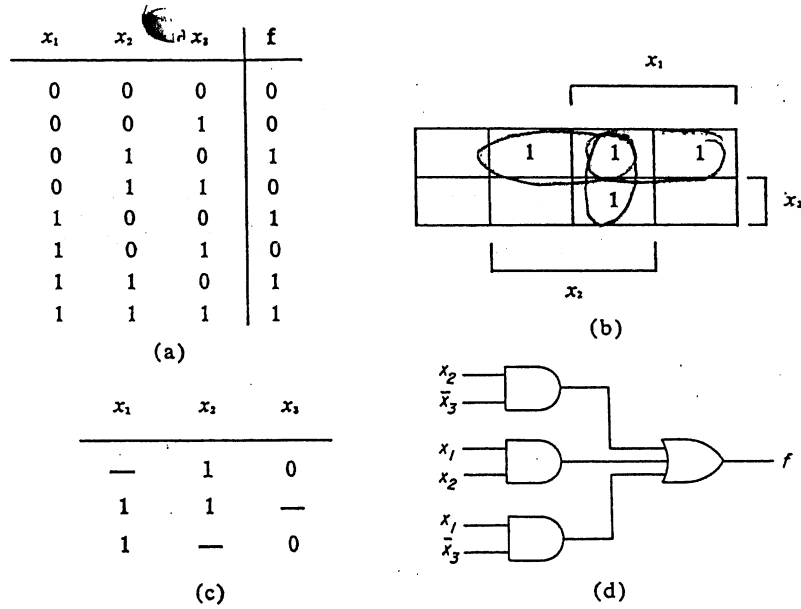


Figure 1.2 Forms for representing a combinational function $f(x_1, x_2, x_3)$ (a) Truth Table (b) Karnaugh map (c) Minimal covering of 1-points (d) Circuit realization

	x	
	0	1
1	2,1	3,0
2	2,1	4,0
3	1,0	4,0
4	3,1	3,0

$N(q,I), Z(q,I)$

Figure 1.4 Example State Table

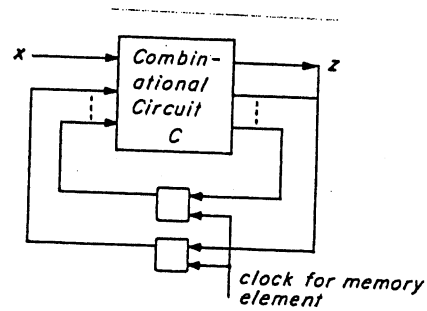


Figure 1.5 Canonical Form for a Synchronous Sequential Circuit

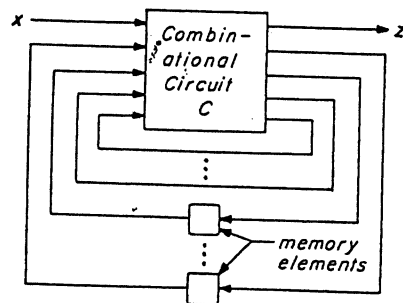


Figure 1.8 Canonical Form for an Asynchronous Circuit

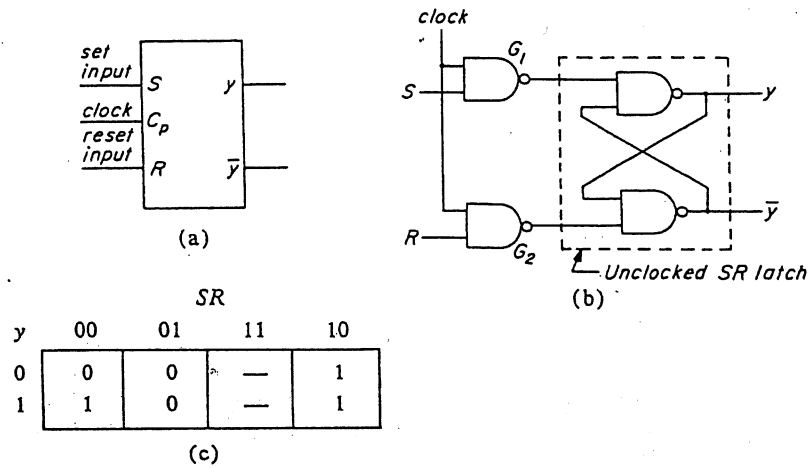


Figure 1.6 Three representations for a SR Flip-Flop (a) Functional representation (b) Circuit representation (c) State table

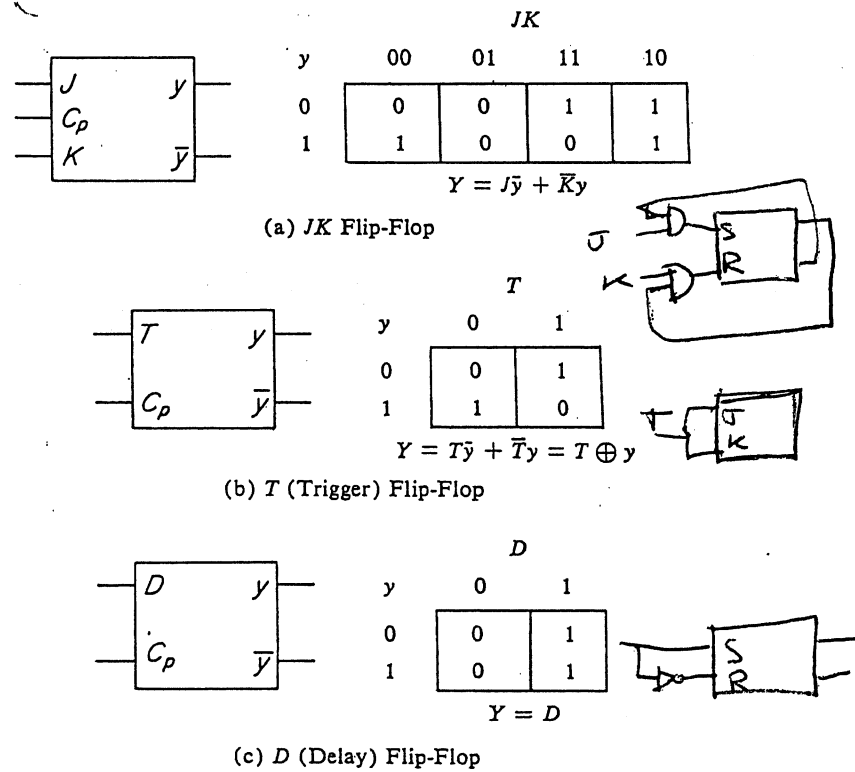


Figure 1.7 Three Types of Flip-Flops

Criterion	Attribute of testing method	Terminology
When is testing performed?	• Concurrently with the normal system operation • As a separate activity	On-line testing Concurrent testing Off-line testing
Where is the source of the stimuli?	• Within the system itself • Applied by an external device (tester)	Self-testing External testing
What do we test for?	• Design errors • Fabrication errors • Fabrication defects • Infancy physical failures • Physical failures	Design verification testing Acceptance testing Burn-in Quality-assurance testing Field testing Maintenance testing
What is the physical object being tested?	• IC • Board • System	Component-level testing Board-level testing System-level testing
How are the stimuli and/or the expected response produced?	• Retrieved from storage • Generated during testing	Stored-pattern testing Algorithmic testing Comparison testing
How are the stimuli applied?	• In a fixed (predetermined) order • Depending on the results obtained so far	Adaptive testing
How fast are the stimuli applied?	• Much slower than the normal operation speed • At the normal operation speed	DC (static) testing AC testing At-speed testing
What are the observed results?	• The entire output patterns • Some function of the output patterns	Compact testing
What lines are accessible for testing?	• Only the I/O lines • I/O and internal lines	Edge-pin testing Guided-probe testing Bed-of-nails testing Electron-beam testing In-circuit testing In-circuit emulation
Who checks the results?	• The system itself • An external device (tester)	Self-testing Self-checking External testing

Figure 1.2 Types of testing

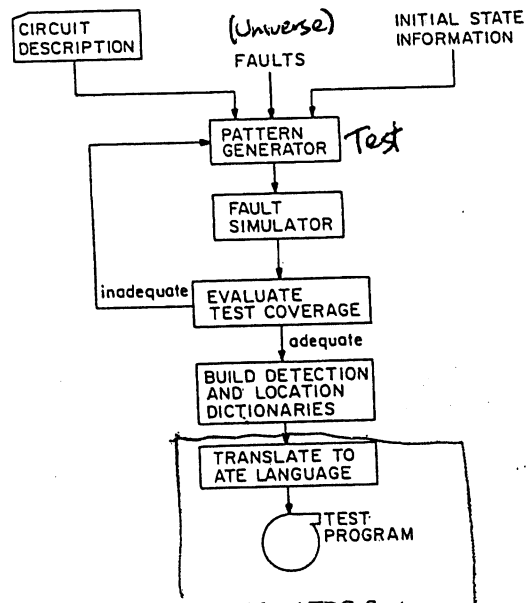


Figure 1.16 ATPG System

Case 1
 X, Z known (fixed)

Case 2
 X changes $\rightarrow Z$ changes
 compare UUT with known good unit

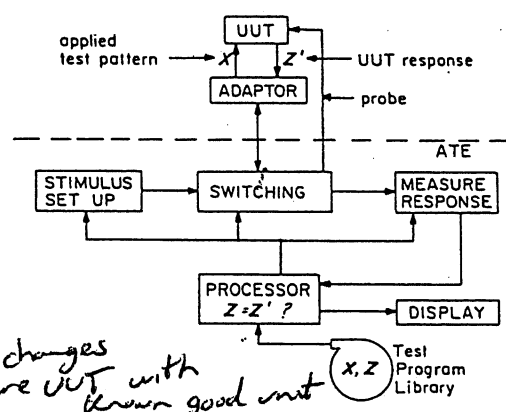
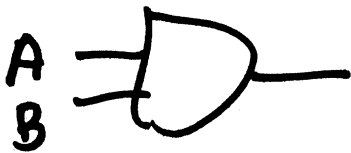


Figure 1.15 Stored Program Automatic Test Equipment (ATE) System Configuration

Logical Faults
affect logic function realized
by element

Normal f
Fault f'

Example



		A	
	B		
			1
		f	

		A	
	B		1
			1
		f'	

We model physical faults as
logical faults

1.13

Advantages

- Reduces complexity
(many physical faults may be modeled by same logical fault)
- Technology independent
Same logical fault applicable to many technologies
- Tests for logical faults may be used to detect physical faults whose affect on circuit is complex and not completely understood

Most commonly used logical
fault model

1.14

Single stuck at fault model

Some gate ~~output~~ (behaves as if)
its output is stuck at 1
(s-a-1) or stuck at 0
(s-a-0) or one of its
inputs is s-a-1 or s-a-0.
or a circuit input or output
behaves as if it is stuck

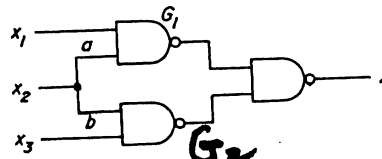


Figure 1.18

For fault x_2 s-a-1 (input)
both a & b are stuck

For fault a s-a-1 (on G_1)
 a is stuck but G_2
behaves normally

for fault b s-a-1 (on G_2)
 b is stuck but G_1
behaves normally

If there are k signals
 $2k$ single stuck faults

In above circuit $k = 8$

$\Rightarrow 16$ single stuck faults

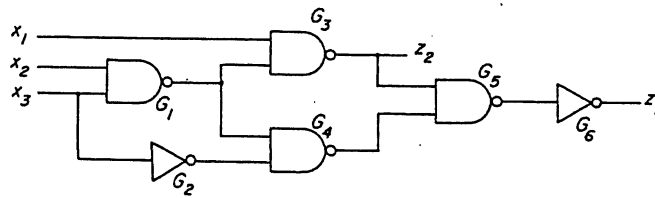


Figure 1.3 Circuit Demonstrating Reconvergent Fanout

Fanout
 Reconvergent fanout
 Important concepts in testing

Fanout - a signal is input
 to more than one gate

Reconvergent fanout -
 two (or more) paths from a
 signal source to inputs of the
 same gate.

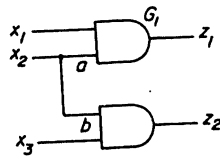


Figure 1.19

Other logical fault types

1. Multiple stuck faults

k signals $\rightarrow$ 2^k single stuck faults
 $\rightarrow 3^k - 1$ single and multiple stuck faults

 k signals

each signal = 0, 1, or N

$NNN \dots N \rightarrow$ normal

all other vectors are faults

2. Bridge fault

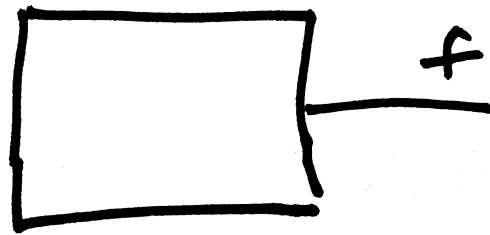
(shorted wires create AND or OR of signals)

In circuit above, OR bridge between x_1 and x_2

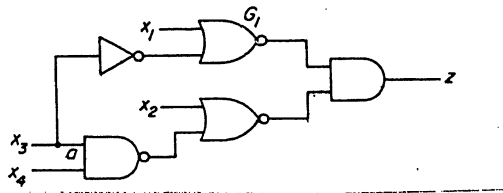
$$z_1' \Rightarrow (x_1 + x_2) \cdot (x_1 + x_2) = x_1 + x_2$$

$$z_2' \Rightarrow (x_1 + x_2) \cdot x_3$$

Develop general procedures for test generation that can be applied to any type of fault which can be described in terms of logical behavior



normal $\rightarrow f$
faulty $\rightarrow f'$



Example

Multiple stuck at fault

x_3 s-a-1 and x_4 s-a-1

$$\begin{aligned} z_{\text{Normal}} &= (\overline{x_1 + x_3}) \cdot (\overline{x_2 + x_3 x_4}) \\ &= (\overline{x_1} \cdot x_3) \cdot (\overline{x_2} \cdot (x_3 \cdot x_4)) \\ &= \overline{x_1} \cdot \overline{x_2} \cdot x_3 \cdot x_4 \end{aligned}$$

$$\begin{aligned} z'_{\text{(Faulty)}} &= (\overline{x_1 + 0}) \cdot (\overline{x_2 + 0}) \\ &= \overline{x_1} \cdot \overline{x_2} \end{aligned}$$

$$T = z \cdot \overline{z'} + z' \cdot \overline{z}$$

$$z=1 \rightarrow z'=1$$

$$z=0 \text{ and } z'=1 \rightarrow x_1=0, x_2=0, x_3=0 \text{ or } x_4=0$$

$$T = \overline{x_1} \cdot \overline{x_2} (x_3 + x_4)$$

Exhaustive Testing

(4.7)

Apply all possible inputs -
will detect any fault if it
is permanent (not intermittent)
and present at the beginning
of testing.

n inputs $\rightarrow 2^n$ tests

Algebraic Testing

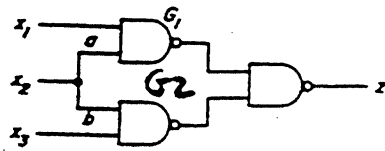
Compute f, f_α

$$T = f \oplus f_\alpha$$

Both impractical

Stuck at Fault Model

(4.8)



Normal Circuit $z = x_1x_2 + x_2x_3$

Fault α x_2 s-a-1 $z_\alpha = x_1 + x_3$

A signal which fans out to 2 + gates may appear normal at one gate and faulty (s-a) at another gate

Fault β - Input a of G_1 s-a-1

$$z_\beta = x_1 + x_2x_3$$

Fault γ - Input b of G_2 s-a-1

$$z_\gamma = x_1x_2 + x_3$$

If circuit ^{has} k input signals, gate inputs ^(I.O) & outputs in total

$\Rightarrow 2k$ single s-a. faults

$\Rightarrow 3^k - 1$ possible multiple
s-a faults

Rationales for single fault assumption

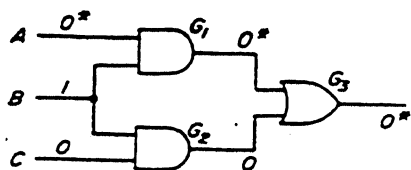
* Multiple faults do not occur
because single fault is detected
before second fault occurs

* Tests which detect single
fault ~~will~~ will also detect
multiple faults.

Although there are exceptions in
general these assumptions are usually
valid and are usually used.

Combinational Circuit Test Generation

4.10



Fault $\alpha \rightarrow A$ s-a-1

$$f = AB + BC$$

$$f_{\alpha} = B + BC = B$$

$$\begin{aligned} f \oplus f_{\alpha} &= (AB + BC) \oplus B \\ &= \bar{A}B\bar{C} \end{aligned}$$

Test has two properties

- ① Applies "opposite value" at site of fault
- ② Defines path of * from site of fault to output

* $\rightarrow$ Normal & faulty circuits have opposite values

"Sensitized" path

Detects faults along path

G_1 s-a-1

G_3 s-a-1

Also detects some faults
not along path

C s-a-1

Fault σ C-s-a-1

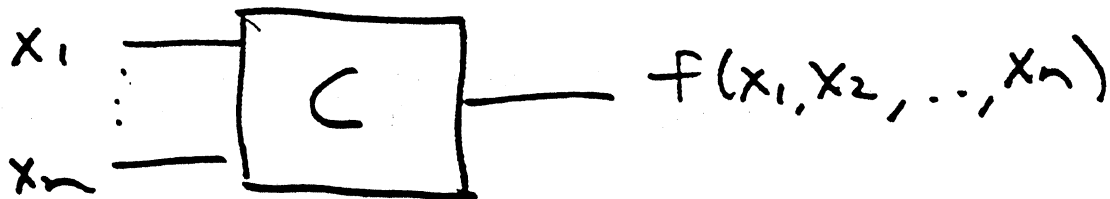
$$f_{\sigma} = AB + B = B(A+1) = B$$

$$f \oplus f_{\sigma} = B \cdot (\overline{AB + BC})$$

$$= B \cdot \bar{A} \cdot \bar{C}$$

Boolean Difference (Algebraic Approach to Test Generation)

(4.12)



Let

$$f(x_1, x_2, \dots, x_{i-1}, 0, x_{i+1}, \dots, x_n) \equiv f_i(0)$$

and

$$f(x_1, x_2, \dots, x_{i-1}, 1, x_{i+1}, \dots, x_n) \equiv f_i(1).$$

The set of tests which detect the fault $\alpha(x_i \rightarrow 0)$ corresponds to the 1-points of the function

$$\begin{aligned} T &= f(x) \cdot \bar{f}_\alpha(x) + \bar{f}(x) \cdot f_\alpha(x) \\ &= f(x) \oplus f_\alpha(x). \end{aligned}$$

Since $F_\alpha(x) = f_i(0)$, by Shannon's expansion theorem, we have that

$$\begin{aligned} T &= (\bar{x}_i \cdot f_i(0) + x_i \cdot f_i(1)) \oplus f_i(0) \\ &= x_i \cdot f_i(1) \cdot \bar{f}_i(0) + x_i \cdot \bar{f}_i(1) \cdot f_i(0) \\ &= x_i \cdot (f_i(1) \oplus f_i(0)). \end{aligned}$$

$f_i(1) \oplus f_i(0)$ = Boolean difference
of f with ~~with~~ respect to x_i

$$\frac{df}{dx_i}$$

1-pts of

(4.13)

$$x_i \cdot \frac{df}{dx_i} = \text{set of all tests}$$

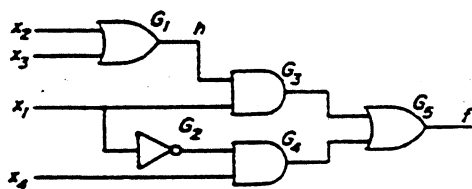
which detect fault x_i s-a-0

1-pts of

$$\bar{x}_i \cdot \frac{df}{dx_i} = \text{set of all tests}$$

which detect fault x_i s-a-1

Example



$$f = (x_2 + x_3) \cdot x_1 + \bar{x}_1 x_4$$

1-pts of $x_i \cdot \frac{df}{dx_i}$ detect fault x_i s-a-0

$$\begin{aligned} \frac{df}{dx_1} &= f(0, x_2, x_3, x_4) \oplus f(1, x_2, x_3, x_4) \\ &= x_1 \oplus (x_2 + x_3) \\ &= \bar{x}_2 \bar{x}_3 x_1 + x_2 \bar{x}_1 + x_3 \bar{x}_1 \end{aligned}$$

$$x_1 \cdot \frac{df}{dx_1} = x_1 \bar{x}_2 \bar{x}_3 x_4 + x_1 x_2 \bar{x}_4 + x_1 x_3 \bar{x}_4$$

Tests $\rightarrow (1, 0, 0, 1), (1, 1, -, 0), (1, -, 1, 0)$

(7.69)

For the fault X_4 s-a-1

$$\begin{aligned}\bar{X}_4 \cdot \frac{dF}{dX_4} &= \bar{X}_4 (X_1(X_2+X_3) \oplus (X_1(X_2+X_3) + \bar{X}_1)) \\ &= \bar{X}_1 \bar{X}_4\end{aligned}$$

$\Rightarrow$ Tests are $(0, -, -, 0)$

Boolean Difference Identities

$$\frac{df(x)}{dx_i} = \frac{df(x)}{dx_i} \quad (1)$$

$$\frac{d[f(x) \cdot g(x)]}{dx_i} = f(x) \cdot \frac{dg(x)}{dx_i} \oplus g(x) \cdot \frac{df(x)}{dx_i} \oplus \frac{df(x)}{dx_i} \cdot \frac{dg(x)}{dx_i} \quad (2)$$

$$\frac{d[\bar{f}(x) + g(x)]}{dx_i} = \bar{f}(x) \cdot \frac{dg(x)}{dx_i} \oplus \bar{g}(x) \cdot \frac{df(x)}{dx_i} \oplus \frac{df(x)}{dx_i} \cdot \frac{dg(x)}{dx_i} \quad (3)$$

$$\frac{d[f(x) \oplus g(x)]}{dx_i} = \frac{df(x)}{dx_i} \oplus \frac{dg(x)}{dx_i} \quad (4)$$

Proof of #2 and #3

$$\begin{aligned}
 & f(x) \cdot \frac{dg(x)}{dx_i} \oplus g(x) \cdot \frac{df(x)}{dx_i} \oplus \frac{df(x)}{dx_i} \cdot \frac{dg(x)}{dx_i} \\
 &= f(x) \cdot (g_i(0) \oplus g_i(1)) \oplus g(x) \cdot (f_i(0) \oplus f_i(1)) \\
 &\quad \oplus (f_i(0) \oplus f_i(1)) \cdot (g_i(0) \oplus g_i(1)) \\
 &= f(x) \cdot (g_i(0) \oplus g_i(1)).
 \end{aligned}$$

Substituting $x_i f_i(1) \oplus \bar{x}_i f_i(0)$ for $f(x)^*$ and factoring we obtain

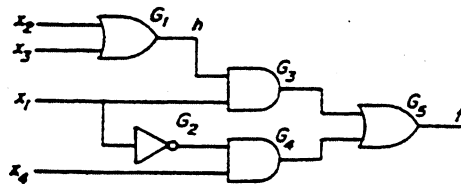
$$\begin{aligned}
 & (f_i(1) \cdot g_i(0) \oplus f_i(0) \cdot g_i(1))(x_i \oplus \bar{x}_i \oplus 1) \\
 &\quad \oplus f_i(1) \cdot g_i(1) \cdot (x_i \oplus x_i \oplus 1) \\
 &\quad \oplus f_i(0) \cdot g_i(0) (\bar{x}_i \oplus \bar{x}_i \oplus 1) \\
 &= f_i(1)g_i(1) \oplus f_i(0)g_i(0) \\
 &= \frac{d(f(x) \cdot g(x))}{dx_i}.
 \end{aligned}$$

The proof of (3) follows directly from (1) and (2) since

$$\frac{d(f(x) + g(x))}{dx_i} = \frac{d(\bar{f}(x) \cdot \bar{g}(x))}{dx_i}.$$

Path Sensitization and the D-algorithm

4.16



Fault h s-a-1

Must make normal value of h = 0

$$\Rightarrow x_2 + x_3 = 0 \Rightarrow x_2 = 0, x_3 = 0$$

Propagate error through G_3

$$\Rightarrow x_1 = 1$$

Propagate error through G_5

$$\Rightarrow G_4 = 0 \Rightarrow \bar{x}_1 x_4 = 0$$

$$\Rightarrow x_1 = 1 \text{ or } x_4 = 0$$

Combining requirements the derived test is $x_1 \bar{x}_2 \bar{x}_3 \Rightarrow (1, 0, 0, -)$

Procedure 2.1 (Path Sensitization): To generate a test to detect a fault in a combinational circuit:

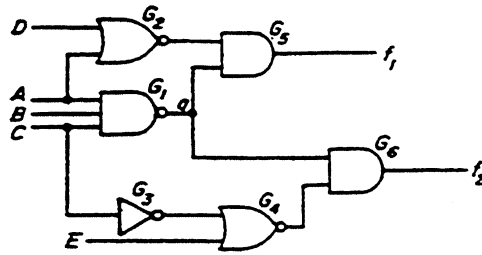
- (1) Specify inputs so as to generate the appropriate value (0 for *s-a-1* and 1 for *s-a-0* faults) at the site of the fault.
- (2) Select a path from the site of the fault to an output and specify additional signal values to propagate the fault signal along this path to the output (*error propagation*).
- (3) Specify input values so as to produce the signal values specified in (2) (*line justification*). □

The rules for error propagation through individual gate elements are simply derived and are summarized in the table of Figure 2.10.

Type of Gate	Restrictions on other gate inputs
AND	All must be 1
OR	All must be 0
NAND	All must be 1
NOR	All must be 0
INVERTER (NOT)	None

Figure 2.10 Rules for Error Propagation

In previous examples all choices were unique.
 In general all choices may have ~~be~~ many possibilities

Example

Fault a (output of G_1) s-a-1

Requires $G_1 = 0$

$$\Rightarrow \overline{ABC} = 0 \Rightarrow A=B=C=1$$

Unique

Path to output

Two Choices G_5 or G_6

$$G_5 \Rightarrow G_2 = 1 \Rightarrow \overline{A+D} = 1$$

$\Rightarrow A=D=0$ Contradiction

$$G_6 \Rightarrow G_4 = 1 \Rightarrow \overline{C+E} = 1$$

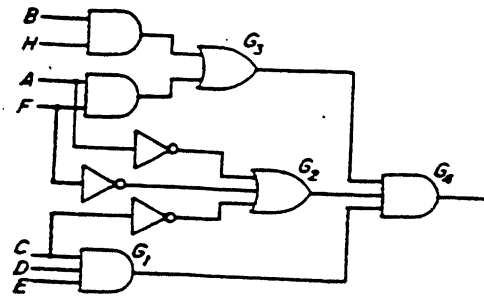
$$\Rightarrow \overline{C} = 0 (C=1), E=0$$

No Contradiction

Test $ABCE \Rightarrow (1, 1, 1, -, 0)$

Choice for Path Sensitization

(4.19)



Fault E s-a-1

Requires $E=0$

Path (Unique) to output G_1, G_4

$$G_1 \Rightarrow C=D=1$$

$$G_4 \Rightarrow G_3=1, G_2=1$$

$$G_3=1 \Rightarrow B=H=1 \text{ or } A=F=1$$

Choose $A=F=1$

$$G_2=1 \Rightarrow A=0 \text{ or } F=0 \text{ or } C=0$$

Contradiction

Backtrack to previous choice for

$$\text{gate } G_3 \Rightarrow B=H=1$$

$$G_2=1 \Rightarrow A=0 \text{ or } F=0 \quad (C \text{ previously defined } 1)$$

$$\text{Test } \bar{A}B\bar{C}D\bar{E}H + B\bar{C}D\bar{E}\bar{F}H$$

$$(0, 1, 1, 1, 0, -, 1) \quad (0, -, 1, 1, 1, 0, 0)$$