

Hw
CSE 147/247
2004

PROBLEMS

- 1.1 a) If possible find a circuit which has some fault which is *undetectable* (i.e., there are no tests which detect the fault).
 b) If possible find a circuit which has two faults α and β which are indistinguishable (i.e., $f_\alpha = f_\beta$).
- 1.2 Is it possible to have a combinational circuit C with some signal S and test T such that T detects both S s-a-1 and S s-a-0? Give an example or prove it impossible.
- 1.3 For the circuit of Figure 1.21 and the following faults find the circuit output.
 a) Shorted diode on a .
 b) AND bridge between inputs to gate G_1 .
 c) The multiple fault: x_3 s-a-1, x_2 s-a-0
- 1.4 In the circuit of Figure 1.21 which if any of the following tests detect the fault x_1 s-a-0?
 a) (0,1,1,1)
 b) (1,1,1,1)
 c) (1,1,0,1)
 d) (1,0,1,0)

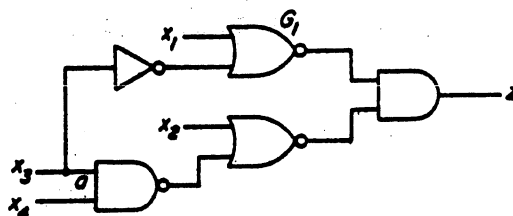


Figure 1.21 Problems 1.3, 1.4, and 1.5.

- 1.5 For the circuit of Figure 1.21 find a Boolean expression for the set of all tests which detect the fault.
 a) x_3 s-a-0
 b) x_2 s-a-0
 c) x_2 s-a-1
- 1.6 For the circuit of Figure 1.22(a) and (b) find a Boolean expression for the set of all tests which distinguish the following pairs of faults.
 a) x_1 s-a-0 and x_3 s-a-1
 b) x_2 s-a-1 and x_3 s-a-0
 c) x_1 s-a-0 and x_3 s-a-0

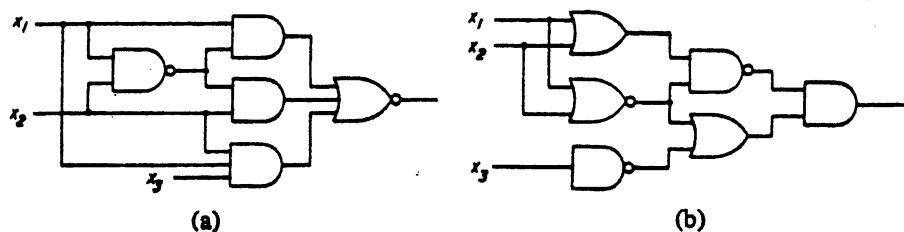


Figure 1.22

- 2.2 For the circuit of Figure 2.52 consider a fault which causes gate G_7 to generate a 1 output if and only if both of its inputs are 0 or both are 1. Find tests which detect this fault by finding the primitive D -cube of the fault and using path sensitization. (Hint: It is easier to find inputs which are *not* tests.)

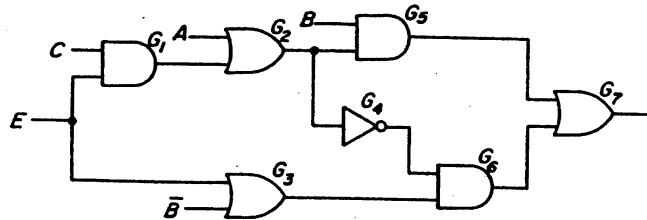


Figure 2.52 Problems 2.2 and 2.3

- 2.3 For the circuit of Figure 2.52, find all tests which detect the multiple fault $A s-a-1, G_6 s-a-0$. Use path sensitization.
- 2.4 For the circuit of Figure 2.53 find all tests which detect the faults
- $A s-a-0$
 - $b s-a-1$
 - $G_2 s-a-1$
 - the multiple fault $b s-a-1, G_2 s-a-1$.
 - Repeat (a) and (b) using the D-algorithm. (Hint: once a test is found, backtrack to the last choice.)
- 2.5 a) For the circuit of Figure 2.53 find all tests which distinguish $A s-a-0$ from $G_2 s-a-1$.
- b) Is there an input which sensitizes both $A s-a-0$ and $G_2 s-a-1$ at the same time? If so, will this input be a test for the multiple fault $A s-a-0, G_2 s-a-1$?

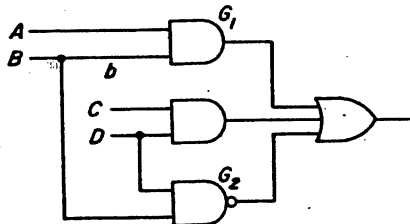


Figure 2.53 Problems 2.4, 2.5 and 2.12

2.6 For the circuit of Figure 2.54

- a) Find all tests which detect the fault $A s-a-1$.
- b) Find all tests which detect the fault $b s-a-0$.
- c) Find all tests which detect the multiple fault $A s-a-1, b s-a-0$.
- d) Find all tests which distinguish the faults $A s-a-1$ and $b s-a-0$.

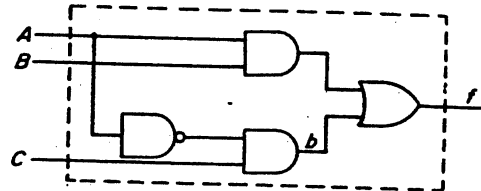


Figure 2.54 Problems 2.6 and 2.7

- 3.4 For the synchronous circuit shown in Figure 3.44, ~~use Procedure 3.1 to~~ derive a test to detect the fault a $s-a-1$, assuming the initial state of the composite circuit is $(y_1, y_2) = (0, 0)$.

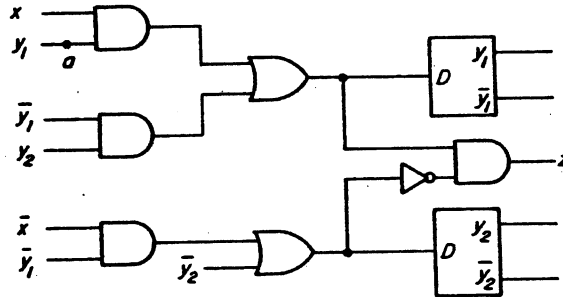


Figure 3.44

- 3.5 For the circuit of Figure 3.5, consider the fault z $s-a-0$.
- Derive a test ~~using Procedure 3.1~~ assuming initial state $(y_1, y_2) = (1, 1)$.
 - Derive a test ~~using Procedure 3.2~~ assuming initial state (u, u) .

2.18 A decoder is a combinational circuit containing n inputs and 2^n outputs, labeled respectively $(x_0, x_1, \dots, x_{n-1})$, and $(z_0, z_1, \dots, z_{2^n-1})$. The circuit functions as follows: If $(a_0, a_1, \dots, a_{n-1})$ is a binary input vector, representing the integer k , then $z_k = 1$ and $z_j = 0$ for all $j \neq k$. Based upon the functional operation of this device, determine a minimal set of tests which will detect any single fault on an input or output line of this device.

2.19 A multiplexer is a combinational circuit C having the structure shown in Figure 2.60.

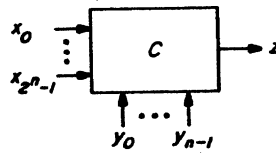


Figure 2.60

If $(a_0, a_1, \dots, a_{n-1})$ is an input vector, representing the integer k , applied to $(y_0, y_1, \dots, y_{n-1})$, then $z = x_k$, where $0 \leq k \leq 2^n - 1$. That is, input line x_k is connected to the output z . Based upon the functional operation of this device, determine a minimal set of tests which will detect any single stuck fault on an input or output line of this device.

3.20 The following I/O sequence is generated by a 3 state machine. The outputs indicated by a_1, a_2, a_3, a_4 are not known. Determine these outputs if possible, and add a minimal number of additional inputs to uniquely determine the machine. If the minimal additional input sequence depends on the output response specify all contingencies.

X = 0 0 0 0 0 0 1 0 0 1 0 0 0

Z = 0 0 1 0 a_1 1 0 1 a_2 0 1 a_3 a_4

5.9 For the circuit in Figure 5.38, determine the faults detected by the test 111 by

~~deductive~~ ^{deductive} ~~consensus~~ fault simulation (start with a collapsed set of faults)

~~deductive fault simulation~~

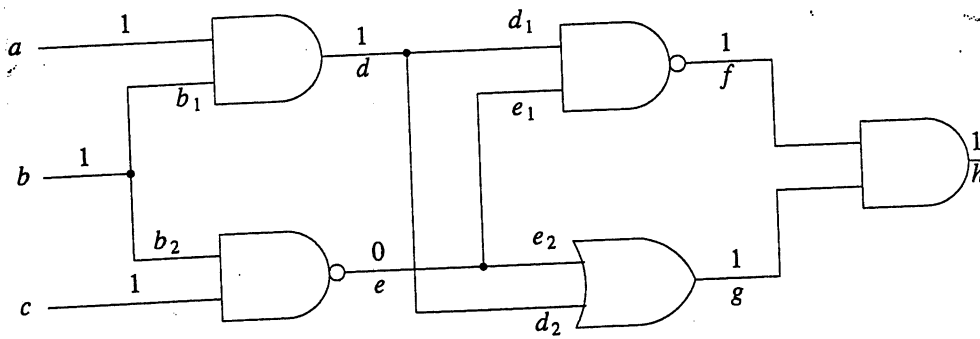


Figure 5.38