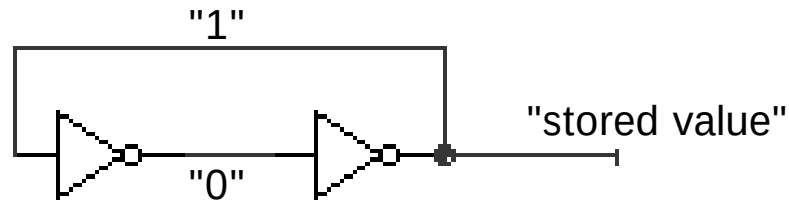
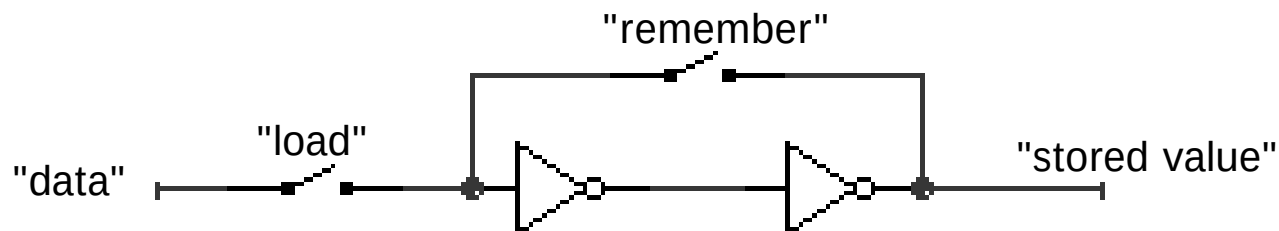


Simplest circuits with feedback

- Two inverters form a static memory cell
 - will hold value as long as it has power applied

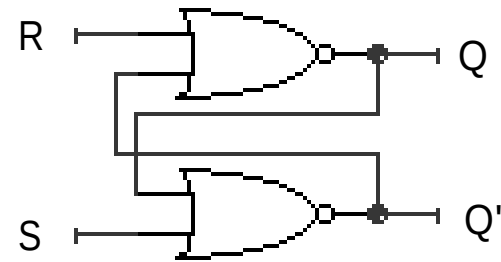
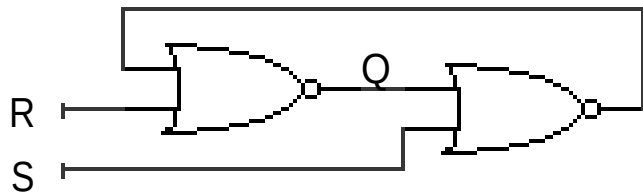


- How to get a new value into the memory cell?
 - selectively break feedback path
 - load new value into cell

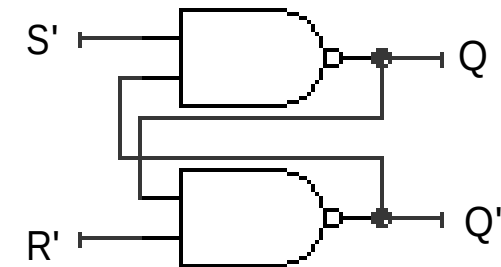
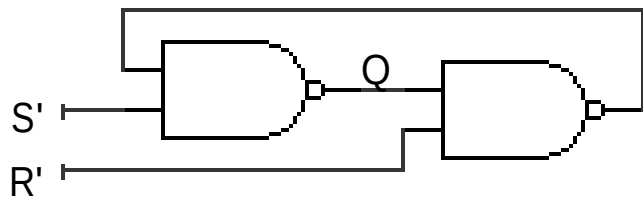


Memory with cross-coupled gates

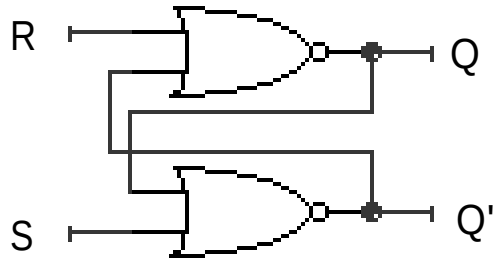
- Cross-coupled NOR gates
 - similar to inverter pair, with capability to force output to 0 (reset=1) or 1 (set=1)



- Cross-coupled NAND gates
 - similar to inverter pair, with capability to force output to 0 (reset=0) or 1 (set=0)



R-S latch analysis



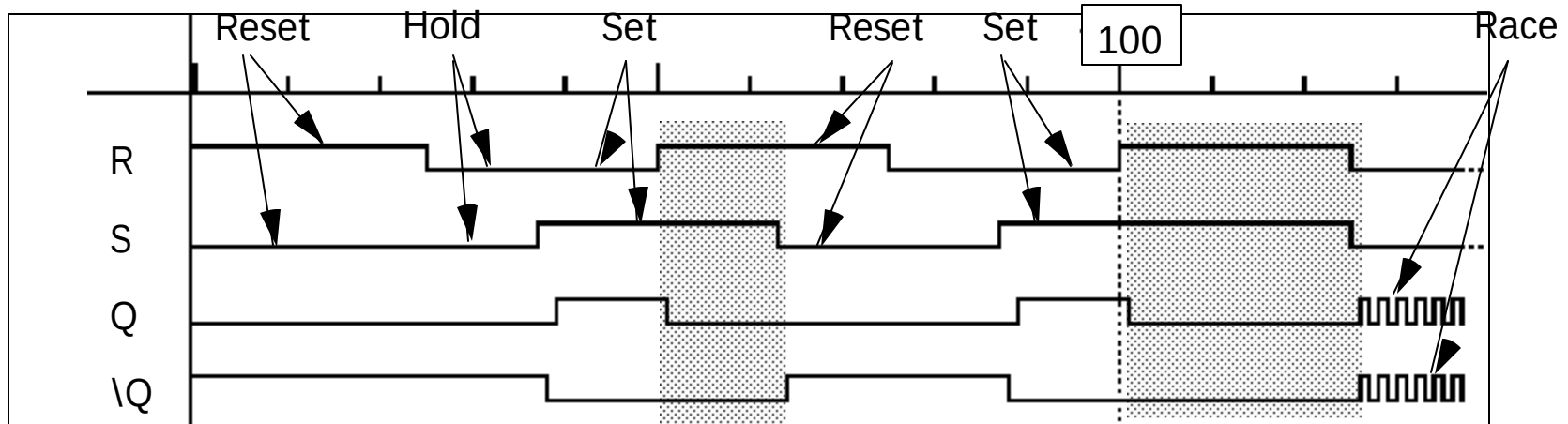
S	R	Q(t)	Q(t+Δ)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

hold

reset

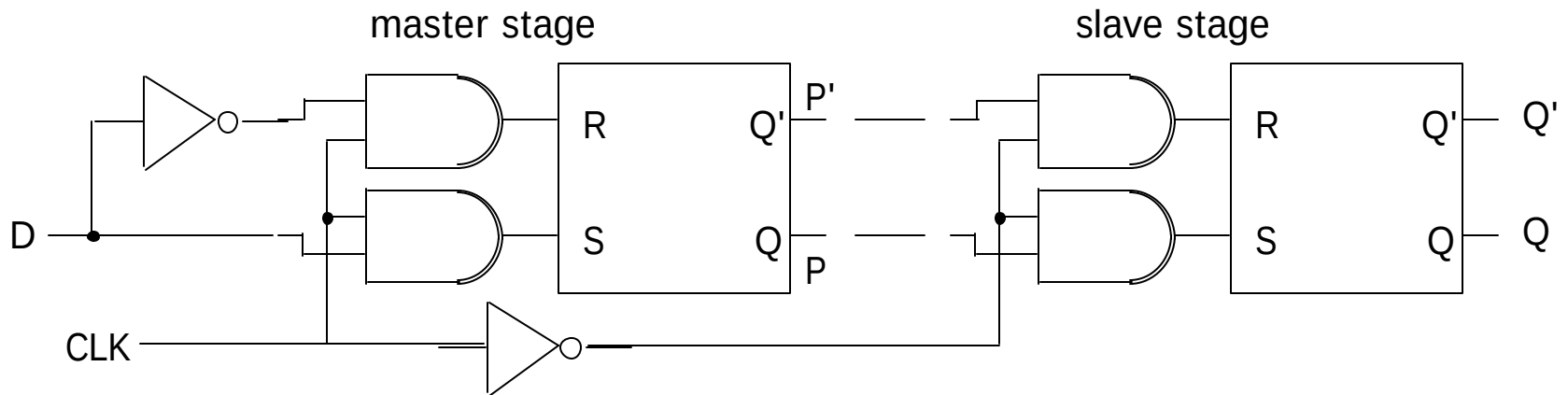
set

not allowed



D flip-flop

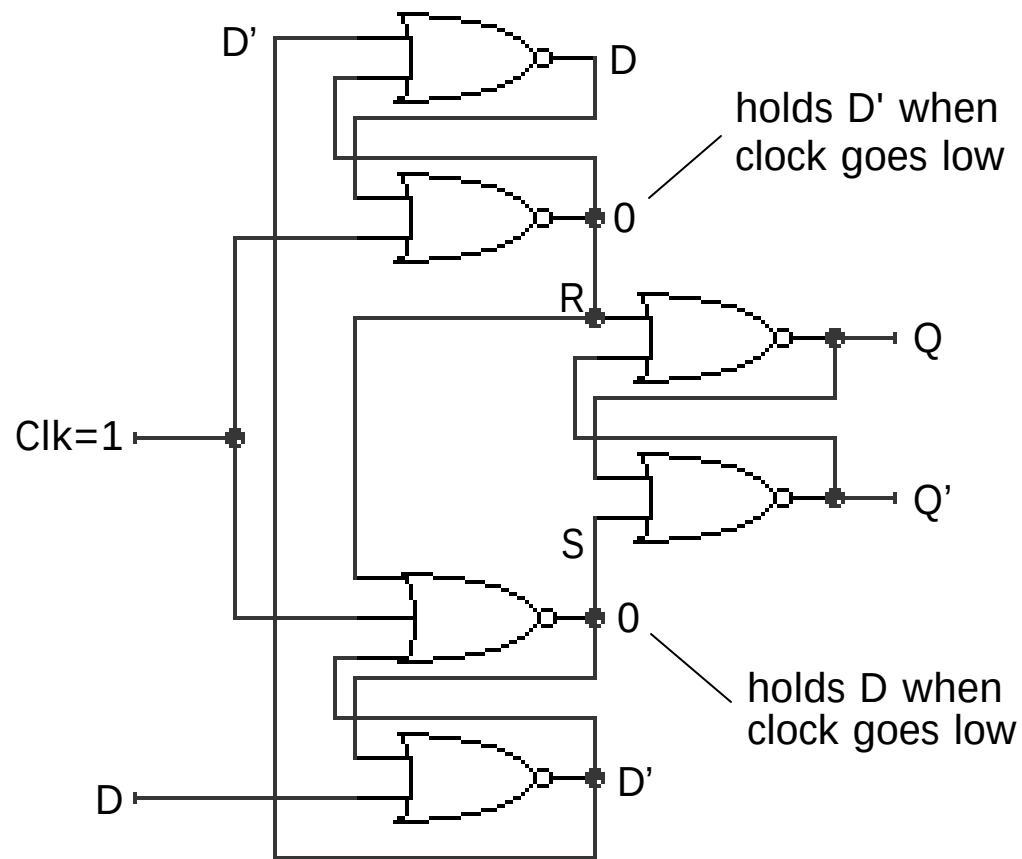
- Master/slave based D flip-flop: behaves like a negative edge-triggered flip-flop



10 gates

Edge-triggered flip-flops

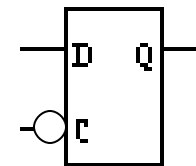
- More efficient solution: only 6 gates
 - sensitive to inputs only near edge of clock signal (not while high)



negative edge-triggered D
flip-flop (D-FF)

4-5 gate delays

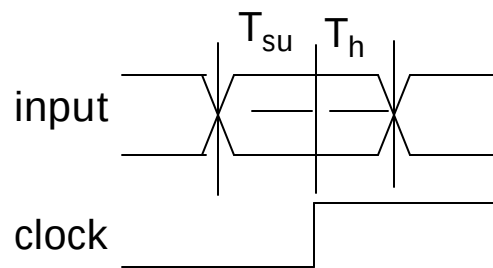
must respect setup and hold time
constraints to successfully
capture input



characteristic equation
 $Q(t+1) = D$

Timing methodologies

- Definition of terms
 - clock: periodic event, causes state of memory element to change
can be rising edge or falling edge or high level or low level
 - setup time: minimum time before the clocking event by which the input must be stable (T_{su})
 - hold time: minimum time after the clocking event until which the input must remain stable (T_h)



there is a timing "window" around the clocking event during which the input must remain stable and unchanged in order to be recognized

