

Homework #4

CSE 140L – Summer Session 2 – 2017

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PROBLEM 1: GENERAL QUESTIONS

Answer the following questions in a concise way. You are encouraged to look for the answer online. These questions will not be graded for the homework and you are not required to provide a report for them or submit anything, but they might be part of the final exam.

- 1) What data type would you use for memory cells in a CPU?
- 2) What are the differences between an ASIC and a FPGA?
- 3) Identify the problem with the code snippet below and rewrite it to fix the problem.

```
always @(posedge clk)
    x = 2;
always @(posedge clk)
    y = x;
```

- 4) Implement a latch using 2:1 Mux and write verilog code for the same.
- 5) The addition and subtraction in a CPU can be done using the same circuit? Yes/No. Explain with reason
- 6) Would this code simulate ? Explain your reasons and any potential problem this would lead to when implemented in hardware?

```
always @* begin
    case (sel)
        2'b00: y = a;
        2'b01: y = b;
        2'b01: y = c;
        2'b11: y = d;
    endcase
end
```

- 7) What is the period and frequency of the given clock generator?

```
always begin
    #5 clk = ~clk
end
```

- 8) What is the difference between a normal register and a shift register?
- 9) What is ALU? What is the function of it?
- 10) What is the size of a transistor in a modern CPU? What are the limitations in making transistors smaller ?

PROBLEM 2: TINY CPU PROJECT

Implement the Tiny CPU project by following the description in the document presented in class. The document can be accessed at the following link:

https://cseweb.ucsd.edu/classes/su16_2/cse140L-a/homeworks/CSE140L_Lab4.pdf

Checkoff list (to be completed with a tutor, a TA or the instructor before the end of last available office hour on Wednesday 08/30, which ends at 6pm).

NOTE: before starting the checkoff, a student **MUST** submit its zipped project via TED.

The submitted material **MUST** contain the source code.

The checkoff can only be attempted once, so make sure that your solution is working fine.

You can have your projects compiled in advance.

- 1) Submit the zipped project folder containing ALL of your source code on TED
- 2) Explain the functionality of the Tiny CPU
- 3) Review the Verilog code
- 4) Run testbench and explain the results to verify the functionality