

CSE 140L – Summer Session II – 2017

Instructor: Mohsen Imani

Homework #2

Checkoff Deadline: Wednesday, August 16

PROBLEM 1: GENERAL QUESTIONS

Answer the following questions in a concise way. You are encouraged to look for the answer online. These questions will not be graded for the homework and you are not required to provide a report for them or submit anything, but they might be part of the final exam.

- 1) What does the “Moore’s law” say?
- 2) What does VLSI mean?
- 3) What are the main design stages of integrated circuits?
- 4) What is a HDL? How is it different from a programming language like C?
- 5) What is Verilog?
- 6) What is an IDE? What is Quartus?
- 7) Explain what an FPGA is
- 8) What is the main reason for using FPGAs?
- 9) List the most important FPGA vendors
- 10) What are the main challenges involved with the design of integrated circuits?

PROBLEM 2: BASIC MODULES WITH QUARTUS, MODELSIM AND VERILOG

In this problem you are asked to implement basic modules with Verilog.

- Each component should be implemented as a Verilog module in a separate “.v” file.
- Also, each module should have its own testbench also implemented in a separate “.v” file, which you will run and explain during the checkoff.
- The inputs provided by the testbench should allow to easily demonstrate that your module behave as expected (similarly as the testbench presented in HW1).
- Coding style is very important: use comments to clearly identify the different modules and organize your code in a readable way

Components to implement:

- 1) 1-bit Half Adder
- 2) 1-bit Full Adder
- 3) 1-bit 4:1 MUX
- 4) 1-bit 4:2 Encoder
- 5) 1-bit 2:4 Decoder

Checkoff List (To be completed with a tutor, a TA or the instructor by Wednesday 08/16).

NOTE: Before starting the checkoff, you MUST submit your zipped project via TED. The submitted material MUST contain all the source code. The checkoff can only be attempted once, so make sure that your solution is working fine.

For two of the modules you implemented in Problem 2, selected by TA/tutor, you will be asked to

- 1) Explain the functionality
- 2) Review the Verilog code
- 3) Compile the code
- 4) Run testbench to verify functionality