

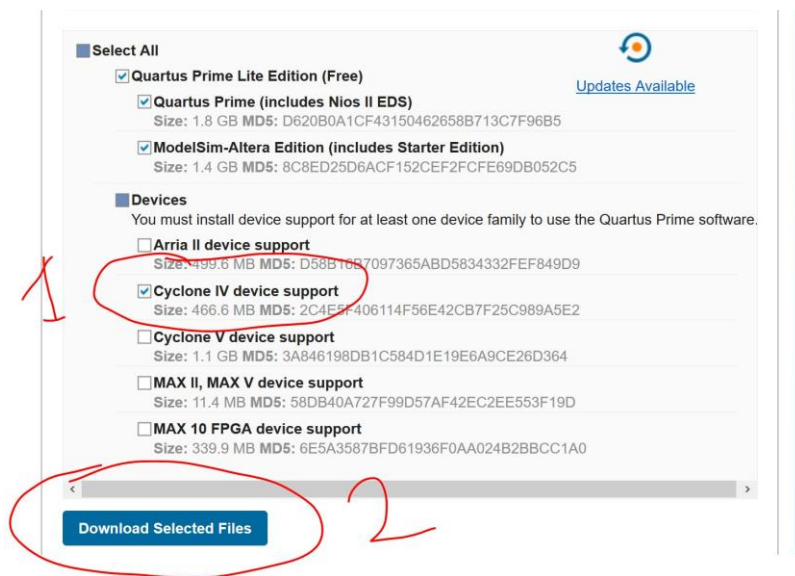
Homework #1 - DEMO  
CSE 140L – Summer Session 2 – 2017  
Instructor: Mohsen Imani

Demo prepared by: Muhsin Gurel

Follow this demo step by step to get familiar with the development and simulation environment. Also, answer the questions at the end to review the course policy. At the end, submit your zipped project in TED in “Homework 1” section under “Content”. You are not required to submit the answers to the questions at the end of this document. This homework will not be graded.

1) Go to this website : <http://dl.altera.com/?edition=lite>

2) Let's save some space and only select Cyclone IV device family and download. You can use the installer software or download directly.



3) Create an account if you don't have it already.

The screenshot shows the 'myAltera Account Help' and 'Terms and Conditions' links at the top. Below is a login form with fields for 'User Name' and 'Password', a 'Remember me' checkbox, and 'Log In' and 'Cancel' buttons. A link 'Forgot Your User Name or Password?' is also present. Below the login form is a section titled 'Don't have an account?' with a radio button selected for 'Create Your myAltera Account'. The text below says 'Your myAltera account allows you to file a service request, register for a class, download software, and more.' There is a field for 'Enter your email address' with the value 'mgurel@eng.ucsd.edu' entered. A note below the field says 'Note: If your email address already exists in our system we will retrieve the associated information.' The 'Create Account' button is circled in red.

4) You can enter the university information.

Email Address: mgurel@eng.ucsd.edu ([Edit Email](#))

\* First Name:

\* Last Name:

\* Company Name:

\* Address:

Address (Line 2):

\* City:

\* Country:

\* State:

\* Zip / Postal Code:

\* Telephone Number:   
Example: (408)544-7000x1234

\* Company Size:

\* My primary job function is:

\* My preferred distributor is:

\* Primary End Market:

5) I used the download manager.

Akamai DLM3 Download Manager: 3 files in total. ✕

The files you selected are being downloaded to the directory you chose. You can pause and resume the download at any time. If the download manager does not download any of the files, you can manually download the files with the direct links in the list below.

[Show direct links](#)

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**Download In Progress. ( 1 of 3 files )**

Total Download Size = **3.6GB**      Download Speed = **6.52MBps**  
Remaining Size = **3.14GB**      Estimated Time Remaining = **8 minutes**  
Download Location = **C:/Users/Muhsin/Downloads**

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**Downloading bundle**

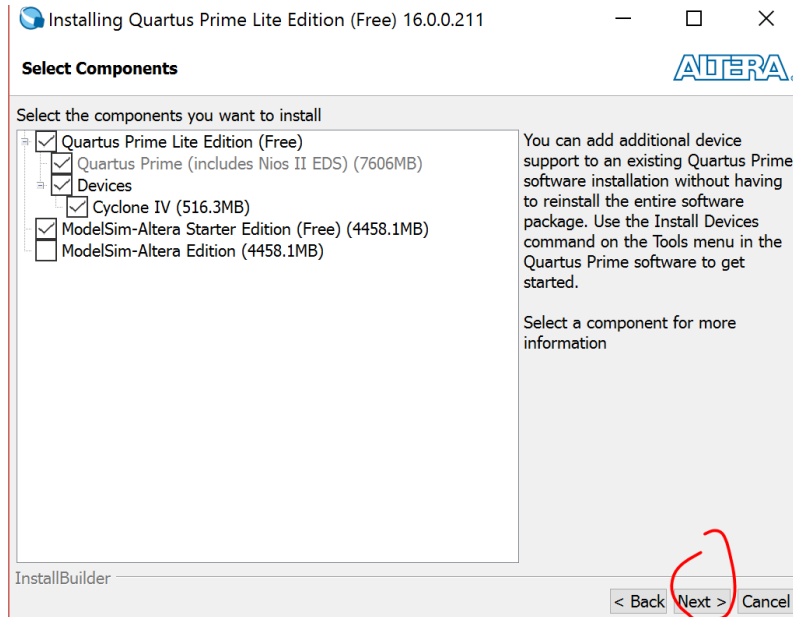
Total Progress 8.55%

QuartusLiteSetup-16.0.0.211-windows.exe (1 of 3): 25.64%

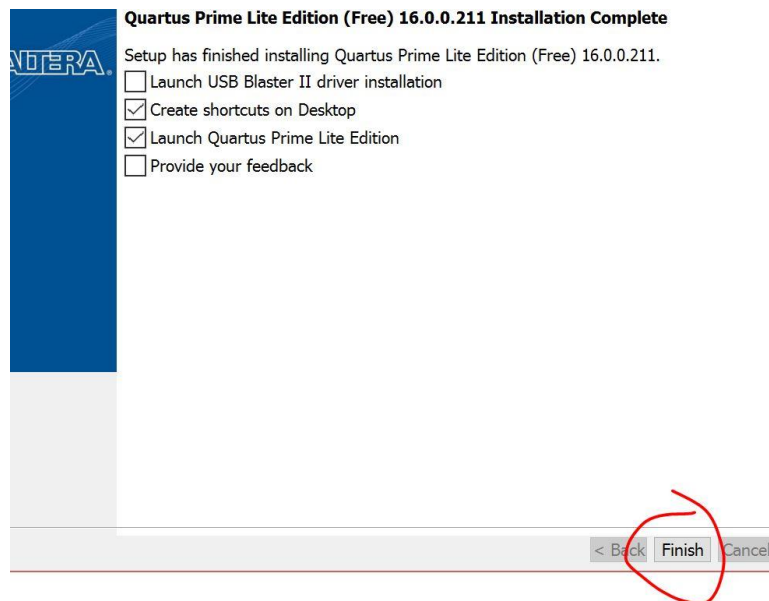
6) Locate the setup file in the directory where you downloaded them, start the installation.

|                                                                                                                                                                 |                   |             |              |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------|--------------|
| <input checked="" type="checkbox"/>  QuartusLiteSetup-16.0.0.211-windows.exe | 7/30/2016 4:13 PM | Application | 1,875,223 KB |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------|--------------|

7) Continue on the installation.

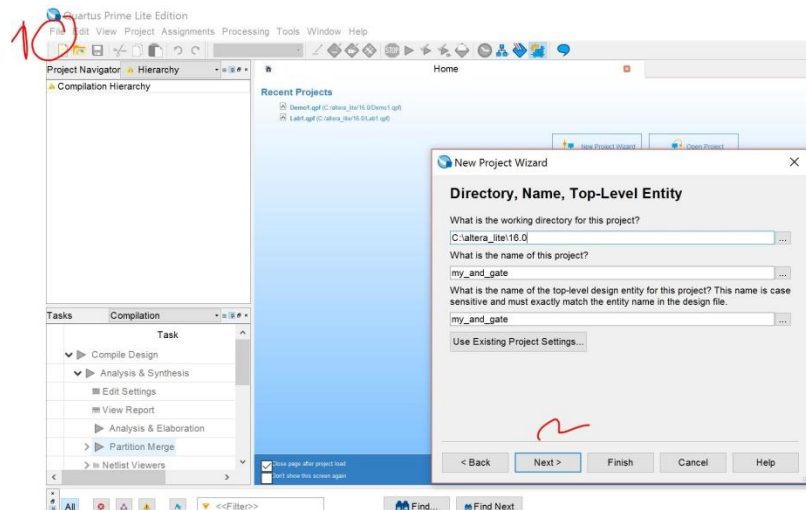


8) After finishing the installation you can launch the software.

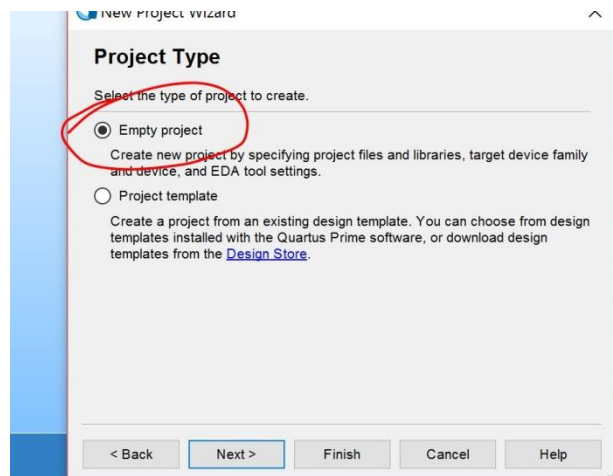


9) Now open the software (Quartus) if it is not already opened.

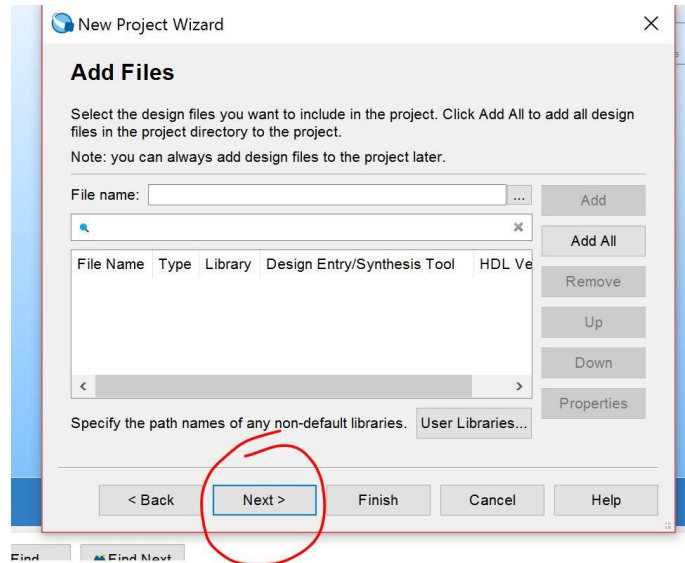
10) Let's create a new project. Click on File / New Project Wizard. Name your project and select or create a project folder. Also, name your top module. In this example they both are the same.



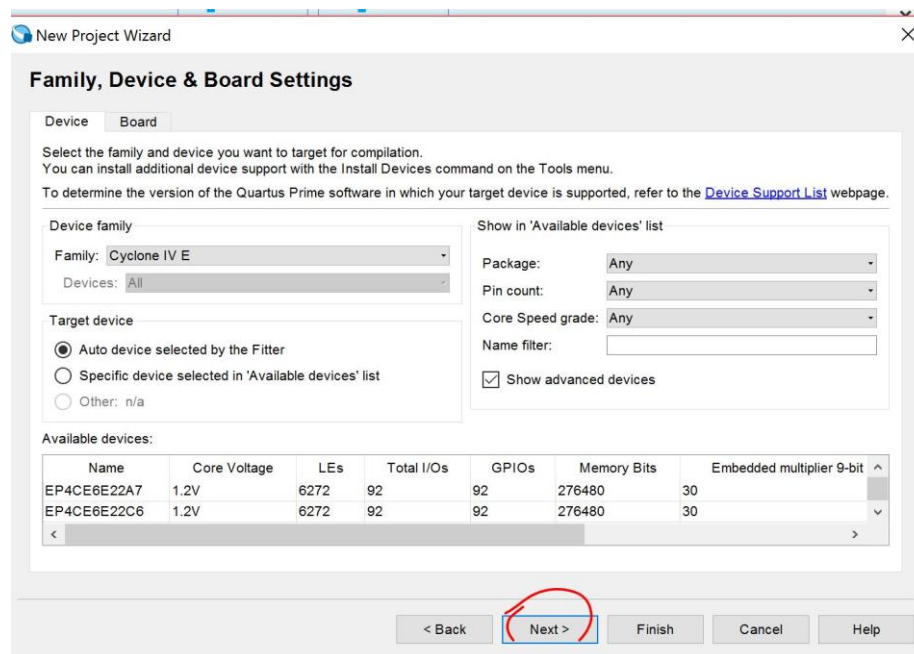
11) Select an empty project.



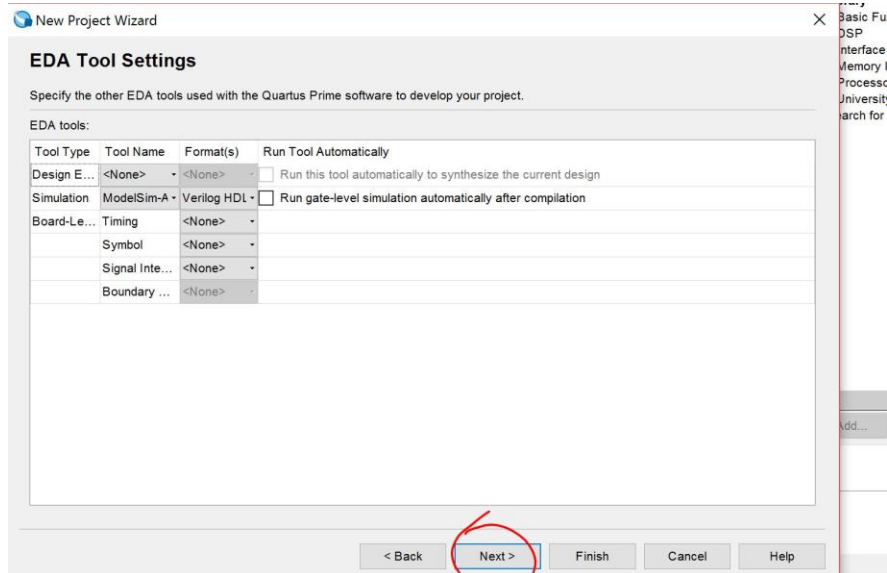
12)



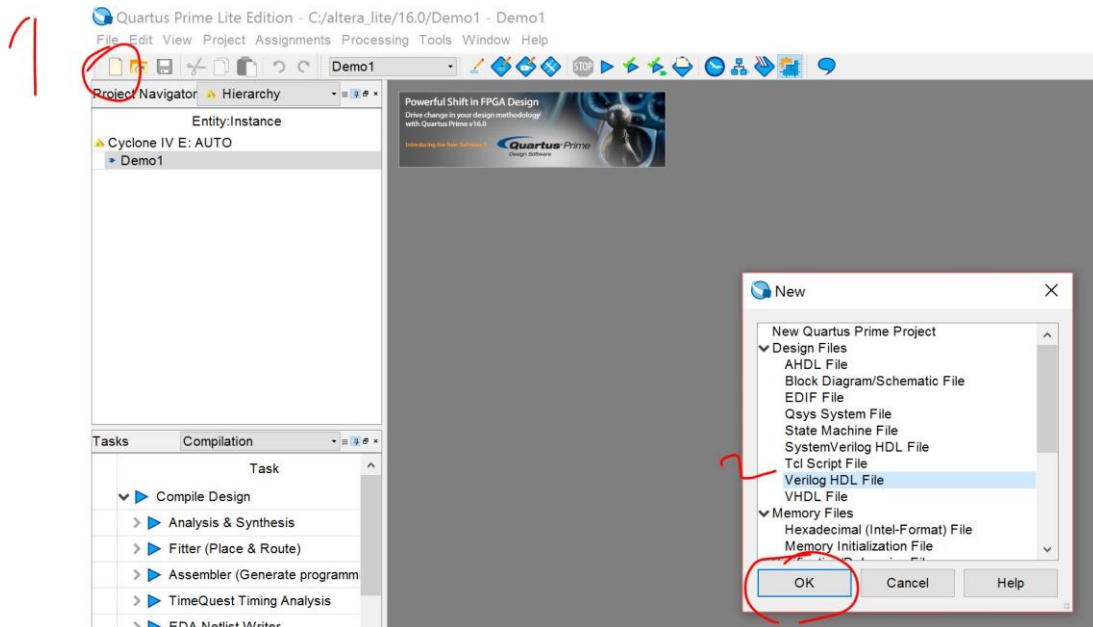
13) Here we can select an FPGA board, but since we will only use simulation just select the default one.



14) Under “simulation”, select Verilog HDL.

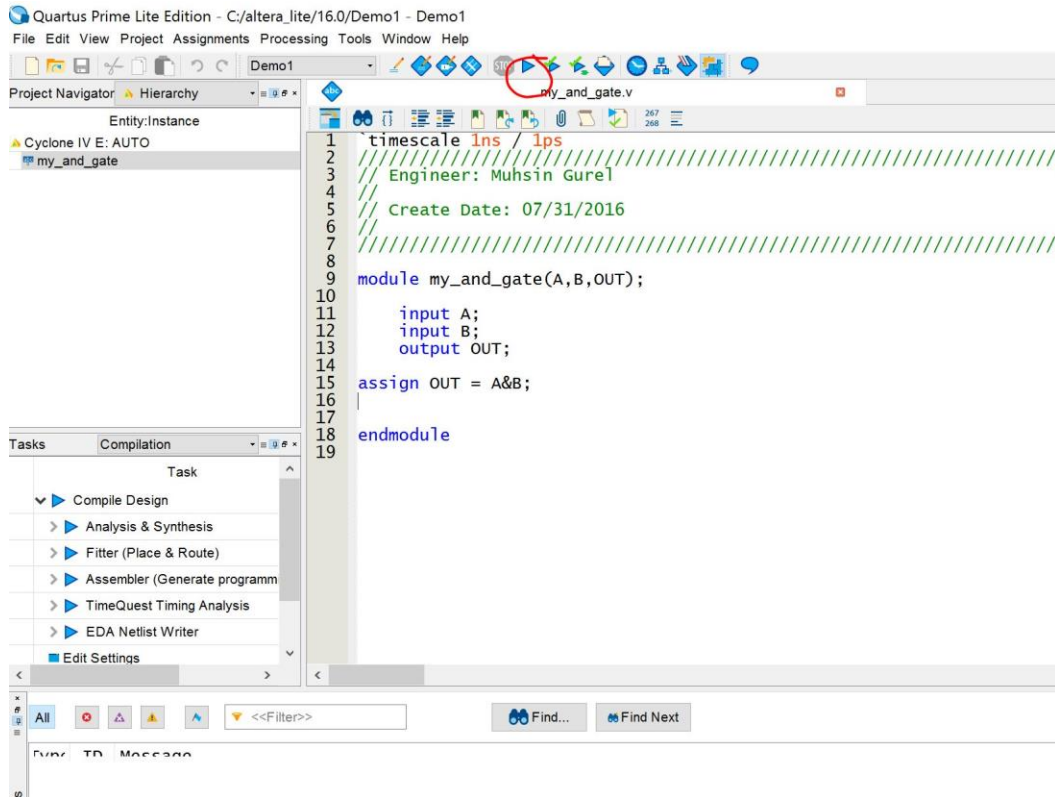


15) Now your project is created, let's write our first Verilog code. Click on the Add button and add a new Verilog file.



16) Let's design an AND gate. Below you can see the code for AND gate. We first define our module, by giving a name on it and defining its ports. In this example A,B,OUT is the name of the ports. Now let's define these Ports as Inputs or Outputs.

Finally, we can define the function in this module. Since it is an AND gate the equation should be like this. Also, don't forget to endmodule keyword. After writing this let's compile our design. If it is successfully compiled that means this Verilog could also be implemented on the FPGA .



17) Now let's write a testbench for our design. This testbench will behave as a “wrapper” for our AND gate and send test inputs to our module. For this, add a new Verilog file like you did in step 15, and name it as "test\_my\_and\_gate"

```
timescale 1ns / 1ps
module test_my_and_gate;

    // Inputs
    reg A;
    reg B;

    // Outputs
    wire OUT;

    // Instantiate the Unit Under Test (UUT)
    my_and_gate uut (
        .A(A),
        .B(B),
        .OUT(OUT)
    );

    initial begin
        // Initialize Inputs
        A = 0;
        B = 0;

        // Wait 100 ns for global reset to finish
        #100;
        A = 0;
        B = 1;

        // Wait 100 ns for global reset to finish
        #100;
        A = 1;
        B = 0;

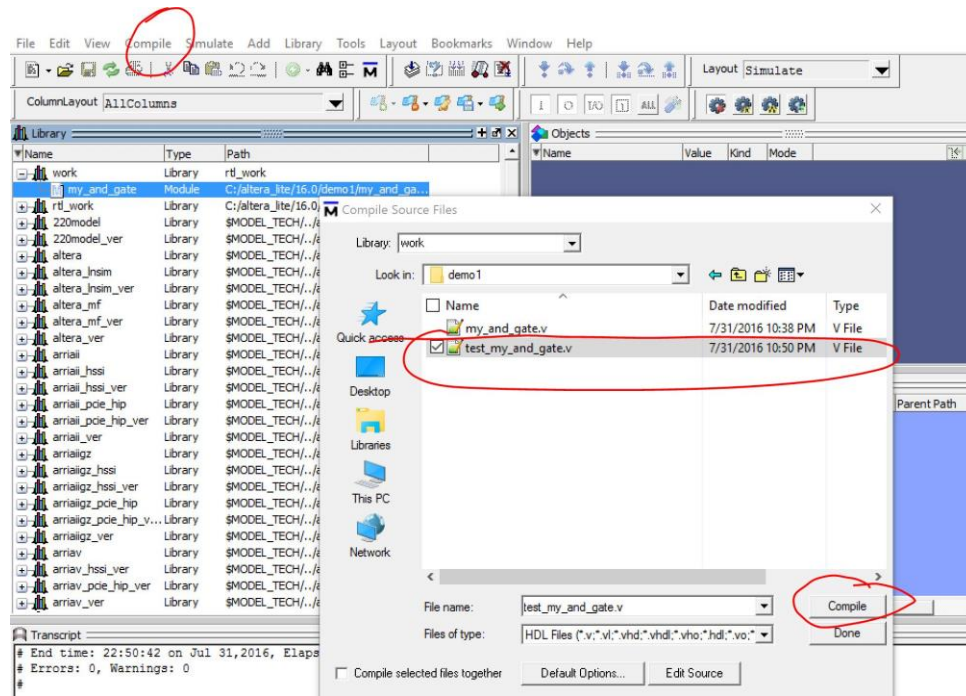
        // Wait 100 ns for global reset to finish
        #100;
        A = 1;
        B = 1;

    end
endmodule
```



18) After saving and compiling the test bench click on : Tools \ Run Simulation \ RTL Simulation. This will open the simulation environment.

19) Now we switched to the simulation software (ModelSim). Click on Compile and add your testbench.



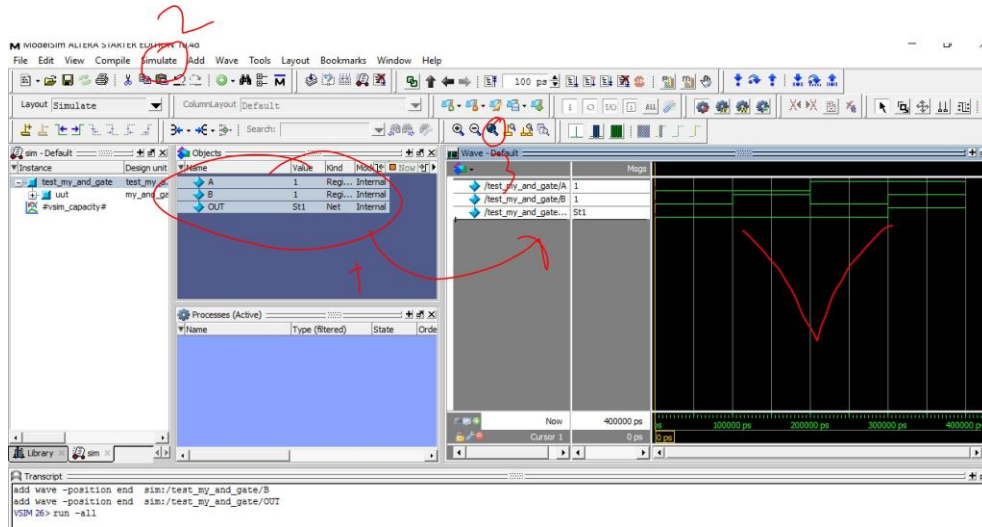
20) Double click on the testbench

| Name              | Type    | Path                                     |
|-------------------|---------|------------------------------------------|
| work              | Library | rtl_work                                 |
| my_and_gate       | Module  | C:/altera_lite/16.0/demo1/my_and_ga...   |
| test_my_and_ga... | Module  | C:/altera_lite/16.0/demo1/test_my_a...   |
| rtl_work          | Library | C:/altera_lite/16.0/simulation/models... |
| 220model          | Library | \$MODEL_TECH/./altera/vhdl/220model      |

21) Now if you cannot see the waveform window, go ahead and right click to open one. Drag and drop the ports from the Object window to waveform window.

Click on :Simulate\Run\Run-all

Lastly, click on the special zoom button.



Now we can see the waveforms for our testbench. As you can see the inputs are changing over time just as we described on the testbench. If you look at the Output you can see that it only goes high when both A and B is high.

#### QUESTIONS:

1. Have you installed Softwares required for this class on your PC or you are planning to use lab machines?
2. How will you submit the homework and how are you going to get grades?
3. Whats the late policy of homework submission of this class?
4. Is Pair Programming or Teams allowed, If yes what is the Maximum size of the group?

**Remember to SUBMIT the zipped project on TED!**