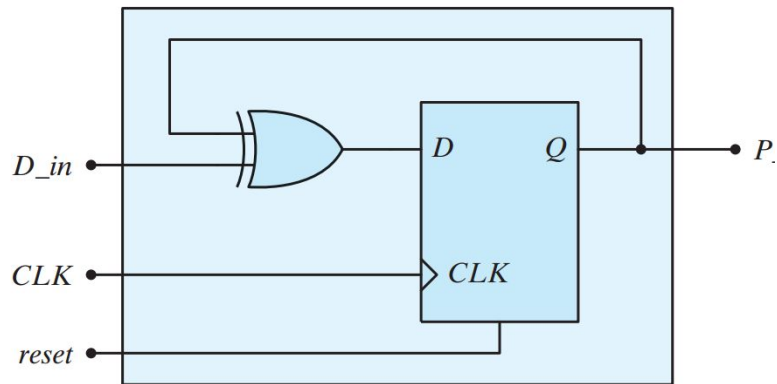
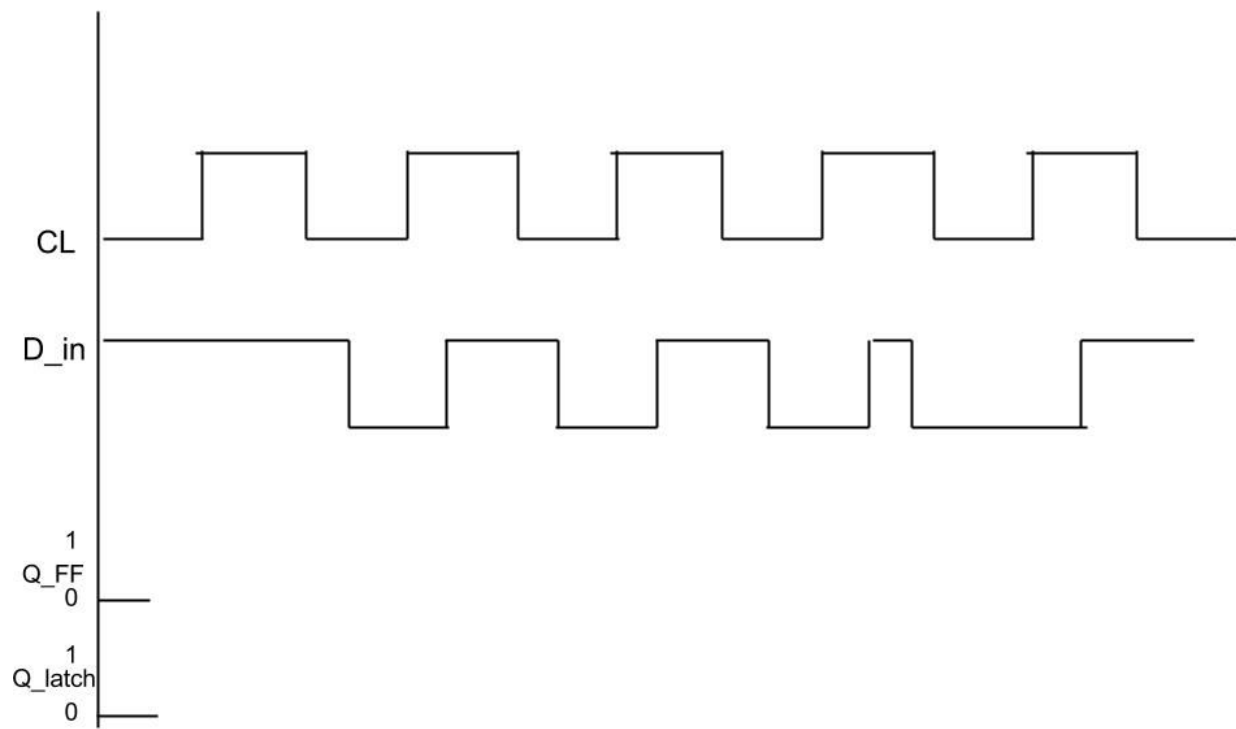


1) For the circuit shown below, do the following:



- write a logic equation for the output and the next state
- write an excitation table (current state, inputs, next state, outputs)
- draw the state diagram
- draw the waveform for output P given the clock and D_{in} signal in figure below. Assume zero delay through all gates and D-FF, and reset signal not enabled. Assume initial state of D-FF to be zero.
- draw the waveform for output P for the same signals shown in part d., but now assuming it is a D-latch instead of D-FF. Assume zero delay through all gates and D-FF, and reset signal not enabled. Assume initial state of the latch to be zero.

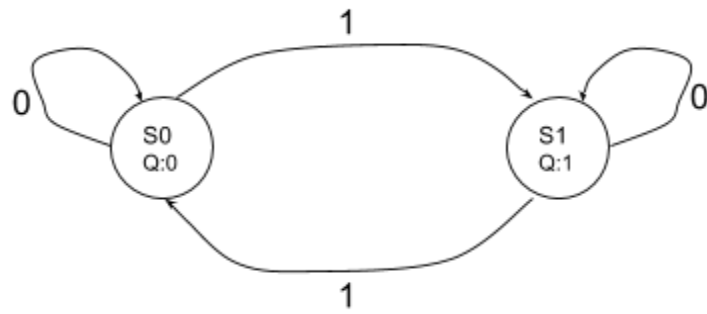


(a) $Q_{t+1} = D_{in} \oplus Q_t$;

$P = Q$

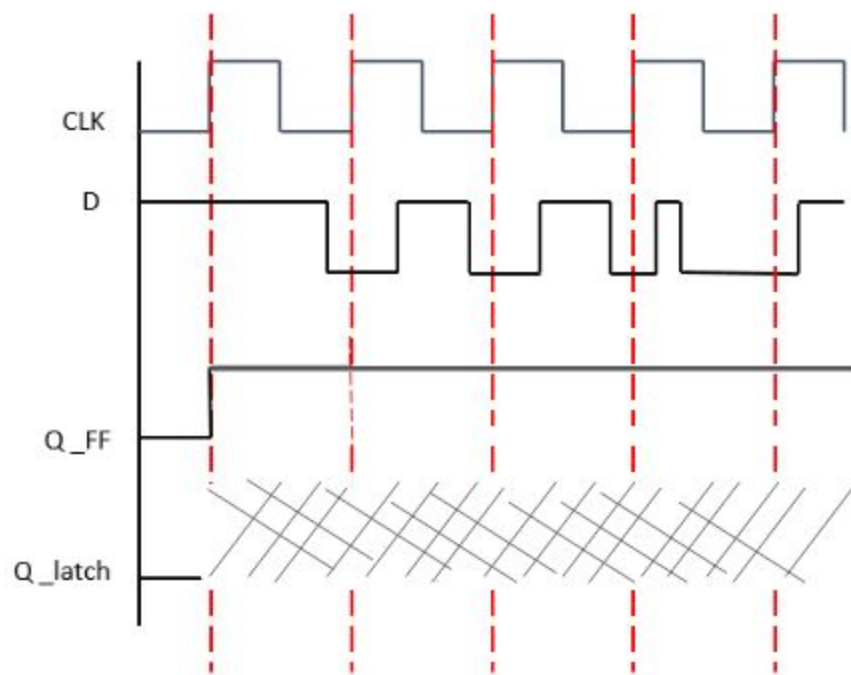
(b)

Q	D_in	Q _{next}
0	0	0
0	1	1
1	0	1
1	1	0



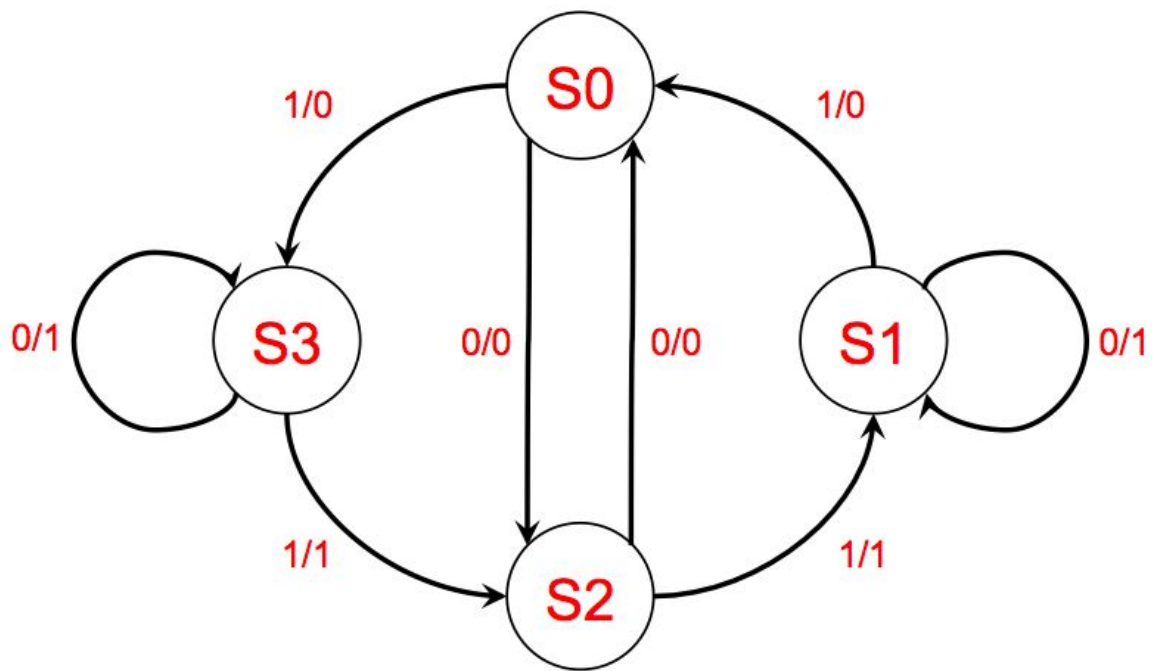
(c)

(d & e)



2)

- a) Mealy
- b)



$Q_1(t)$	$Q_0(t)$	$x(t)$	$Q_1(t+1)$	$Q_0(t+1)$	$D_1(t)$	$D_0(t)$	$y(t)$
0	0	0	1	0	1	0	0
0	0	1	1	1	1	1	0
0	1	0	0	1	0	1	1
0	1	1	0	0	0	0	0
1	0	0	0	0	0	0	0
1	0	1	0	1	0	1	1
1	1	0	1	1	1	1	1
1	1	1	1	0	1	0	1

s0	11	s0
s1	00	s1
s1	01	s1
s1	10	s2
s1	11	s1
s2	00	s0
s2	01	s0
s2	10	s0
s2	11	s0

Q1(t)Q0(t)	xy	D1(t) D0(t)
00	00	00
00	01	01
00	10	00
00	11	00
01	00	01
01	01	01
01	10	10
01	11	01
10	00	00
10	01	00
10	10	00
10	11	00
11	00	xx
11	01	xx
11	10	xx

11	11	xx
----	----	----

$$D1 = xy'Q0(t)$$

Q1(t)Q0(t)\xy	00	01	11	10
00	0	0	0	0
01	0	0	0	1
11	x	x	x	x
10	0	0	0	0

$$D0 = x'yQ1(t) + x'Q0(t) + y Q0(t)$$

Q1(t)Q0(t)\xy	00	01	11	10
00	0	1	0	0
01	1	1	1	0
11	x	x	x	x
10	0	0	0	0

4)

a. truth table:

INPUTS:

OUTPUTS:

Y	Z	Q1(t)	Q2(t)	Q1(t+1)	Q2(t+1)	out_1(t)	out_2(t)
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	1	1	1
0	1	0	0	1	0	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	1	1	1	1
1	0	0	0	1	0	0	0

1	0	0	1	0	1	0	1
1	0	1	0	0	1	1	0
1	0	1	1	1	1	1	1
1	1	0	0	0	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	0
1	1	1	1	0	1	1	1

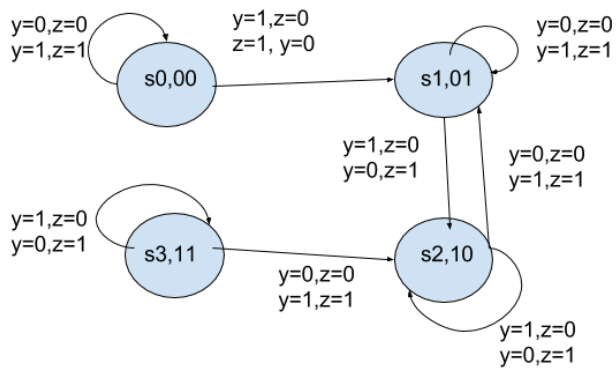
state table:

S0=00, S1=01, S2=10, S3=11

Y	Z	current state	next state	out_1	out_2
0	0	s0	s0	0	0
0	0	s1	s1	0	1
0	0	s2	s1	1	0
0	0	s3	s2	1	1
0	1	s0	s1	0	0
0	1	s1	s2	0	1
0	1	s2	s2	0	1
0	1	s3	s3	1	1
1	0	s0	s1	0	0
1	0	s1	s2	0	1

1	0	s2	s2	0	1
1	0	s3	s3	1	1
1	1	s0	s0	0	0
1	1	s1	s1	0	1
1	1	s2	s1	1	0
1	1	s3	s2	1	1

b) state diagram



** If students have used Q1Q2 ordering, the states 01 and 10 in the state diagram will be switched.

c) The FSM adds the previous output to the input/invert of the input at each cycle.

d) it's a Moore machine because the output depends only on the state

5)

a)

$$t_{pcq} + t_{pd(MAX)} + t_{setup} \leq T_c$$

$t_{pd(MAX)}$ is from the path (NOT-NOR-XOR-AND).

$$t_{pd(MAX)} = 10ps + 20ps + 40ps + 25ps = 95ps.$$

$$t_{pcq} + t_{pd(MAX)} + t_{setup} = 45ps + 95ps + 70ps = 210ps \leq T_c$$

$$\text{frequency} \leq 1s / 210ps \approx 4.762GHz$$

Thus, the maximum operating frequency is about 4.762 GHz (or 1000/210 GHz).

b)

$$t_{ccq} + t_{cd(MIN)} \geq \text{Clock}_{skew} + t_{hold}$$

$t_{cd(MIN)}$ is from the path (AND).

$$t_{cd(MIN)} = 20\text{ps}.$$

$$40\text{ps} + 20\text{ps} \geq \text{Clock}_{skew} + 30\text{ps}$$

$$\text{Clock}_{skew} \leq 30\text{ps}$$

This circuit can tolerate 30ps clock skew before a hold time violation.

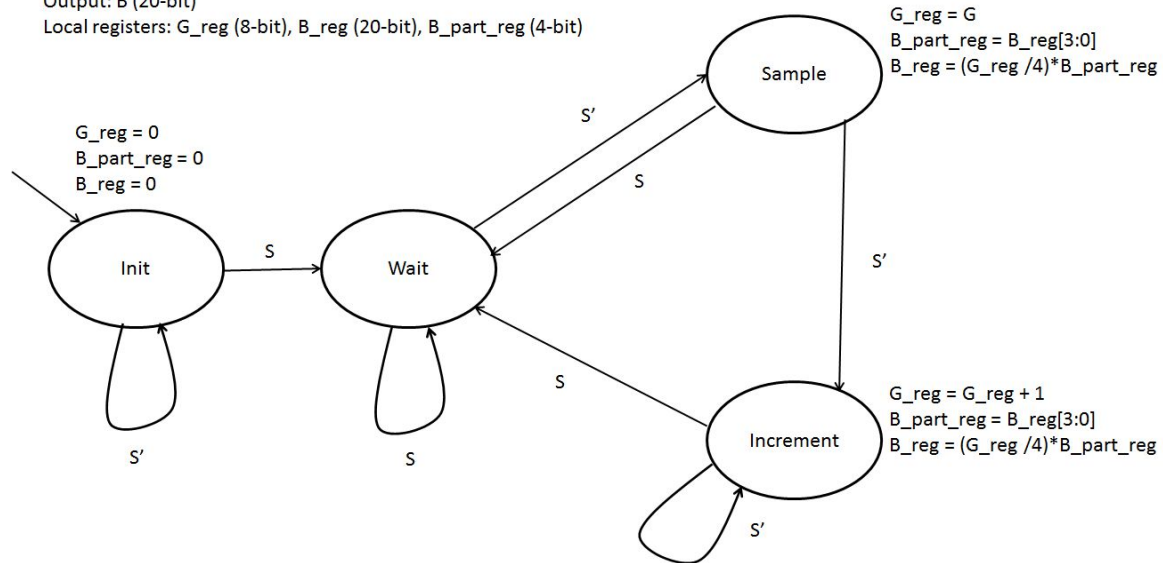
6)

a)

Input: S (1-bit), G (16-bit)

Output: B (20-bit)

Local registers: G_reg (8-bit), B_reg (20-bit), B_part_reg (4-bit)



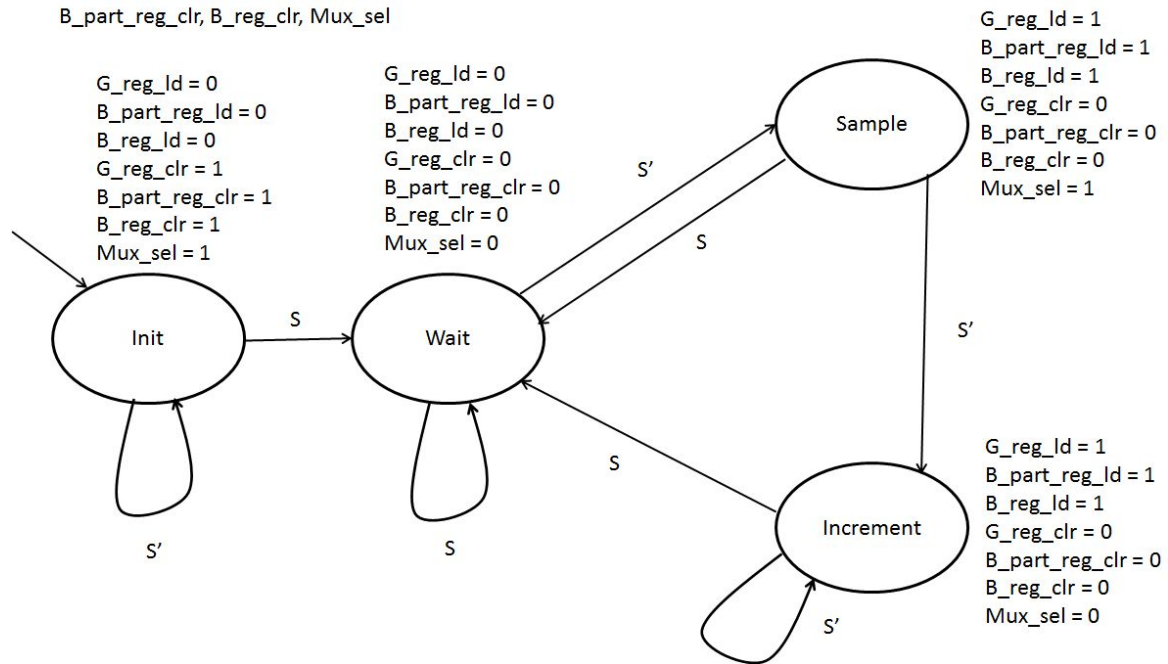
b)

d)

Input: S

Output: G_reg_ld, B_part_reg_ld, B_reg_ld, G_reg_clr

B_part_reg_clr, B_reg_clr, Mux_sel



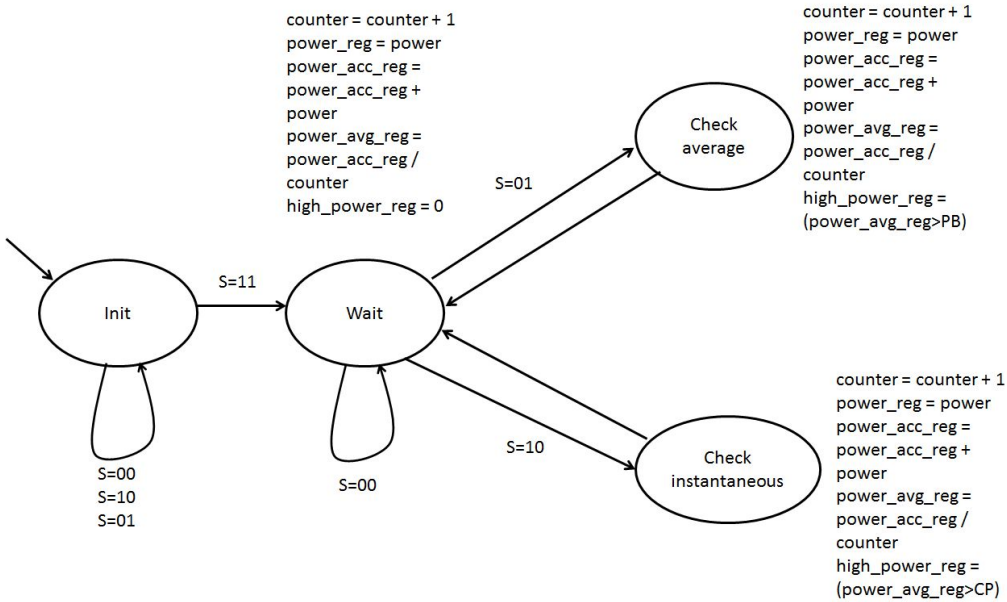
7)

a)

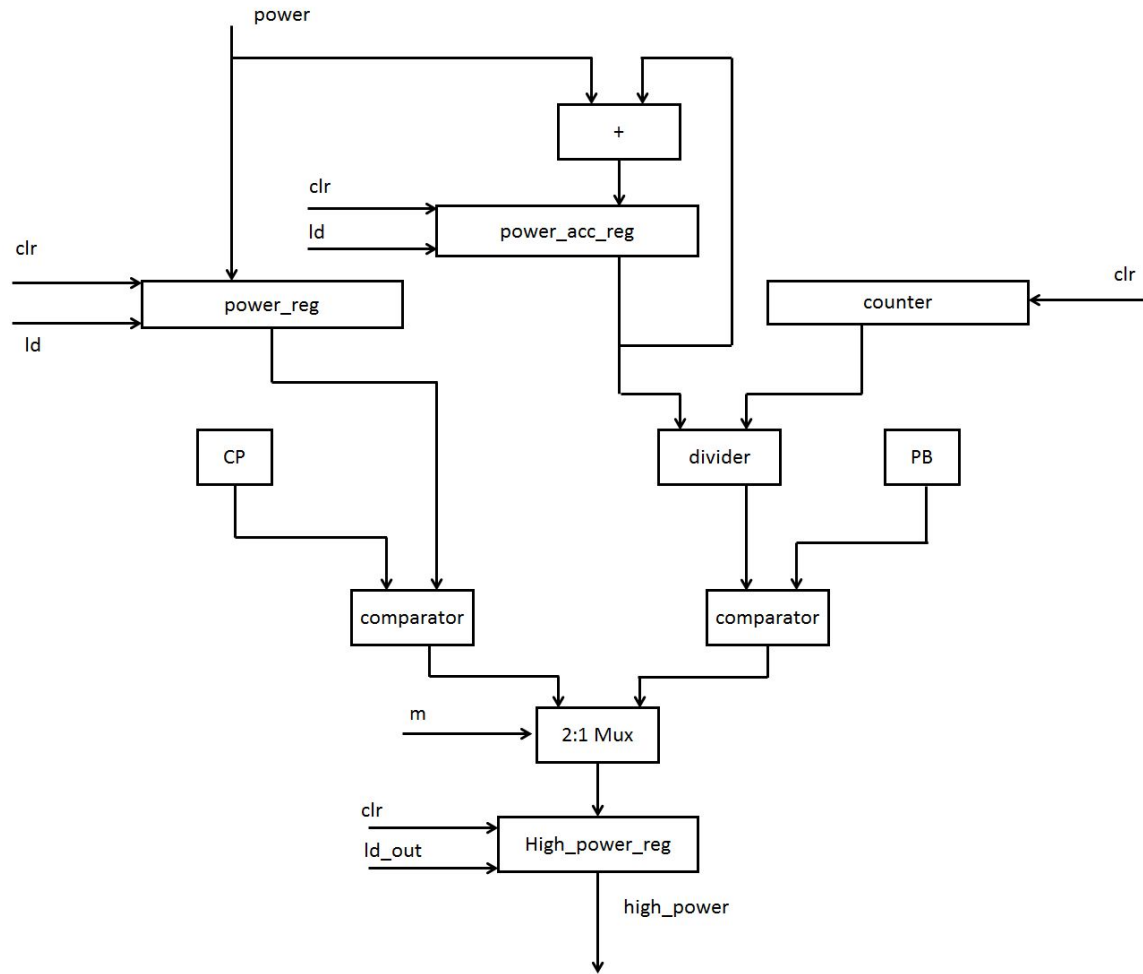
Input: S (2-bit), power (8-bit)

Output: high_power (1-bit)

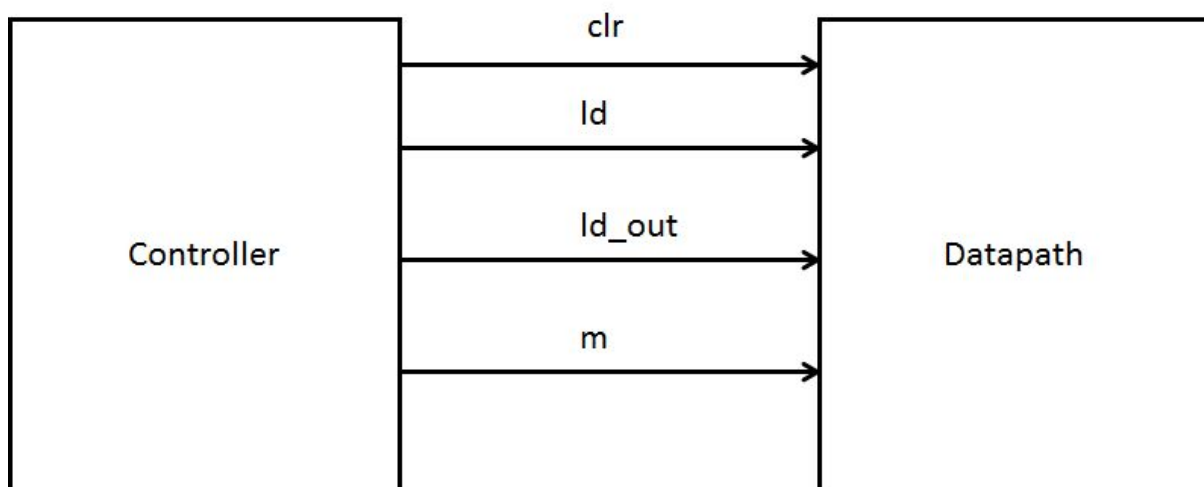
Internal registers: counter, power_reg, power_acc_reg, power_avg_reg, high_power_reg, CP, PB



b)



c)



d)

Input: S (2-bit)
Output: Id, Id_out, clr

