

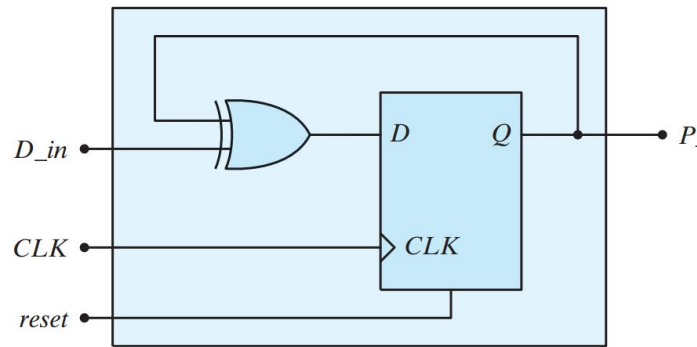
Homework #4

CSE 140 – Summer Session 2 – 2016

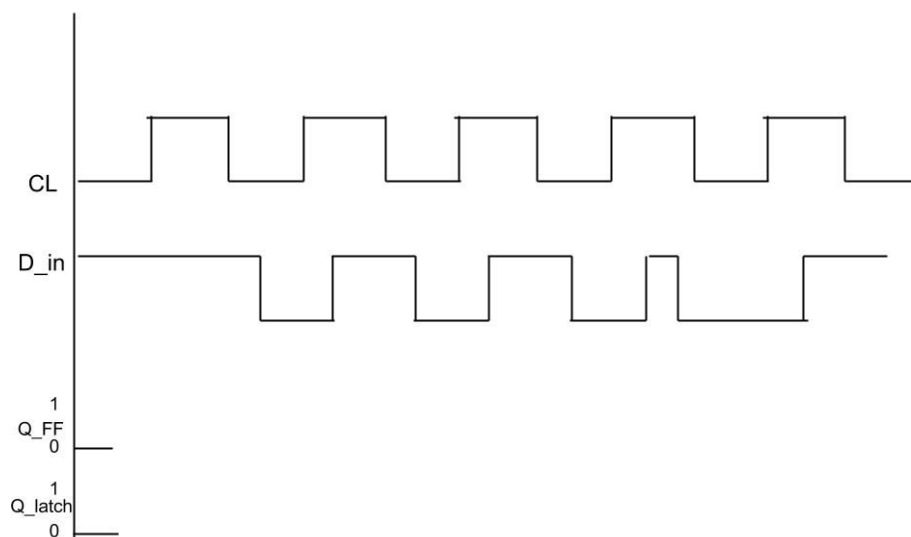
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Only a subset of questions will be graded

1) For the circuit shown below, do the following:



- Write a logic equation for the output “P” and for the next state
- Write the excitation table (current state, inputs, next state)
- Draw the state diagram
- Draw the waveform for output P given the clock and D_{in} signal in figure below. Assume zero delay through all gates and D-FF, and reset signal not enabled. Assume initial state of D-FF to be zero.
- Draw the waveform for output P for the same signals shown in part d., but now assuming it is a D-latch instead of D-FF. Assume zero delay through all gates and D-FF, and reset signal not enabled. Assume initial state of the latch to be zero.



2) Design the following Finite State Machine (FSM).

A state machine has one input $x(t)$, one output $y(t)$, and two-bit state ($Q_1(t)$, $Q_0(t)$). Its behavior over time is described by the following state equations.

$$Q_1(t+1) = Q_0(t)Q_1(t) + Q_0'(t)Q_1'(t)$$

$$Q_0(t+1) = x'(t)Q_0(t) + x(t)Q_0'(t)$$

$$y(t) = x(t)Q_1(t) + x'(t)Q_0(t)$$

- Do the above state equations describe a Moore machine or Mealy machine?
- Draw the state diagram using the following state assignments:
 $S_0 = 00$ (Q_1Q_0), $S_1 = 01$ (Q_1Q_0), $S_2 = 10$ (Q_1Q_0), $S_3 = 11$ (Q_1Q_0).
- We want to implement this FSM by using two D flip-flops and AND, OR, NOT gates. Fill out the state table, excitation table and draw the schematic of your solution

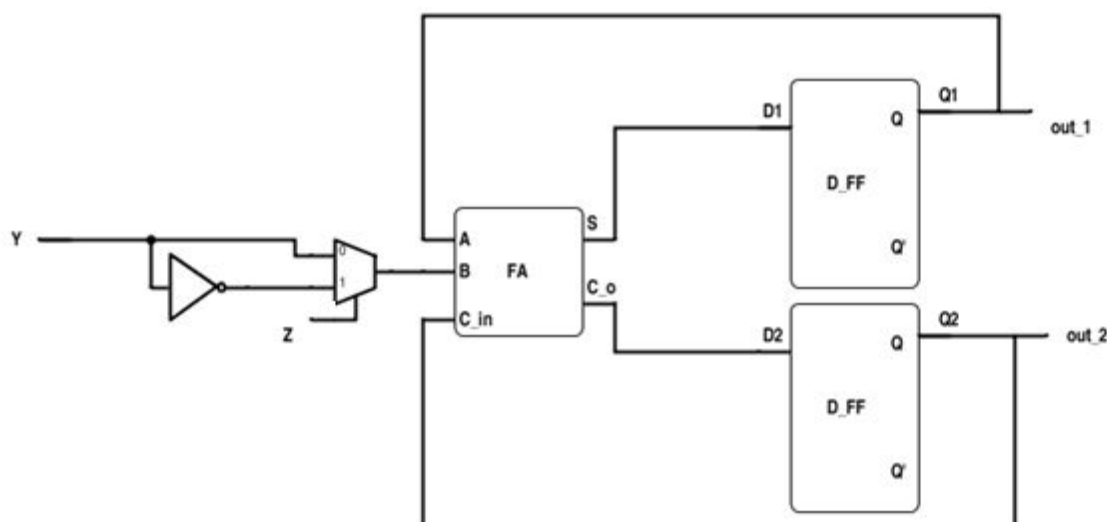
3) A Mealy FSM has a 2-bit input (X_1, X_0) and a 1-bit output Y .

The machine is initially in a state S_0 , until the input is 01. This takes the machine to a state S_1 . From S_1 , when the input switches to 10, the output switches to 1, then the machine goes to state S_2 for exactly one cycle. After that, the machine goes back to S_0 and on this transition the output is switched to 0. All other input combinations do not trigger state transitions. In all other cases, the output is 0.

- Draw the state diagram for this machine
- Draw the state table with assignments and the excitation table
- Derive the characteristic equations for the new state and for the output
- Draw the circuit for your Mealy FSM

4) The circuit below has two 1 bit inputs (Y , Z) and two outputs (out_1 , out_2). The FA block is a Full Adder, while D_FF indicates a D Flip-Flop. For this circuit:

- Write the state table.
- Draw the state diagram.
- Describe the functionality of this FSM.
- Is this a Mealy machine or a Moore machine?



5) For the following circuit, the timing characteristics are summarized below:

Flip-flop:

clock-to-Q maximum delay (propagation delay) $t_{pcq} = 45$ ps,

clock-to-Q minimum delay (contamination delay) $t_{ccq} = 40$ ps,

Setup time $t_{setup} = 70$ ps,

Hold time $t_{hold} = 30$ ps.

Logic gates:

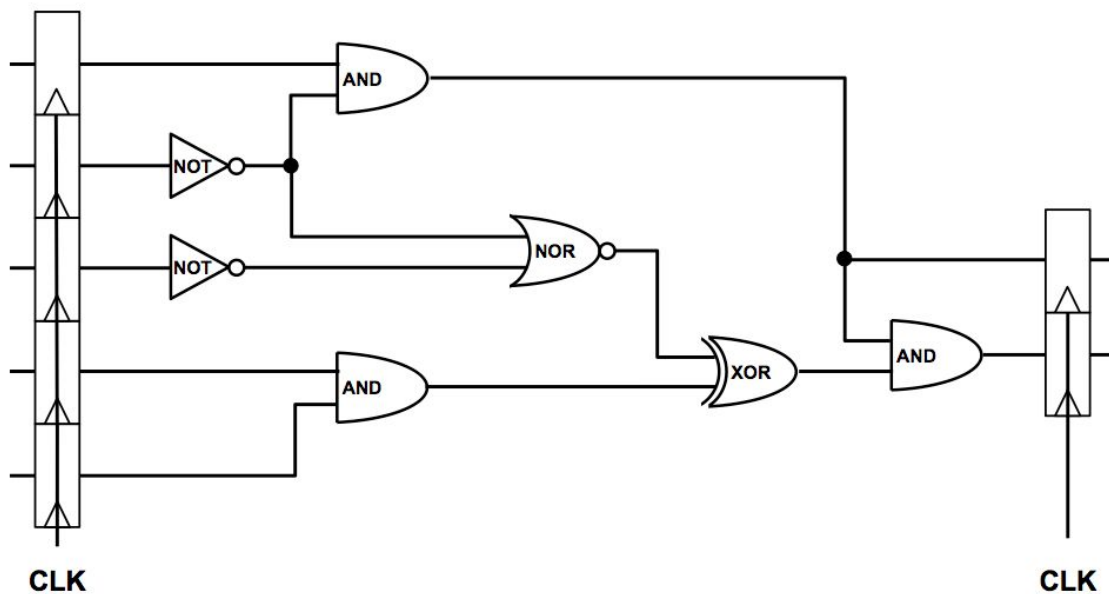
AND propagation delay $t_{ANDpd} = 25$ ps, AND contamination delay $t_{ANDcd} = 20$ ps,

NOT propagation delay $t_{NOTpd} = 10$ ps, and NOT contamination delay $t_{NOTcd} = 10$ ps,

NOR propagation delay $t_{NORpd} = 20$ ps, and NOR contamination delay $t_{NORcd} = 20$ ps,

XOR propagation delay $t_{XORpd} = 40$ ps, and XOR contamination delay $t_{XORcd} = 30$ ps.

- Assume there is no clock skew. What is the maximum operating clock frequency?
- How much clock skew can this circuit tolerate before the circuit experiences a hold time violation?



- 6) Use the RTL design process to design a system that outputs a multi-bit data number based on the following.

The system has a 16-bit unsigned data input G and an unsigned output B. The data input is sampled and stored in a local register when a single bit input S changes from 1 to 0.

Right after sampling a new value, the system increases the stored value by 1 at each clock cycle as long as S is zero.

If S is switched back to 1, the system waits.

At each clock cycle, the output of the system is:

$$(\text{stored_input} / 4) * \text{previous_output}[3:0]$$

Where `previous_output[3:0]` are the 4 least significant bits of the previous output.

Choose and report the internal bit widths that prevent overflow and present the following in your solution:

- Diagram of the HLSM. Label inputs and outputs and use comments to clarify your reasoning. Write clearly the size of all internal registers. Choose the size in order to avoid overflow
- Create a datapath and clearly label the control signals of your components.
- Connect the datapath to a controller and report the values of control signals.
- Derive the controller's FSM diagram

Present your solution in a clear format. Unclear and poorly written solutions will NOT get full points.

- 7) CPU power monitoring system (**Not mandatory, it will not be graded**):

Use the RTL design process to design a system that monitors the power consumption of a CPU.

A 2-bit input S controls the power monitoring strategy. A power sensor provides the input in milliWatts as a 8-bit binary string.

Also, the system has an internal counter.

The system has an input clock with the frequency of 1 kHz.

The system samples a new value from the power sensor and increases the internal counters by 1 every 1ms.

The system has two internal thresholds. The first is referred to as "Power Budget" (PB) equal to 100mW/s. The second is referred to as "Critical Power" (CP), equal to 200mW.

The system has also one 1-bit output: `high_power`.

The behavior of the system is described as follows:

The system is initially in a state where all internal registers have value 0

When the input S switches to 11, the system activates the counter and samples input power. The high_power output is 0.

From this, if S is 01, then for one cycle the system checks whether the average power consumption is above the threshold PB. If yes, it switches high_power to 1 for one cycle. While doing this, the system should keep on sampling power.

if S is 10, then for one cycle the system checks whether the current power consumption is above the threshold CP. If yes, it switches high_power to 1 for one cycle. While doing this, the system should keep on sampling power.

Hint: think carefully about how you calculate an average over time.

Present the following in your solution:

- a. Diagram of the HLSM. Label inputs and outputs and use comments to clarify your reasoning. Write clearly the size of all internal registers. Choose the size in order to avoid overflow. You have internal registers for PB and CP, which minimum size should they have?
- b. Create a datapath and clearly label the control signals of your components.
- c. Connect the datapath to a controller
- d. Derive the controller's FSM diagram