

Assignment 4

1. Build Pipelining CPU building blocks (individual modules) in Verilog (modules)
 - ✓ a. Debug Verilog ✓ Tests
 - ✓ b. Simulation ✓ ↗
 - ✓ c. Synthesis ✓
2. Demo to 141L TA. ✓
3. Highly suggested: Get start on assignment #5 : put together the pipelining CPU using port-mapping.
4. Due next Friday 6pm (9/4)

At a minimum, you will need these independently functioning pipelining CPU blocks, 20% each:

- (1) Fetch Unit (which includes PC logic and branch-handling)
- (2) Control Unit
- (3) Register file (and handling of one type of data hazard inside the register file)
- (4) ALU
- (5) Either a forwarding detection unit, or a hazard detection unit, or both, depending on your specific ISAs

You should focus on coming up with a few test cases that have good *coverage*. Having many, many test cases is not necessarily be a good thing.

Assignment 5

1. Put together the pipelining CPU
2. Finish your Pipelining CPU by Sunday 9pm (demo to TA)
 - a. Verilog
 - b. Simulation
 - c. Synthesis
3. Due Monday (9/7) 5pm

*grace
period
- grading only*

Hint:

Put together the pipelining CPU one stage at a time!!!
Ready for a long weekend!!!

Extra Lab Office hours this weekend:

Vasileios: Saturday 9/5 1-5pm + 6-9pm

Hung-wei: Sunday 9/6 1-5pm + 6-9pm

Ankur: Monday (9/7) 1-5pm

Grading Lab 5

- 25% Verilog of pipelining CPU put together
- 50% Simulation results
- 25% synthesis of entire CPU

Labor day (9/7) 5pm is the deadline. There will be a sign-up sheet for grading only on 9/7.

No lecture next Thursday

Next Thursday, no lecture for 141L. Study for your 141 Final Exam.