

Exercise # 01 : ROM analyzer

A ROM memory (1K x 16) stores 1024 data of 16 bits each, represented according to the “2’s complement” notation.

On a serial transmission line, 16-bits numbers are transmitted synchronously w.r.t. a clock signal clk, one bit per clock cycle, according to the following protocol:

- Numbers are transmitted LSB first
- Each new number has a 4 bit header : “1111”
- 6,000+ clock cycles occur between two consecutive transmitted numbers.

A system is to be designed such that, whenever a new number N is received via the input line, determines the overall number T of data D, stored in the ROM, are such that

$$|D| = N.$$

At the operation completion, T has to be visualized, on a proper set of 7-segment displays, till getting the next number N.

Exercise #02 : Histogram generator

A ROM memory (1K x 8) stores 1024 data of 8 bits each, represent the samples of an arithmetic function (they are stored in the “2’s complement” notation).

Design a system that, when the START signal is raised, stores into a RAM memory the histogram of the samples stored in the ROM.

At the end of the computation, the RAM stores the statistical frequency of occurrence of each sample; in particular:

- cell 0 will store the number of times the value -128 appears in the ROM
- cell 1 will store the number of times the value -127 appears in the ROM
- ...
- cell 255 will store the number of times the value +127 appears in the ROM

Exercise #03 : Peak values of a function

A RAM memory (1k x 8) stores 1024 samples of a function $f(x)$, represented on 8 bits in 2's complement notation. In particular each cell i of the memory stores the value of $f(x_i)$.

Design a system that, when the START signal is raised, is able to perform the following tasks:

- Compute the number of peak points of the function $f(x)$; the $x=0$ and $x=1023$ cannot be considered peak points.
- Compute the maximum of the function
- Visualize both data on a digital display.

Exercise # 04 : Gate remote-control

A gate remote controller is to be designed.

It must fulfill the following requirements:

- The open and close commands arrive through a *new_com* signal, positive edge triggered. When a new command arrives, the gate has to:
 - open, if it is closed
 - close, if it is open
 - invert the moving direction, if it is moving.
- During normal functioning, the gate must close after a user defined amount of time (from 0 to 5 min, with a precision of half a second).
- The gate opens inward.
- A light must blink while the gate is moving, and it must blink for a user defined amount of seconds before the movement (from 0 sec. to 10sec., with a precision of half a second).
- For security sake there are:
 - Two photocells, one inside the court (to detect objects that may hamper the complete opening of the doors) and an extern one on the gate jambs (to detect objects that may hamper the complete closure of the doors). If the inner photocell light is crossed during the opening or if one of the two is crossed during the closure, the gate must invert its moving direction.
 - Two strength sensors able to notice whether during the movement the gate encounters an obstacle out of the photocells' range: in this case the gate must invert its moving direction.

In case of reaction to an obstacle, if the gate ends in 'close' position, it stays so, while if it ends in 'open' position, it will retry to close after a user defined amount of time.

- The working clock rate is 10MHz.
- All signals coming from sensors are level triggered (active on high value) and must stay high at least 1ms to be recognized.

A position sensor, able to communicate if the gate is open, closed or in a middle position, is available. In case of strange situations (i.e. impossibility to close or to open at the same time) an acoustic alarm must be turned on, until it is possible to return to a normal condition.

The controller has the following interface signals:

System signals

- CLK – 10 MHz clock
- A_RES – asynchronous reset
- NEW_CMD – command signal
- BUS_LIGHT – used to access the time between light turning on and gate opening
- BUS_OPEN – used to access the time before closure

Sensors signals (level triggered)

- IS_OPEN – high if the gate is completely open
- IS_CLOSED – high if the gate is completely close
- If both previous signals are high the gate is in a middle position
- INT_CELL – high if the inner photocell is crossed
- EXT_CELL – high if the extern photocell is crossed
- STRNG_1 – high if the gate encounters an obstacle during the opening
- STRNG_2 – high if the gate encounters an obstacle during the closing

Control signals (level triggered)

- LIGH_ON – if it is high, the light is on
- SOUND_ON – if it is high, the alarm is on
- ENGINE_ON – if it is high, the engine is on
- OPEN / ~CLOSE – if it is high, the engine opens the gate, otherwise it closes it

Exercise # 05: TV remote-control

Design a tv remote controller.

The remote controller receives the following input signals :

- Change channel (P+ e P-)
- Change volume (V+ e V-)
- On/Off Switch: each pressing on the ON/OFF signal forces a change in the tv state (it switches the tv off if the tv was on, and vice versa)

The communication between remote controller and tv is implemented on a serial line; the possible commands sent by the remote to the tv are:

Command	Code
P+	001
P-	000
V+	011
V-	010
ON	101
OFF	100
ALIVE	111

When the serial line is inactive, it sends '0's.

It is required to define the protocol (with start and stop bits) to be used over the serial line to send and receive signals.

The V+ and V- signals can be sent continuously to the tv, and they are valid until the corresponding key is pressed; all the pther signals have to be sent only once, following the pressing of the corresponding key.

The remote controller has to send to the tv at least one command every second. If there are no commands to send, it has to transmit the ALIVE command.

Exercise # 06 : Signal regenerator

On a serial transmission line, data are transmitted according to a “2 out of 3” protocol:

- the transmitter encodes each data bit as 3 consecutive identical bits (e.g., ‘1’ -> ‘111’)
- the receiver analyses each group of 3 bits and decodes it:
 - as ‘0’ when at least two bits in the group are equal to ‘0’,
 - as ‘1’ otherwise.

A circuit is to be design to be connected to the transmission line to *regenerate* the received data: it receives data from an input lines, interprets them according to the protocol, and transmit them on an output line, according to the same protocol (e.g., when it receives ‘010’ it transmits ‘000’, when it receives ‘011’ it transmits ‘111’, when it receives ‘111’ it transmits ‘111’ and so on).

Exercise #07 : Badge access

A badge access control system is to be designed.

The system has to manage the access to 8 different gates. Each gate has:

- A magnetic badge reader, which is connected to the controller through a serial line. On the serial line, each data is transmitted using one start bit, 8 data bits, and 1 stop bit; the line is at logic '1' if nothing is transmitted.
- An automatic lock, which is open when the corresponding OPEN signal is 1. The lock is closed if OPEN=0.

When a badge is swiped in the reader, the reader sends to the control system, on the serial line, the ID (16 bits) stored in the badge. The controller decides if to grant or not the access to the gate browsing the content of a RAM memory. The memory stores the list of gates and times each ID has access to. The organization of the data into the RAM has to be defined.

If the access is granted, the opening of the lock is enabled for 10 seconds.

Discuss the dimension of the RAM memory, depending on the max number N_USERS of possible badges.

In a second RAM it is also requested to store the last 1024 accesses granted by the system.