

Section 1.1

Asynchronous Circuits

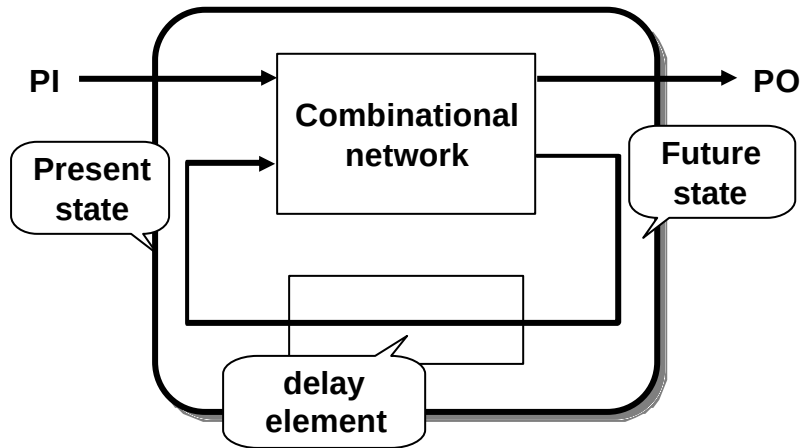
Introduction

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Outline

- Introduction**
- Functional modes**
- Asynchronous circuit model**

Asynchronous Circuits Model



Asynchronous vs Synchronous: state

In synchronous circuits (D FF)

- Each flip-flop can remember one bit
- Each flip-flop holds a state variable
- The present state is the flip-flop output(s)
- The next state is the the D input(s)

In asynchronous circuits

- Each feedback loop can latch one bit
- Each feedback loop holds a state variable
- The state is the value on the feedback lead
- The next state is ...

Pros

- **The world is asynchronous: the interfaces towards the world have to be asynchronous**
- **A global sync signal (clock) is not required and therefore there are no skew problems. The change of internal state occurs when there is a change in the input variable**
- **They can be faster, smaller, and dissipate less power than their synchronous versions.**

Cons

- **Difficult to design: critical races have to be avoided. For medium to big size circuits the only solutions would be automatic synthesis, but no efficient tool is available on the market.**
- **Almost impossible to test: the higher speed does not justify the higher testing costs**

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Functional modes

- **Two modes:**
 - **Fundamental mode**
 - **Input/Output mode**

Functional modes

- **Two modes:**

- **Fundamental mode**
- **Input/Output mode**

- Inputs change only when all the nodes of the network are stable
- Only one input changes at a time
- No further changes occur until all state variables have stabilized

Functional modes

- **Two modes:**

- **Fundamental mode**
- **Input/Output mode**

- Inputs do not change before that one of the outputs changed consequently to the previous input change

Caveat

- **Each mode requires a particular design methodology**
- **There is no guarantee that a circuit designed to work in one mode will behave correctly in the other mode**

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Speed-independent vs delay-insensitive

- **An asynchronous circuit is said to be speed-independent if, assuming 0-delay interconnects, it works correctly independently from the delay of its gates**
- **An asynchronous circuit is said to be delay-insensitive if it works correctly independently from the delays of its gates AND its interconnects**

Assumptions

- **In the following we will refer to the Huffman model, which requires the circuit to work in fundamental mode.**
- **Classic synthesis algorithms will allow to eliminate races and hazards**

Be careful: nobody can guarantee that the external world works in fundamental mode