

Summer Session I, 2003
CSE 141L
Projects in Computer Architecture

General Information

Class room: Center 214
Time: Tue. 6 - 8:50 PM

Instructor: Pramod V. Argade
Office: AP&M 3151
Office Hours: Thursday 6 - 7:30 PM
Email: p2argade@cs.ucsd.edu

TA: Anjum Gupta
Office: AP&M 2444
Office Hours: Thursday 3:30 – 5:00 PM and Friday 3:30 - 5 PM
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TA: Saurabh Panjwani
Office: AP&M 2444
Office Hours: Monday and Wednesday 3:30 - 5 PM
Email: panjwani@cs.ucsd.edu

Johnny's hours are cancelled for now.

General description of the course

In this course you will design Instruction Set Architecture for a 8-bit processor and design the hardware and test it. You will optimize your architecture and implementation for three array processing tasks described in the Lab Assignment 1.

Prerequisites

You must have completed Logic Design Courses CSE 140 and CSE140L. By completing CSE 140L, you must have working knowledge of either LogicWorks 4 or Xilinx Foundation tools. We will use LogicWorks 4 to design the processor and the TAs are familiar with this tool. You may use Xilinx tool, but TAs may not be able to help you with Xilinx tools related issues. Please contact the instructor if you are planning to use Xilinx tools.

Grading Information:

There will be 4 lab assignments during the course. Each lab requires the submission of a well written lab report as well electronic submission of programs or logic design. Your grade will be entirely determined by the quality of these lab reports and the completeness of the lab work which the submitted work will demonstrate. You have one week to

complete each lab and turn in your reports. For this course to be a rewarding and productive experience for all of us, we need to be very disciplined in our grading and you need to be very prompt with submitting assignments. Labs will be due in the beginning of the next class. No late submissions are allowed.

Each lab will be worth 100 points. Percentage weight of each lab for your grade is as follows:

- Lab 1: 20%
- Lab 2 :20%
- Lab 3: 25%
- Lab 4: 35%.

There will be no midterms and no final for the course.

This being a summer session, there is a short amount of time in which to complete the assignments. You are encouraged to work in groups. Form your own groups of from 1 to 3 people. Don't leave the first class without forming a group. If you need help forming a group stay around after class and I will help you. Once you establish a group, it can be changed only with the consent of the instructor.

You may appeal grades on labs to the TA, who graded them. If that does not lead to a satisfactory resolution, you may discuss with me. You have one week from when we return the lab to appeal the grade. For the assignments, you will be required to use Logic Works or Xilinx. I will not be teaching the tools or their use. Logic Works is available as follows:

- AP&M Room 2444
- Personal copies of LogicWorks are available in the bookstore.

Academic Honesty:

Work within your own group. Following is not permitted:

- Discussion of the lab assignments with someone in other group or someone who has already completed the lab, including prior quarters.
- Looking at a completed write-up of another student or group.
- Finding hardware solutions in textbooks or on the web, or anywhere else.
- Copying designs, or portions of designs from others outside your group or from previous quarters.
- Soliciting, receiving, or providing assistance to others outside your group.
- Altering timing data from Logic Works to make it appear that your design functions correctly or differently than it does.