CSE 231 Spring 1998
HW 3

1(a) We have the total of six webs. We observe that the two definitions of the variable d in <s5> and <s7> belong to the same web along with the use of d in <s8>. Moreover, there are two different webs for the variable b. One is composed by the definition of b in <s2> and the uses in <s3>, <s5> and <s7> and the other is formed by the definition in <s8> and use in <s9>.

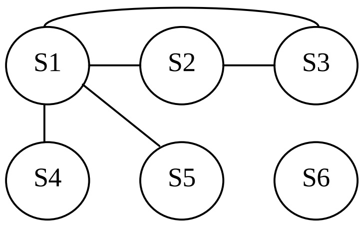
```
<s1>                a := 1
<s2>                b := 2
<s3>                c := a + b
<s4>                if (…) then go to L3
<s5>                d := a + b
<s6>                go to L4
<s7>        L3:     d := c + b
<s8>        L4:     b := a – d
<s9>                f := a * b
```

1(b)

Code with symbolic registers (we assigned a symbolic register for each web shown in 1(a)):

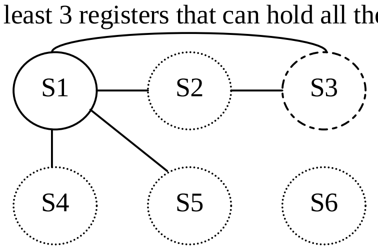
```
<s1>                S1 := 1
<s2>                S2 := 2
<s3>                S3 := S1 + S2
<s4>                if (…) then go to L3
<s5>                S4 := S1 + S2
<s6>                go to L4
<s7>        L3:     S4 := S3 + S2
<s8>        L4:     S5 := S1 – S4
<s9>                S6 := S1 * S5
```

Assuming that only f is alive by the end of the code segment execution, we have the following Interference Graph:



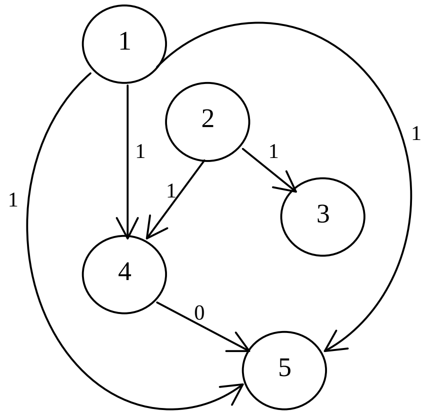
1(c) Maxlive is 3 for this program, more specifically a, b and c are live at the same program point.

1(d) The Interference Graph was colored with 3 colors as shown following. Moreover, if we assume that we have at least 3 registers that can hold all the variables of this code, then maxlive is achieved.



2(a) Dependence DAG for the block:

```
1) r1 := [r7+4](4)        (load)
2) r2 := [r7+8](2)        (load)
3) r3 := r2 + 2
4) r4 := r1 + r2
5) [r5](4) := r4          (store)
```



2(b) Delay computed for each node according to algorithm of the textbook (section 17.1, page 538):

Node	Delay
1	3
2	2
3	0
4	2
5	2

3(b) A possible scheduling for the DAG would be the following:

Cycle	Node
1	2
2	1
3	3
4	4
5	5

We observe that since instructions **1**, **2** and **5** take 2 cycles executing, the total block execution will take the total time of 8 cycles.