

This is a take-home exam. You are allowed to check books, notes, and conduct an internet search. However, you are expected to work on the solution by yourself. No discussion with anyone else is allowed.

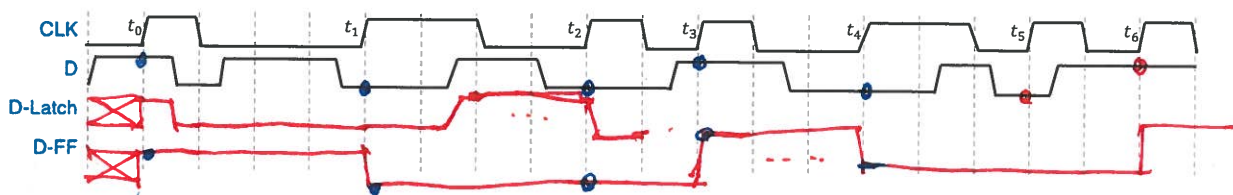
There are two parts to the exam. Part A weighs 90 points. Part B weighs 10 points. However, in Part B, the total weight of the problems is higher than 10 points. You are encouraged to earn up to 10 points. In other words, there is no penalty on wrong solutions in Part B, but the maximum points to earn are limited to 10 points.

Please read the following instructions carefully. If you are unclear about any of the questions on the exam, make the most plausible assumption to answer the question. Instructors and proctors will not answer questions on the exam material. **All the Best!**

Part A: (90 pts)

1 Timing Diagram of Latch and Flip-Flop

Given the input waveforms shown below, sketch the output D-Latch of the latch and the output D-FF of the flip-flop. Label your drawing at the time points of the rising edges of the clock as shown in the figure. (20 pts)



2 Finite State Machine

A pattern recognizer inputs a string of binary bits $x(t)$ and outputs $y(t) = 1$ whenever $x(t-3, t) = 1011$ or 1010 ; $y(t) = 0$ otherwise. (30 pts)

1. Draw the state diagram for the state machine using a minimal number of states.
2. Write the state table for a state machine using 2 D Flip Flops.
3. Describe $y(t)$, $D_1(t)$, $D_0(t)$ as functions of variables $(x, Q_1(t), Q_0(t))$ in minimal sum-of-products expressions. No need to draw the logic diagram.

3 Mealy and Moore Machine Conversion

Given a state table as below, each entry of the table is the next state and output. (20 pts)

id	$Q_1(t) Q_0(t)$	$x(t) = 0$	$x(t) = 1$
0	S0	S0,0	S1,1
1	S1	S0,1	S3,0
2	S2	S1,0	S3,1
3	S3	S2,0	S4,1
4	S4	S2,1	S3,0

$S0,0$ $S0,1$
 $S1,0$ $S1,1$
 $S2,0$ $S2,1$
 $S3,0$ $S3,1$
 $S4,1$

1. Fill the following table as the machine starts at state S0 and process through the given input x from CLK (Clock) sequence = 1 to 10.

CLK	1	2	3	4	5	6	7	8	9	10
x	0	1	0	1	0	1	1	0	1	0
state	S0									
y										

- Convert the above machine into a Moore machine. Write the state table.
- Use the Moore machine to fill the table starting at state S0 and process through the given input x from CLK (Clock) sequence 1 to 10.

CLK	1	2	3	4	5	6	7	8	9	10
x	0	1	0	1	0	1	1	0	1	0
state	S0									
y										

4 Timing and Retiming

For the following circuit (figure 4, the timing characteristics of the components are summarized below.(20 pts)

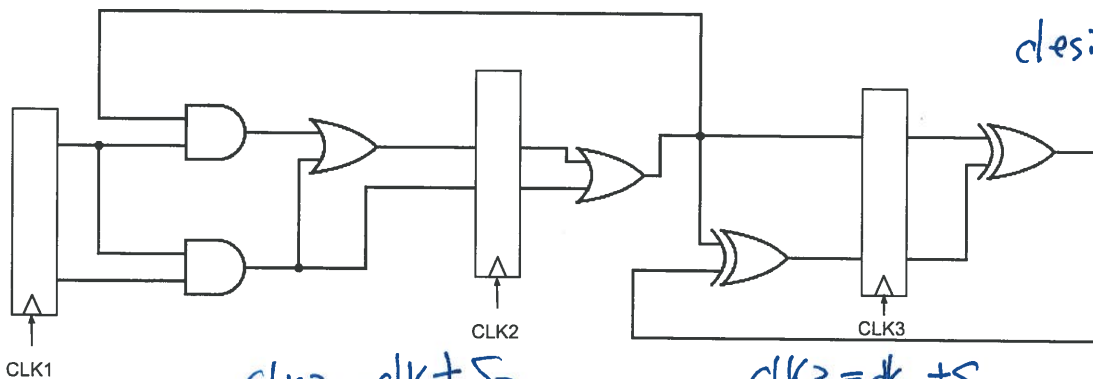
- Flip-flop: clock-to-Q maximum delay (propagation delay) $t_{pcq} = 20\text{ps}$, clock-to-Q minimum delay (contamination delay) $t_{ccq} = 15\text{ps}$, setup time $t_{setup} = 10\text{ps}$, hold time $t_{hold} = 20\text{ps}$
- Logic gate (e.g. Buffer, AND, OR, XOR, etc): propagation delay $t_{pd}(\text{gate}) = 15\text{ps}$, contamination delay $t_{cd}(\text{gate}) = 10\text{ps}$.

Longest Path $t_{pcq} + t_{pd}(\text{comb}) + t_{setup} \leq T + t_{skew}^{ji}$

Shortest Path $t_{ccq} + t_{cd}(\text{comb}) \geq t_{hold} + t_{skew}^{ji}$

designated skew

for
wise.



Clock	#gates
1 → 2	1, 2
~~1 → 3~~	
2 → 2	3, 3
2 → 3	1, 2
3 → 3	2, 2

Figure 1: A4. sequential circuit for retiming.

1. Derive the minimal clock cycle time T , suppose that there is no clock skew.
2. Derive the minimal clock cycle time T using a designated skew.

Part B: (10 pts) 8 In Part B, the total weight of the problems is higher than 10 points. You are encouraged to earn up to 10 points. In other words, there is no penalty on wrong solutions, but the maximum points to earn are limited to 10 points. Note that some problems are open, i.e. exact (perfect) solutions may be challenging to derive. Nonetheless, the principles taught in the class can be used to start the exploration.

B.1. Latch: With reference to the SR latch of slide 14 of lecture 7, replace the NOR gate at the bottom with a NAND gate. Complete the state table 1. (5 pts)

id	S	R	Q_t	y_t	Q_{t+1}	y_{t+1}	Q_{t+2}	y_{t+2}	Q_{t+3}	y_{t+3}
0	0	0	0	0						
1	0	0	0	1						
2	0	0	1	0						
3	0	0	1	1						
4	0	1	0	0						
5	0	1	0	1						
6	0	1	1	0						
7	0	1	1	1						
8	1	0	0	0						
9	1	0	0	1						
10	1	0	1	0						
11	1	0	1	1						
12	1	1	0	0						
13	1	1	0	1						
14	1	1	1	0						
15	1	1	1	1						

Table 1: B.1 State Table

B.2. Finite State Machine: With reference to page 4 of lecture 8 slides, we have a pattern-matching game with a fair coin (50% chance on either tail or head for each toss). The coin is tossed in sequence. Each person chooses a pattern of 4 consecutive tosses. The pattern that appears the first wins. Design a pattern so that you have the best chance to win. Explain your solution. (5 pts)

B.3. Timing and Retiming: For the following circuit (figure 4), the timing characteristics of the components are the same as problem A.4. (5 pts)

1. Derive the minimal clock cycle time T , suppose that there is no clock skew.
2. Derive the minimal clock cycle time T using a designated skew. Use $CLK1$ as the reference, write the amounts of skew of the rest of the clock signals, i.e. $CLK2$, $CLK3$ and $CLK4$ with respect to $CLK1$.

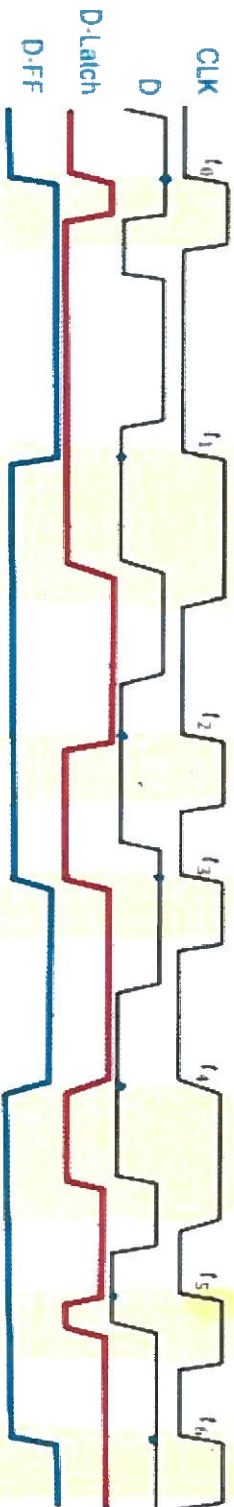
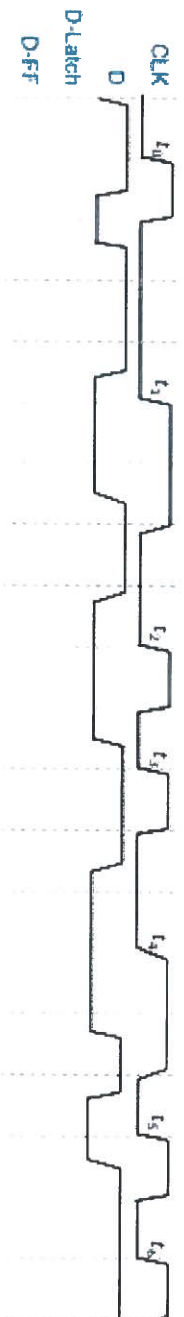


Midterm II Solutions

CSE 140

1 Timing Diagram of Latch and Flip-Flop

Given the input waveforms shown below, sketch the output D-Latch and the output D-FF of the flip-flop. Label your drawing at the time points of the rising edges of the clock as shown in the figure. (20 pts)

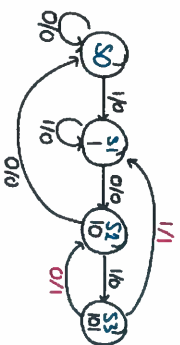


2 Finite State Machine

A pattern recognizer inputs a string of binary bits $x(t)$ and outputs $y(t) = 1$ whenever $x(t-3, t) = 1011$ or 1010 ; $y(t) = 0$ otherwise. (30 pts)

1. Draw the state diagram for the state machine using a minimal number of states.
2. Write the state table for a state machine using 2 D Flip Flops.
3. Describe $y(t)$, $D_1(t)$, $D_0(t)$ as functions of variables (x , $Q_1(t)$, $Q_0(t)$) in minimal sum-of-products expressions. No need to draw the logic diagram.

2. i)



ii)

x	$x=0$	$x=1$
S_0	$S_0, 0$	$S_1, 0$
S_1	$S_2, 0$	$S_1, 0$
S_2	$S_3, 0$	$S_3, 0$
S_3	$S_2, 1$	$S_1, 1$

iii)

t	0	1	2	3	4	5	6	7
x	0	0	0	1	0	1	0	1
Q_1	0	0	0	0	1	1	1	1
Q_0	0	0	1	0	0	0	1	0
y	0	0	0	0	1	0	1	1

x	0	1
Q_1	0	1
Q_0	0	1

$$D_1(t) = Q_0(t)x(t) + Q_1(t)Q_0(t)x(t)$$

x	0	1
Q_1	0	1
Q_0	0	1

$$D_0(t) = x(t)$$

x	0	1
Q_1	0	1
Q_0	0	1

$$y(t) = Q_1(t)Q_0(t)$$

3 Mealy and Moore Machine Conversion

Given a state table as below, each entry of the table is the next state and output. (20 pts)

id	$Q_1(t)$	$Q_0(t)$	$x(t) = 0$	$x(t) = 1$
0	S0		S0,0	S1,1
1	S1		S0,1	S3,0
2	S2		S1,0	S3,1
3	S3		S2,0	S4,1
4	S4		S2,1	S3,0

1. Fill the following table as the machine starts at state S0 and process through the given input x from CLK (Clock) sequence = 1 to 10.

CLK	1	2	3	4	5	6	7	8	9	10
x	0	1	0	1	0	1	1	0	1	0
state	S0									
y										

CLK	1	2	3	4	5	6	7	8	9	10
x	0	1	0	1	0	1	1	0	1	0
state	S0	S1	S0	S1	S0	S1	S2	S1	S0	S1
y	0	1	0	1	0	1	0	1	0	1

- Convert the above machine into a Moore machine. Write the state table.
- Use the Moore machine to fill the table starting at state S0 and process through the given input x from CLK (Clock) sequence 1 to 10.

CLK	1	2	3	4	5	6	7	8	9	10
x	0	1	0	1	0	1	1	0	1	0
state	S0									
y										

CLK	1	2	3	4	5	6	7	8	9	10
x	0	1	0	1	0	1	1	0	1	0
state	S0	S1	S0	S1	S0	S1	S2	S1	S0	S1
y	0	1	0	1	0	1	0	1	0	1

- Convert the above machine into a Moore machine. Write the state table.

Mealy

id	$Q_1(t)$	$Q_0(t)$	$x(t)=0$	$x(t)=1$
0	S0		S0,0	S1,1
1	S1		S0,1	S3,0
2	S2		S1,0	S3,1
3	S3		S2,0	S4,1
4	S4		S2,1	S3,0

→

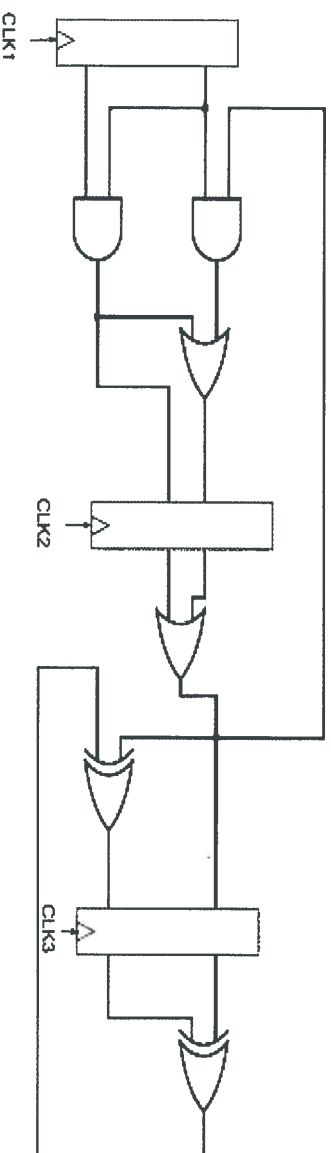
Moore

id	$Q_1(t)$	$Q_0(t)$	$x(t)=0$	$x(t)=1$	y
0	S0		S0	S1	0
1	S1		S0	S3	0
2	S2		S1	S3	0
3	S3		S2	S4	0
4	S4		S2	S3	1
5	S0		S0	S1	1
6	S1		S0	S3	1
7	S2		S1	S3	1
8	S3		S2	S4	1

4 Timing and Retiming

For the following circuit (Figure 4, the timing characteristics of the components are summarized below. (20 pts)

- **Flip-flop:** clock-to-Q maximum delay (propagation delay) $t_{pq} = 20\text{ps}$, clock-to-Q minimum delay (contamination delay) $t_{cq} = 15\text{ps}$, setup time $t_{setup} = 10\text{ps}$, hold time $t_{hold} = 20\text{ps}$
- **Logic gate (e.g., Buffer, AND, OR, XOR, etc.):** propagation delay $t_{pd}(gate) = 15\text{ps}$, contamination delay $t_{cd}(gate) = 10\text{ps}$.



1. Derive the minimal clock cycle time T , suppose that there is no clock skew.

2. Derive the minimal clock cycle time T using a designated skew.

(1) Longest path: $t_{pcq} + t_{pd} + t_{setup}$

Shortest path: $t_{cd} + t_{ccq}$

Constraints: $T + \text{skew} \geq \text{longest path}$, $t_{hold} + t_{skew} \leq \text{shortest path}$

(2) Paths: $t_{hold} + \text{skew} \leq \text{short}$ $\text{long} \leq T + \text{skew}$

CLK1->CLK2: $20 + S2 \leq 10 + 15$, $2 \times 15 + 20 + 10 \leq T + S2$

CLK2->CLK2: $20 \leq 3 \times 10 + 15$, $3 \times 15 + 20 + 10 \leq T$

CLK2->CLK3: $20 + S3 - S2 \leq 10 + 15$, $2 \times 15 + 20 + 10 \leq T + S3 - S2$

CLK3->CLK3: $20 \leq 2 \times 10 + 15$, $2 \times 15 + 20 + 10 \leq T$

(3) Linear Programming:

Min T

$20 + S2 \leq 25$, $60 \leq T + S2$

$20 \leq 45$, $\underline{75 \leq T}$

$20 + S3 - S2 \leq 25$, $60 \leq T + S3 - S2$

$20 \leq 35$, $60 \leq T$

(4) Solutions:

A1: $T = 75$ (ps)

A2: $T = 75$ (ps), $S2 = S3 = 0$

Let us assume noise 5
 $S2 = S3 = 0$ ps
 $\Rightarrow T = 75$ ps

B.1. Latch: With reference to the SR latch of slide 14 of lecture 7, replace the NOR gate at the bottom with a NAND gate. Complete the state table 1. (5 pts)

$$Q = (R + y)'$$

$$y = (SQ)'$$

id	S	R	Q_i	y_i	Q_{i+1}	y_{i+1}	Q_{i+2}	y_{i+2}	Q_{i+3}	y_{i+3}
0	0	0	0	0	1	1	0	1	0	1
1	0	0	0	1	0	1	0	1	0	1
2	0	0	1	0	1	1	0	1	0	1
3	0	0	1	1	0	1	0	1	0	1
4	0	1	0	0	0	1	0	1	0	1
5	0	1	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	0	1	0	1
7	0	1	1	1	0	1	0	1	0	1
8	1	0	0	0	1	1	0	0	1	1
9	1	0	0	1	0	1	0	1	0	1
10	1	0	1	0	1	0	1	0	1	0
11	1	0	1	1	0	0	1	1	0	0
12	1	1	0	0	0	1	0	1	0	1
13	1	1	0	1	0	1	0	1	0	1
14	1	1	1	0	0	0	0	1	0	1
15	1	1	1	1	0	0	0	1	0	1

Table 1: B.1 State Table

```
import random
pat = 'HHHT'
n_avg = 50000
avg_num_toss = 0
for i in range(n_avg):
    num_toss = 1
    cur = random.choice(['H', 'T'])
    while cur != pat:
        num_toss += 1
        cur = cur+random.choice(['H', 'T'])
    if len(cur)>len(pat):
        cur = cur[len(cur)-len(pat):]
    avg_num_toss += num_toss/n_avg
print(avg_num_toss)
```

https://colab.research.google.com/drive/1AwIO7nD2ubJlx2VOJWE_4ZotCBwtlHn?usp=sharing

B.2. Finite State Machine: With reference to page 4 of lecture 8 slides, we have a pattern-matching game with a fair coin (50% chance on either tail or head for each toss). The coin is tossed in sequence. Each person chooses a pattern of 4 consecutive tosses. The pattern that appears the first wins. Design a pattern so that you have the best chance to win. Explain your solution. (5 pts)

Let the pattern be denoted by $\bar{p} = p_1, p_2, p_3, p_4$. For $i \in \{1, \dots, 4\}$, define $\bar{q}_i \triangleq p_1, \dots, p_i$. Suppose the first occurrence of $\bar{q}_i$ occurs X_i tosses after the first occurrence of $\bar{q}_{i-1}$. Notice that our pattern of interest $\bar{p}$ occurs after $X_1 + X_2 + X_3 + X_4$ coin tosses.

Without loss of generality suppose $p_1 = H$. This results in 8 possible patterns for $\bar{p}$. Evaluate the expectation $E[X_1 + X_2 + X_3 + X_4]$ and select the pattern(s) with the least expectation.

Consider $\bar{p} = HHHT$. From the linearity of expectations

$E[X_1 + X_2 + X_3 + X_4] = E[X_1] + E[X_2] + E[X_3] + E[X_4]$. Observe that X_1 follows the geometric distribution with parameter 0.5 resulting in $E[X_1] = 2$. The following recurrence holds for

$E[X_2] = P(H) + P(T)(1 + E[X_1] + E[X_2])$ resulting in $E[X_2] = 4$. Similarly use

$E[X_3] = P(H) + P(T)(1 + E[X_1] + E[X_2] + E[X_3])$ to obtain $E[X_3] = 8$. Finally for X_4 ,

$E[X_4] = P(T) + P(H)(1 + E[X_4])$, resulting in $E[X_4] = 2$. Therefore $E[X_1 + X_2 + X_3 + X_4] = 16$.

A similar analysis may be done for the other patterns from which we conclude that the patterns $\bar{p} = HHHT, HHTT, HTTT$ are the patterns that likely to occur before any other pattern.

An alternative approach is to use simulations to evaluate this expectation, as shown in the following code and Google Colab notebook. Note: Credit will be given for answers that solve this problem via finite state machines/Markov chains as well.

B.3. Timing and Retiming: For the following circuit (figure 4), the timing characteristics of the components are the same as problem A.4. (5 pts)

1. Derive the minimal clock cycle time T , suppose that there is no clock skew.
2. Derive the minimal clock cycle time T using a designated skew. Use $CLK1$ as the reference, write the amounts of skew of the rest of the clock signals, i.e. $CLK2$, $CLK3$ and $CLK4$ with respect to $CLK1$.

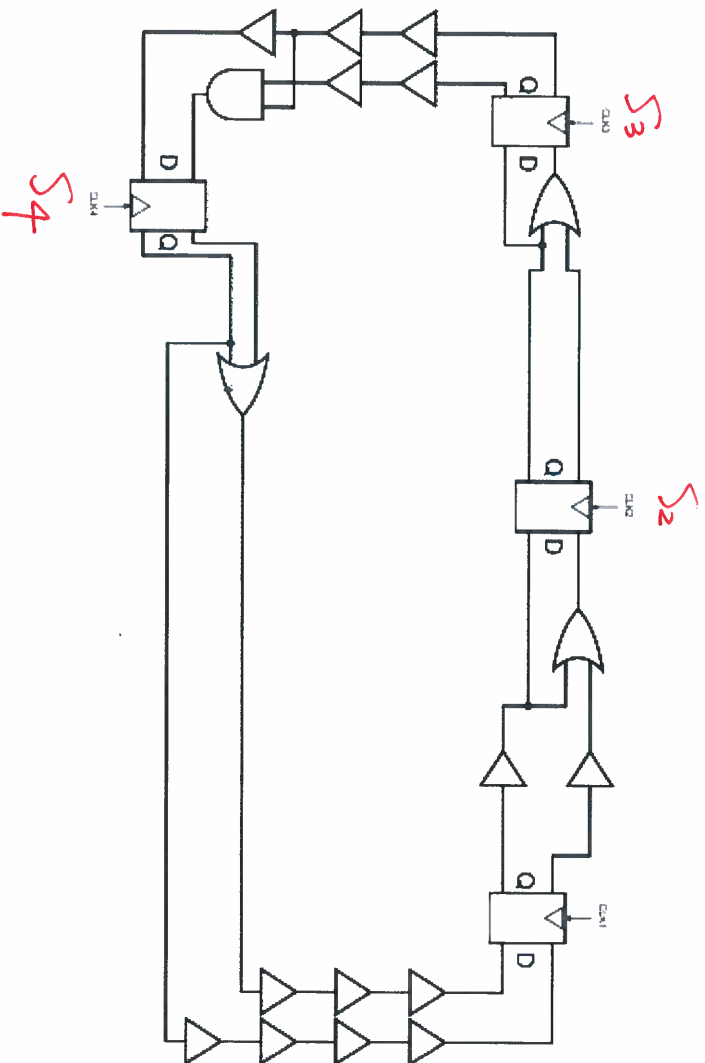


Figure 2: B3 sequential circuit for retiming.

B.3

B.3. Timing and Retiming: For the following circuit (figure 4), the timing characteristics of the components are the same as problem A.4. (5 pts)

Flip-Flop

$$t_{pcq} = 20ps$$

$$t_{ccq} = 15ps$$

$$t_{setup} = 10ps$$

$$t_{hold} = 20ps$$

Gate

$$t_{pd} = 15ps$$

$$t_{cd} = 10ps$$

Setup time constraint:

$$T_C \geq t_{pcq} + t_{pd} + t_{setup} - t_{skew}$$

Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} + t_{skew}$$

B.3 (1)

1. Derive the minimal clock cycle time T , suppose that there is no clock skew (2 pts).

Length of maximal path: 4 (CLK1-CLK4)

1. Setup time constraint:

$$T_C \geq t_{pcq} + t_{pd} + t_{setup} - t_{skew}$$

2. Maximal paths:

- clk 1->2: 2
- clk 2->3: 1
- clk 3->4: 3
- clk 4-> 1: 4

3. Solution

$$T_c \geq 20 + 4 \cdot 15 + 10ps + 0 = 90ps$$

B.3 (2)

2. Derive the minimal clock cycle time T using a designated skew. Use CLK1 as the reference, write the amounts of skew of the rest of the clock signals, i.e. CLK2, CLK3 and CLK4 with respect to CLK1 (3 pts).

1. Hold time constraint:

$$t_{ccq} + t_{cd} > t_{hold} + t_{skew}$$

Setup time constraint:

$$T_G \geq t_{pcq} + t_{pd} + t_{setup} - t_{skew}$$

2. Paths

◦ CLK1->CLK2

$$20 + S_2 < 10 + 15, 2 \cdot 15 + 20 + 10 \leq T + S_2$$

◦ CLK2-CLK3

$$20 + S_3 - S_2 < 15, 1 \cdot 15 + 20 + 10 \leq T + S_3 - S_2$$

◦ CLK3-CLK4

$$20 + S_4 - S_3 < 3 \cdot 10 + 15, 3 \cdot 15 + 20 + 10 \leq T + S_4 - S_3$$

◦ CLK4-CLK1

$$20 - S_4 < 4 \cdot 10 + 15, 4 \cdot 15 + 20 + 10 \leq T + S_4$$

3. Linear Programming

$$\begin{array}{ll} \min T & \\ s. t. & 20 + S_2 < 25, & 60 \leq T + S_2 \\ & 20 + S_3 - S_2 < 15, & 45 \leq T + S_3 - S_2 \\ & 20 + S_4 - S_3 < 45, & 75 \leq T + S_4 - S_3 \\ & 20 - S_4 < 55, & 90 \leq T - S_4 \end{array}$$

4. Solution

$$(1) T = 90ps$$

$$(2)$$

$$\begin{array}{l} T = 67.5ps \\ S_2 = -7.5ps \\ S_3 = -30ps \\ S_4 = -22.5ps \end{array}$$