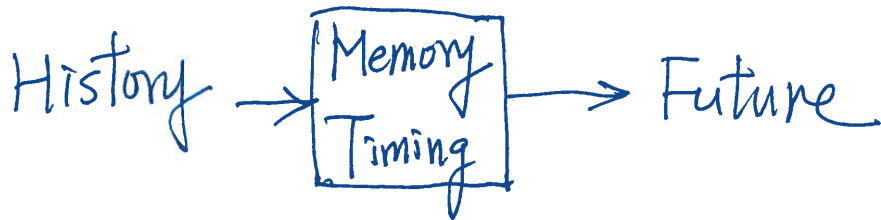


Lecture 7:
Sequential Networks

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State
transition



Part II: Sequential Networks

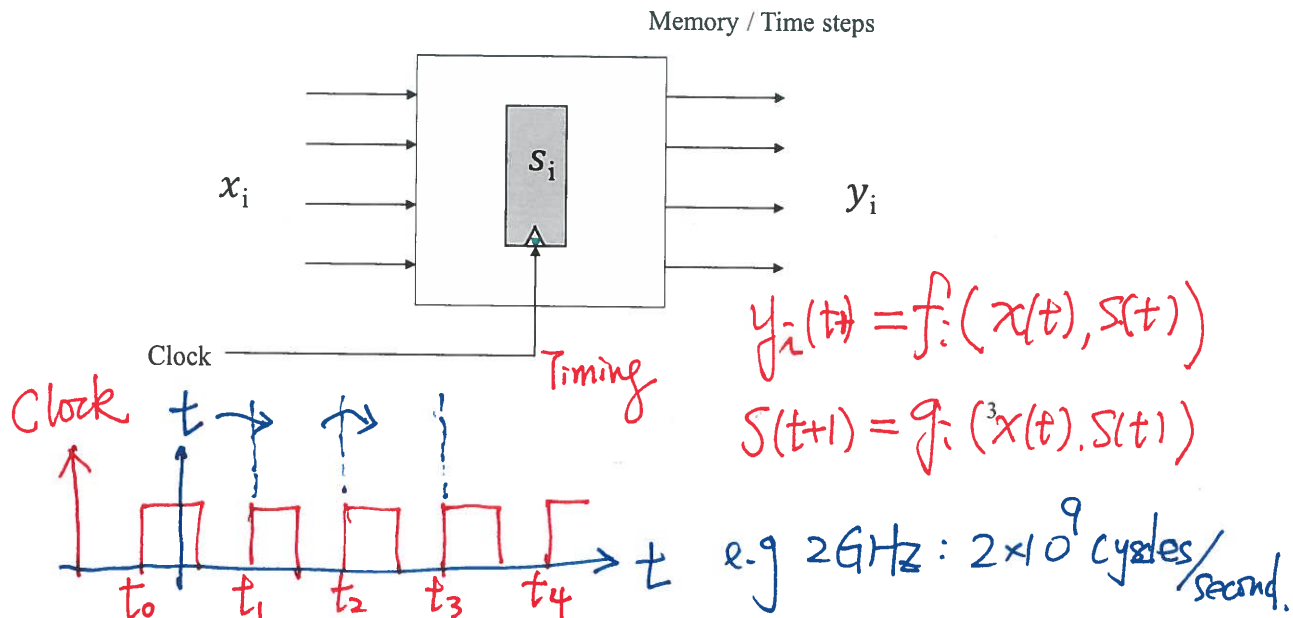
1. Introduction
 1. Sequential Circuits
 2. Memory Hierarchy *(Asynchronous System)*
 3. Basic Mechanism of Memory
2. Basic Building Blocks
 1. Latches
 2. Flip-Flops
 3. Examples of Memory Modules
3. Implementation

1. Introduction: What is a sequential circuit?

“A circuit whose output depends on current inputs and past outputs”

“A circuit with **memory**”

Memory: a key parameter is Time



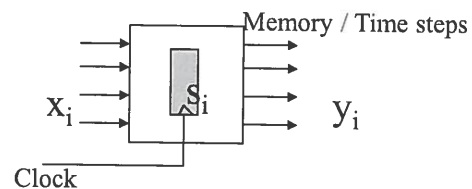
1. Introduction: Sequential Network Key features

Memory: Flip flops

Specification: Finite State Machines

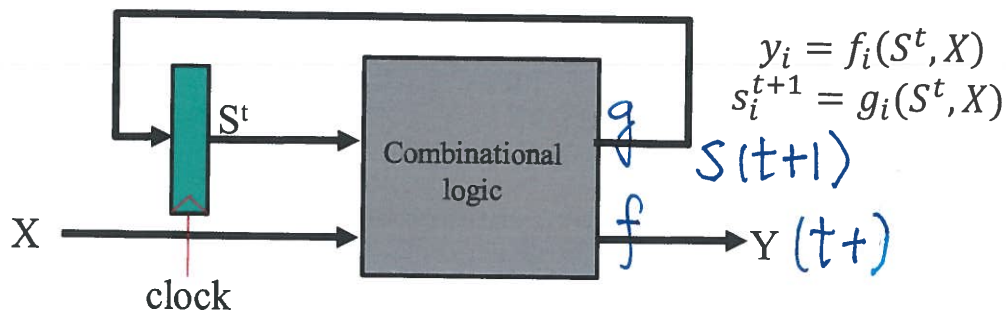
Implementation: Excitation Tables

Main Theme: Timing



Present time = t and next time = $t+1$

Timing constraints to separate the present and next times.

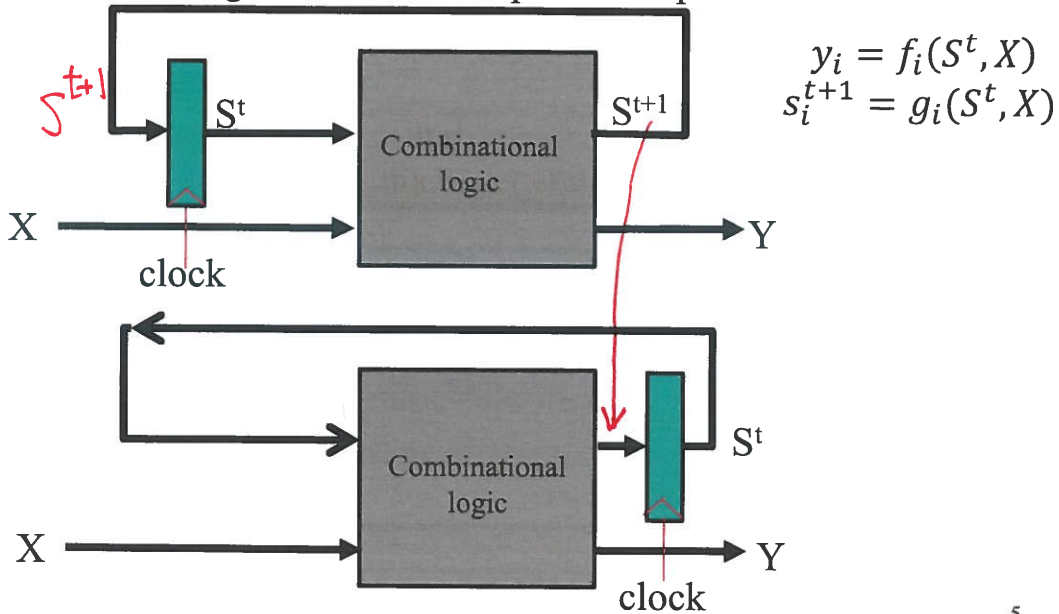


1. Introduction: Sequential Network Key features

Main Theme: Timing

Present time = t and **next time = t+1**

Timing constraints to separate the present and next times.

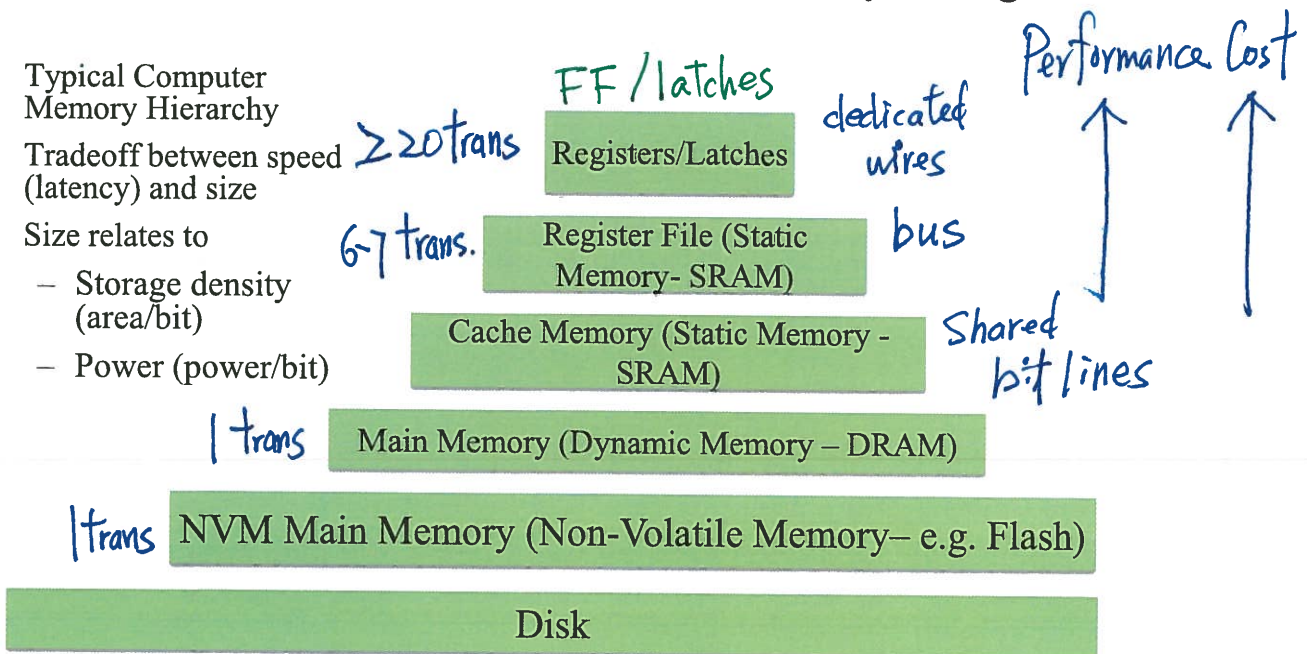


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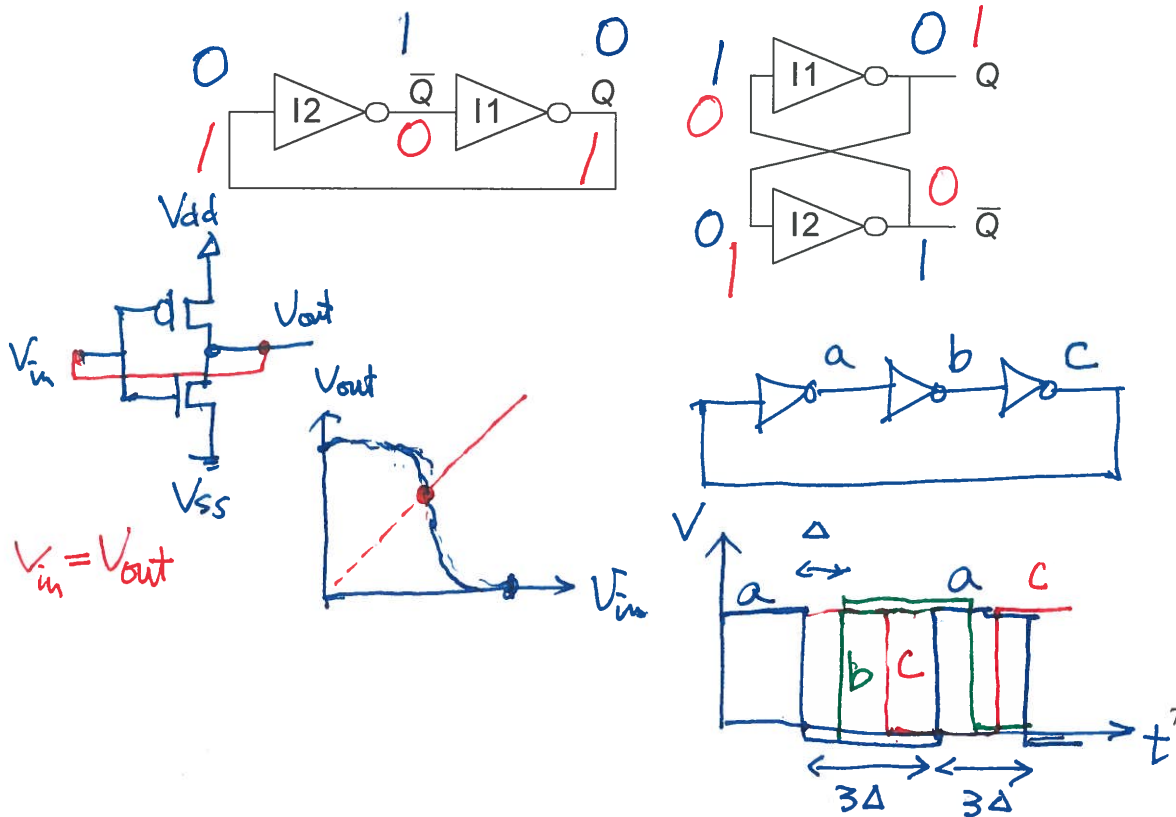
1. Introduction: Different Types of Memory/Storage

- Typical Computer Memory Hierarchy
- Tradeoff between speed (latency) and size
- Size relates to
 - Storage density (area/bit)
 - Power (power/bit)



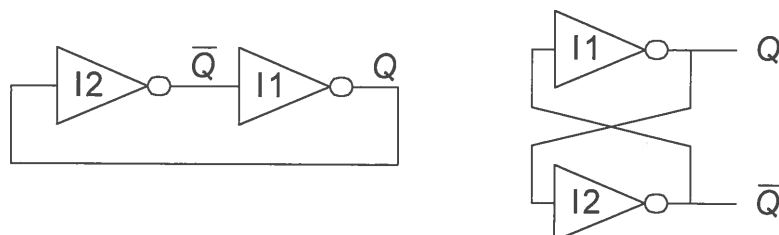
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1. Introduction: Fundamental Memory Mechanism



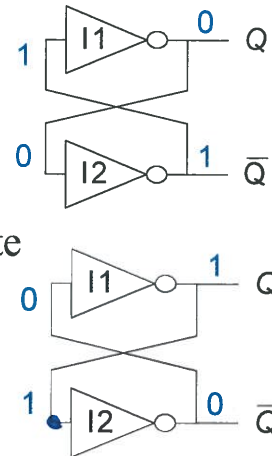
1. Introduction: Memory Mechanism Capacitive Load

- Fundamental building block of sequential circuits
- Two outputs: $\bar{Q}$, Q
- There is a feedback loop!
 - In a typical combinational logic, there is no feedback loop.
- No inputs



1. Introduction: Capacitive Loads

- Consider the two possible cases:
 - $Q = 0$: then $Q' = 1$ and $Q = 0$ (consistent)
 - $Q = 1$: then $Q' = 0$ and $Q = 1$ (consistent)
 - Bistable circuit stores 1 bit of state in the state variable, Q (or Q')
 - Hold the value due to capacitive charges and feedback loop strengthening
- But there are **no inputs to control the state**



Capacitive load $\rightarrow$ memory.

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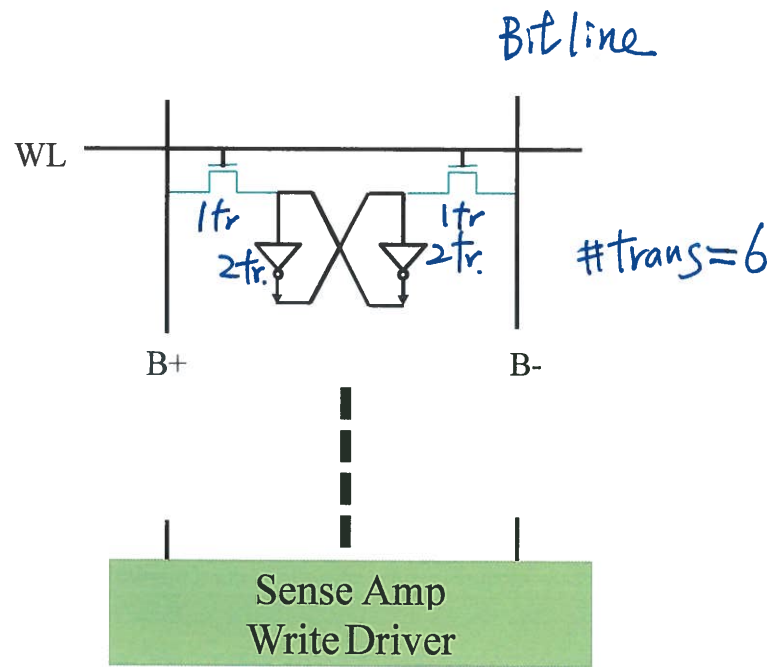
Example

Q. Given a memory component made of a loop of inverters, the number of inverters in the loop has to be

- A. Even
- B. Odd
- C. No constraints

1. Introduction: Memory Storage Mechanism

- Word line (WL) to access cell
- Read – measure voltage difference between B+ and B-
- Write – force values of B+ and B- which may flip the cell
- Static Random Access Memory - SRAM



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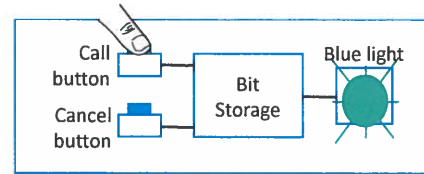
2. Basic Building Blocks

- Latches (Level Sensitive)
 - SR Latches, D Latches
- Flip-Flops (Edge Triggered)
 - D FFs, (JK FFs, T FFs)
- Examples of Memory Modules
 - Registers, Shift Registers, Pattern Recognizers, Counters, FIFOs

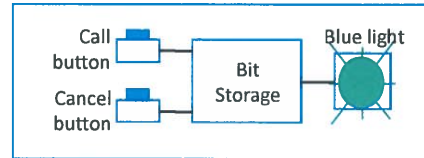
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2. Basic Building Blocks: Flight attendant call button

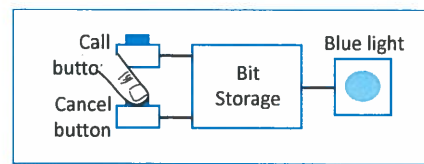
- Flight attendant call button
 - Press call: light turns on
 - Stays on* after button released
 - Press cancel: light turns off
 - Logic gate circuit to implement this?



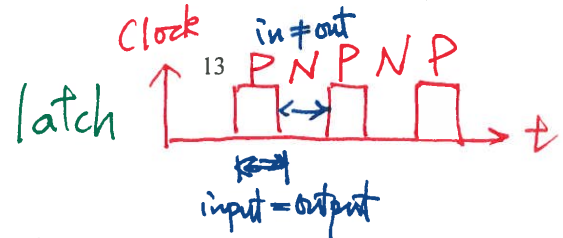
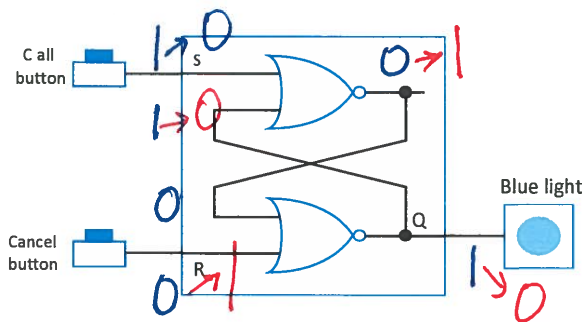
1. Call button pressed – light turns on



2. Call button released – light stays on

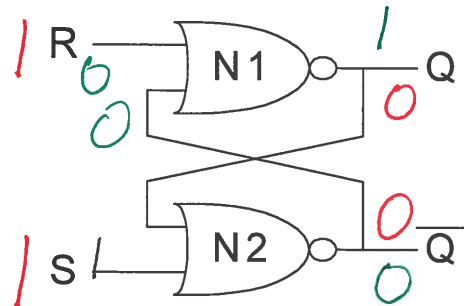


3. Cancel button pressed – light turns off



2. Basic Building Blocks: SR (Set/Reset) Latch

- SR Latch



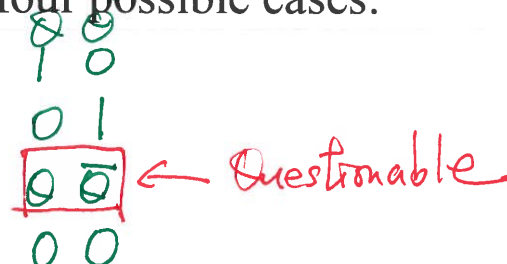
- Consider the four possible cases:

– $S = 1, R = 0$

– $S = 0, R = 1$

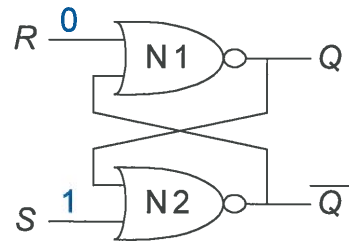
– $S = 0, R = 0$

– $S = 1, R = 1$

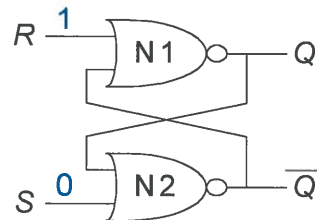


2. Basic Building Blocks: SR Latch Analysis

– $S = 1, R = 0$: then $Q = 1$ and $\overline{Q} = 0$



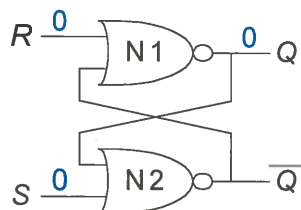
– $S = 0, R = 1$: then $Q = 0$ and $\overline{Q} = 1$



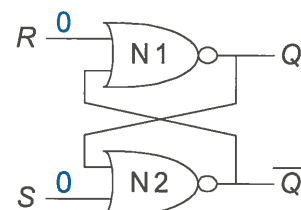
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2. Basic Building Blocks: SR Latch Analysis

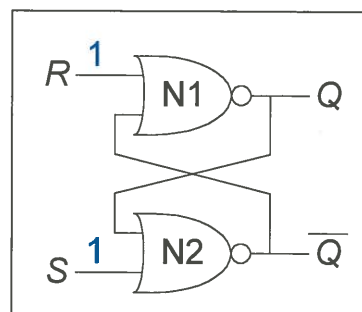
– $S = 0, R = 0$: then $Q = Q_{prev}$
 $Q_{prev} = 0$



$Q_{prev} = 1$

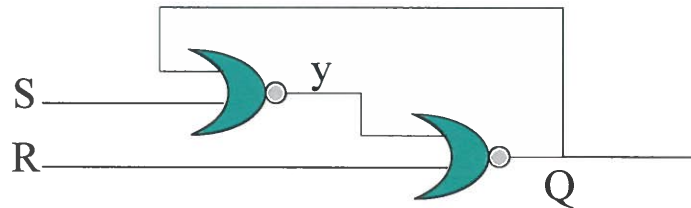
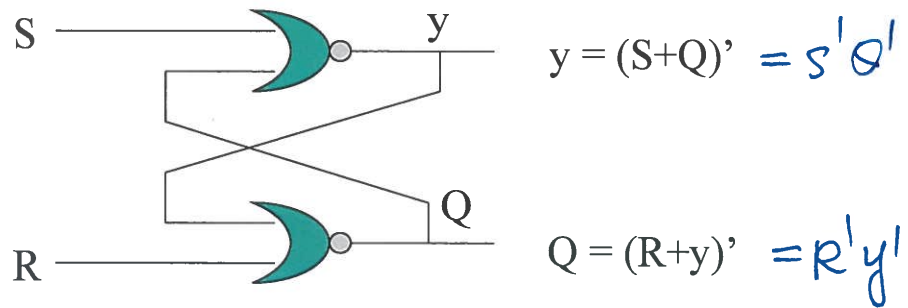


– $S = 1, R = 1$: then $Q = 0$ and $\overline{Q} = 0$



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2. Basic Building Blocks: SR Latch



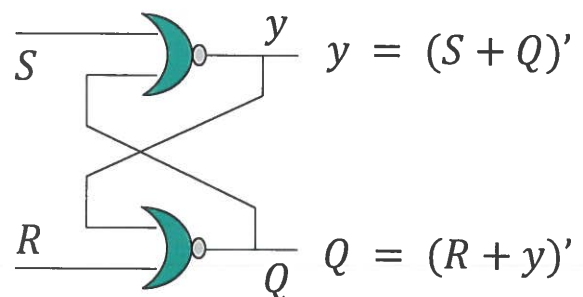
Inputs: S, R

State: (Q, y)

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id	S	R	Qt	yt	Qt	yt	Qt	yt	Qt	yt
0	0	0	0	0	1	1	0	0	1	1
1	0	0	0	1	0	1	0	1	0	1
2	0	0	1	0	1	0	1	0	1	0
3	0	0	1	1	0	0	1	1	0	0
4	0	1	0	0	0	1	0	1	0	1
5	0	1	0	1	0	1	0	1	0	1
6	0	1	1	0	0	0	0	1	0	1
7	0	1	1	1	0	0	0	1	0	1
8	1	0	0	0	1	0	1	0	1	0
9	1	0	0	1	0	0	1	0	1	0
10	1	0	1	0	1	0	1	0	1	0
11	1	0	1	1	0	0	1	0	1	0
12	1	1	0	0	0	0	0	0	0	0
13	1	1	0	1	0	0	0	0	0	0
14	1	1	1	0	0	0	0	0	0	0
15	1	1	1	1	0	0	0	0	0	0

Truth table of SR latch
with incremental steps in
time



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