

Lecture 1: Introduction to Digital Logic Design

*Hardware Construction
Optimization
Debugging
0/1 Boolean Algebra + Sequential Machine*

CSE 140: Components and Design Techniques for Digital Systems

Spring 2022

CK Cheng

Dept. of Computer Science and Engineering
University of California, San Diego

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Outlines

- Staff
 - Instructor, TAs, Tutors
- Logistics
 - Websites, Textbooks, Grading Policy
- Motivation
 - Moore's Law, Deep Learning, Quantum Computing
- Scope
 - Position among CSE courses
 - Coverage

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Staff: the Instructor

- Instructor: CK Cheng
- Education: Ph.D. in EECS UC Berkeley
- Industrial Experiences: Engineer of AMD, Mentor Graphics, Bellcore; Consultant for technology companies
- Email: ckcheng+140@ucsd.edu
- Office: Room 2130 CSE Building
- Office hours
 - TBA
- Websites
 - <http://cseweb.ucsd.edu/~kuan>
 - <http://cseweb.ucsd.edu/classes/sp22/cse140-a>

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Staff: TAs and Tutors

TAs

- Abraham, Elizabeth eabraham@ucsd.edu
- Holtz, Chester chholtz@ucsd.edu, Lead TA
- Jang, Wonsuk w1jang@ucsd.edu
- Li, Yuxin yul801@ucsd.edu
- Liu, Isabella lal005@ucsd.edu
- Ma, Jason jam043@ucsd.edu
- Wang, Kanlin kaw008@ucsd.edu

Tutors

- Dong, Jiayan jid001@ucsd.edu
- Huang, Yucheng yuh032@ucsd.edu
- Sun, William wis003@ucsd.edu

Office hours will be posted on the course website (piazza)

Logistics: Class Schedule

- Lecture: TR 3:30-4:50PM
- Discussion: F 3-350PM
- 4-5 Homework Assignments, 3 Exams: W4, W7, W10
- The Third Exam: Due time M 6:00PM, 6/6/2022 *Submission*

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Logistics: Textbooks

Reserved at library

- Digital Design and Computer Architecture by David Money Harris and Sarah L. Harris, Morgan Kaufmann (Reading Activities)
- Digital Systems and Hardware/Firmware Algorithms, Milos D. Ercegovac and Tomas Lang (System Designs, pdf file will be released)

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Logistics: Sites for the Class

- Class website
 - <http://cseweb.ucsd.edu/classes/sp22/cse140-a/index.html>
 - Syllabus
 - Class notes
 - Assignment: Homework and Reading Activities
 - Exercises: Solutions and Rubrics
- Forum: Piazza (Office Hrs., Online Discussion)
- Homework and Exam submission: Gradescope
- Lecture/Discussion Record: Podcast

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Logistic: Class Expectation

- Level 1: Concepts and Methods (Lecture and slides)
 - Class attendance of video record
- Level 2: Hands on Practices (Exercises)
 - Homework
- Level 3: Command of Materials (Samples of exams)
 - Exams: First part of exam (90%)
- Level 4: Extension and Exploration (Content beyond the textbook)
 - Exams: Second part of exam (10%)

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Logistics: Grading

Total pts distribution:

- Homework: 35pts (grade based on a subset of problems)
- Exams: 32.5pts for each of the best two out of 3 exams
 - Exam 1: Week 4
 - Exam 2: Week 7
 - Exam 3: (due 600PM, Monday 6/6/2022)
- Grading: The better choice of the following two categories
 - Exact score (100pts)
 - $A > 93$, $A- > 90$, $B+ > 87$, $B > 83$, $B- > 80$, $C+ > 77$, $C > 73$
 - $C- > 50$.
 - The curve (100% of class)
 - $A+$ top $x\%$ ($x < 5$)
 - $(A, A-)$ top $33 \pm \varepsilon\%$; $(B+, B, B-)$ top $66 \pm 2\varepsilon\%$

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Logistic: grading components

- Homework:
 - Due Wed night on Gradescope
 - Group discussion is encouraged. However, we are required to write individually
 - Discount 10% loss of credit for each day after the deadline but no credit **after the solution is posted.**
 - Some parts will be graded by completion only (**students are responsible for correct solutions**)
 - **Standard: Posted solutions and rubrics**

Logistic: 3 Exams

Exams: take-home exam taken within 48 hours

- Open book, notes, free to check websites
- Solution and grading policy will be posted after the exam.
- Exams are not cumulative but requires a good command of the previous exam content
- Two timeframe options for the class to decide
 - I. 80 minutes time frame: Finish the exam in 80 minutes after you start the exam.
 - II. 48 hours time frame: Deliver the result in 48 hours after the exam is posted.
- Exam schedule
 - I. Weekends
 - II. Weekdays
 - III. Sunday + Monday

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Course Problems...Cheating

- What is cheating?
 - Studying together in groups is not cheating but encouraged
 - Turned-in work must be *completely* your own.
 - Copying someone else's solution on a HW or Exam is cheating
 - Both “giver” and “receiver” are equally culpable
- We will be better off to work on the problem alone during the exam.
- We have to address the issue once the cheating is reported by someone (e.g. TA, Tutor, Student, etc.).

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Motivation

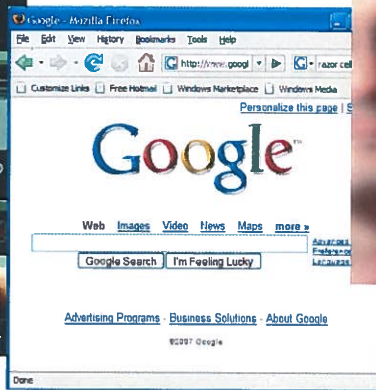
- Microelectronic technologies have revolutionized our world: cell phones, internet, rapid advances in medicine, etc.
- The semiconductor industry has grown from \$21 billions in 1985 to \$555.9 billions in 2021.

$$x^36 = \frac{555.9}{21}$$

$$\frac{2021}{-1985} = 36$$

$$x = ?$$

$$1.095$$



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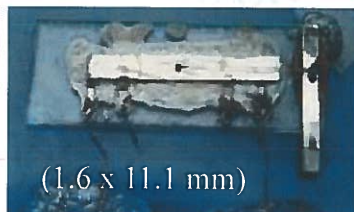
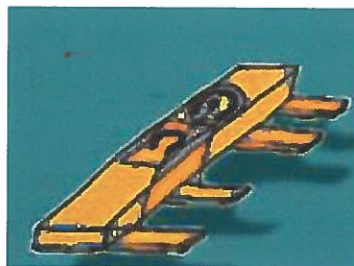
The Digital Revolution

Integrated Circuit: Many digital operations on the same material

Vacuum tubes



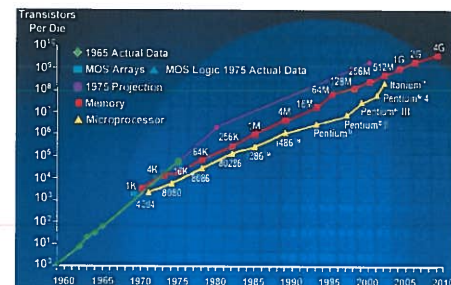
ENIAC



(1.6 x 11.1 mm)

Integrated Circuit

Exponential Growth of Computation



Moore's Law

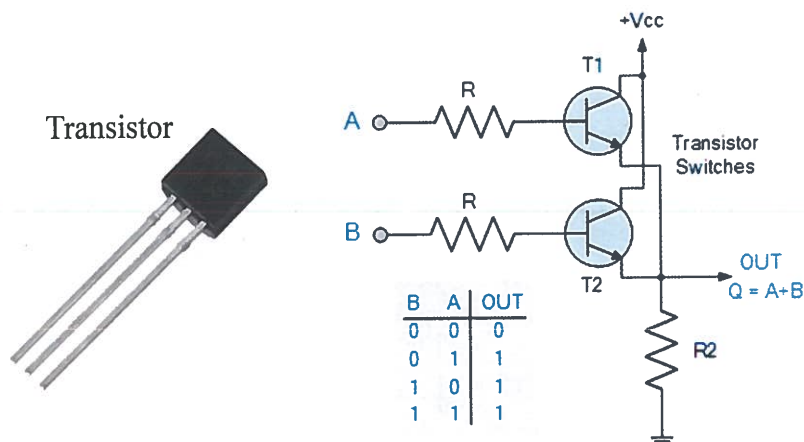
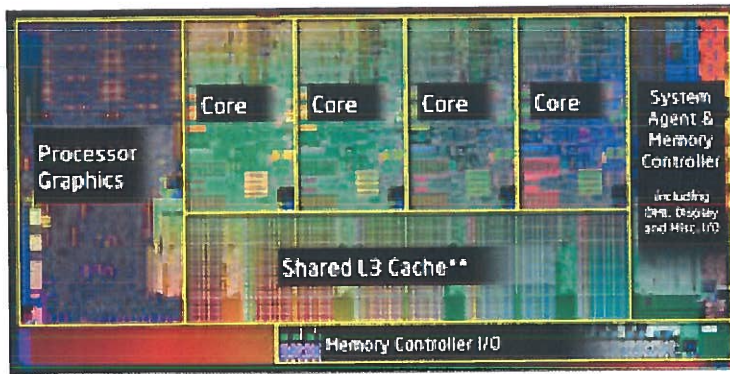
WWII
Stored Program Model

1949

1965

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Building complex circuits



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Robert Noyce, 1927 - 1990

- Nicknamed “Mayor of Silicon Valley”
- Co-founded Fairchild Semiconductor in 1957
- Co-founded Intel in 1968
- Co-invented the integrated circuit

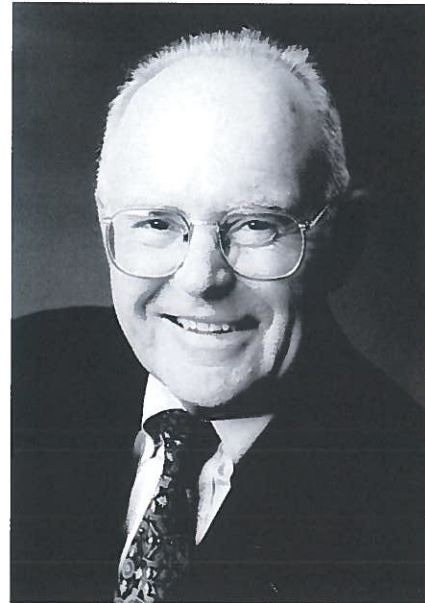


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Gordon Moore

- Cofounded Intel in 1968 with Robert Noyce.
- **Moore's Law:** the number of transistors on a computer chip doubles every 1.5 years (observed in 1965)

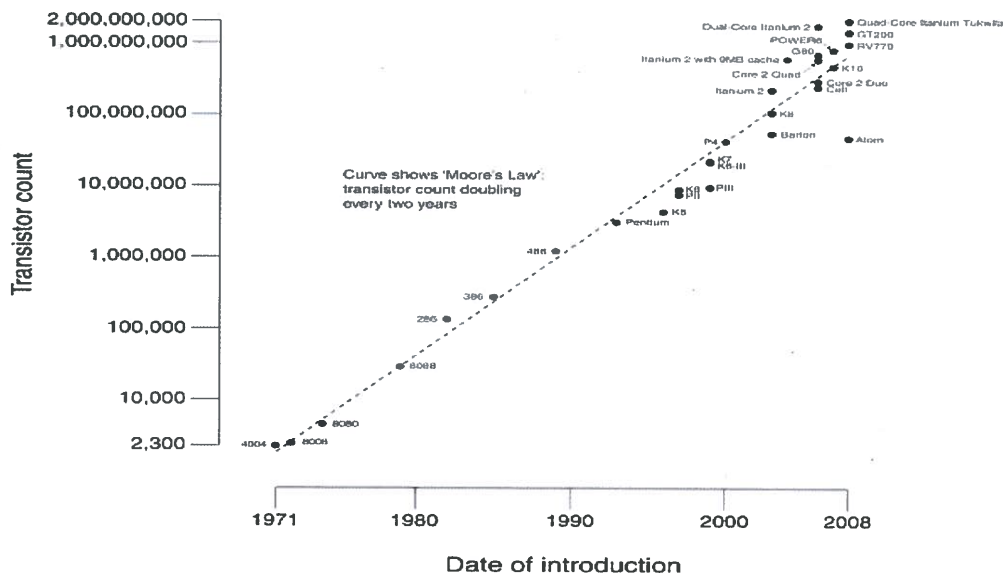
market ↑
revenue ↑
R&D ↑



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Technology Trends: Moore's Law

CPU Transistor Counts 1971-2008 & Moore's Law



- Since 1975, transistor counts have doubled every two years.
- Moore's law: wider applications: larger market: higher revenue: more R&D

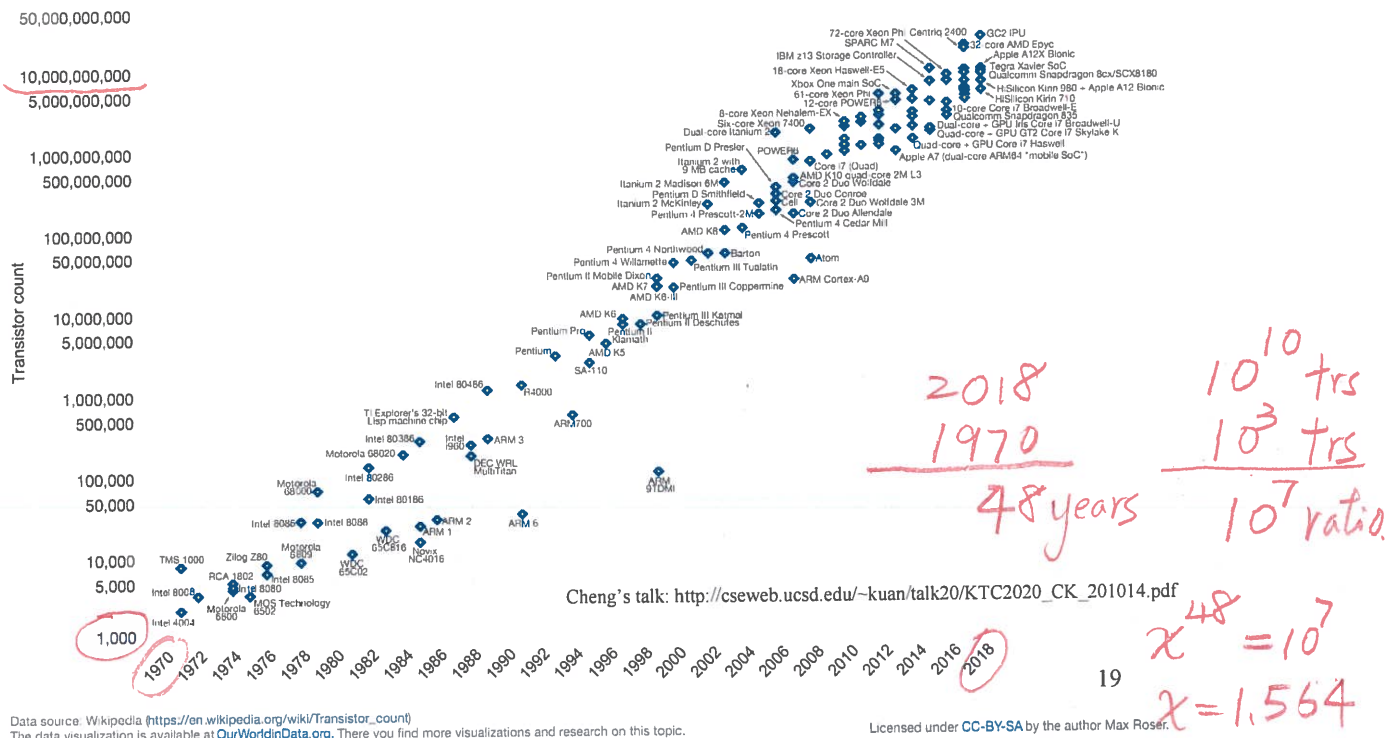
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Introduction: Moore in 1965

The complexity for minimum component costs has increased at a rate of roughly a factor of two/yr.

Moore's Law – The number of transistors on integrated circuit chips (1971-2018)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.

Our World
in Data

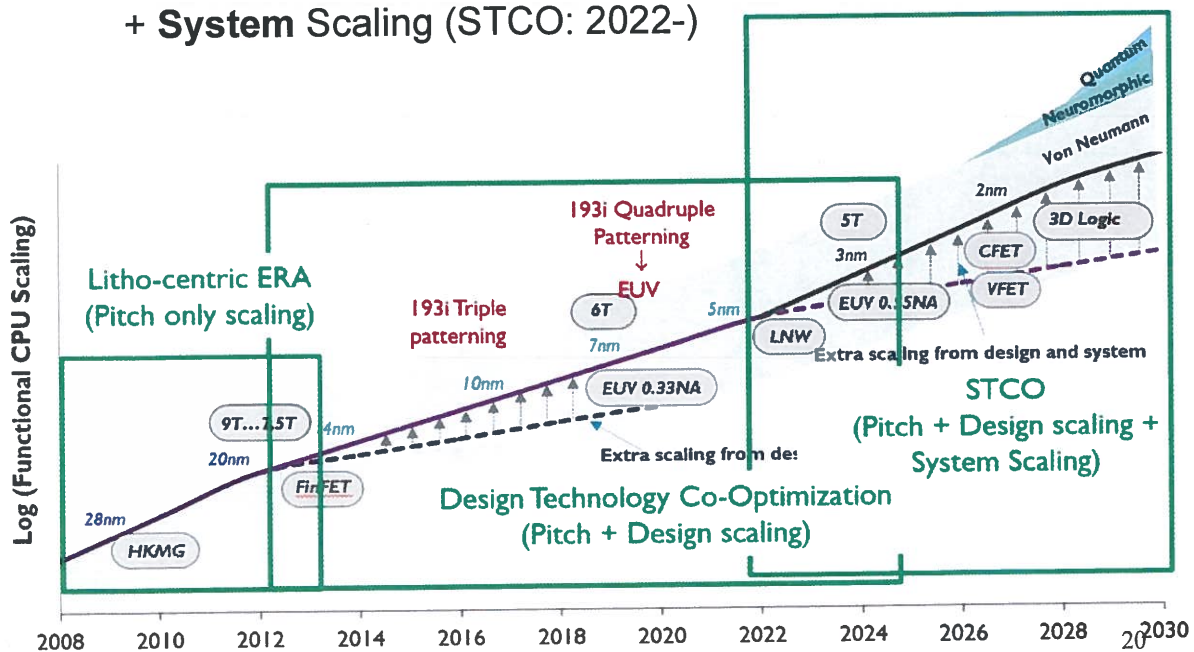
Moore's Law: Roadmap

Scaling Methods:

Pitch only (2008-2013)

+ **Design** Technology Co-Optimization (DTCO: 2012-2025)

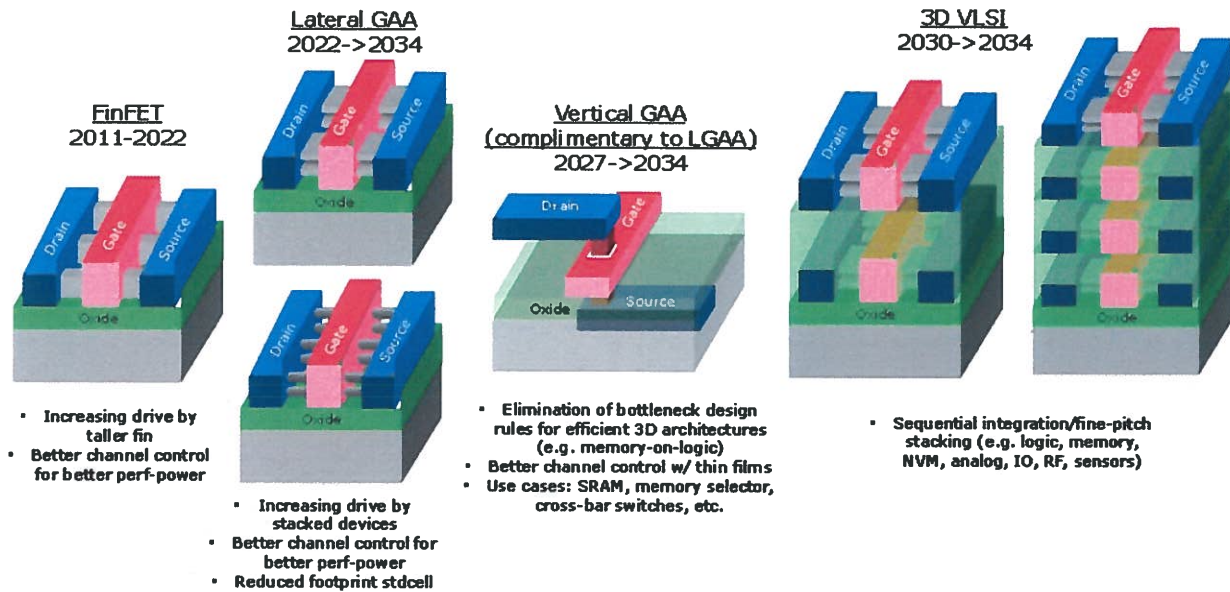
+ System Scaling (STCO: 2022-)



[S. M. Y. Sherazi et al., "Standard-cell design architecture options below 5nm node: The ultimate scaling of FinFET and Nanoshee," keynote, Proc. SPIE, 2019]

Year of 1st Production

2.5D/3D fine-pitch assembly + stacking



Change in the MOSFET device architecture from the 2D planar through 2.5D FinFets to 3D monolithic VLSI

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IEEE IRDS Executive Summary, pp. 53, 2020

New Technologies

- New materials and fabrication for devices
 - Low power devices
 - Three dimensional integrated circuits
 - Graphene
- New architecture
 - Machine learning, deep learning
- Quantum computing

Understand the principles to explore the future

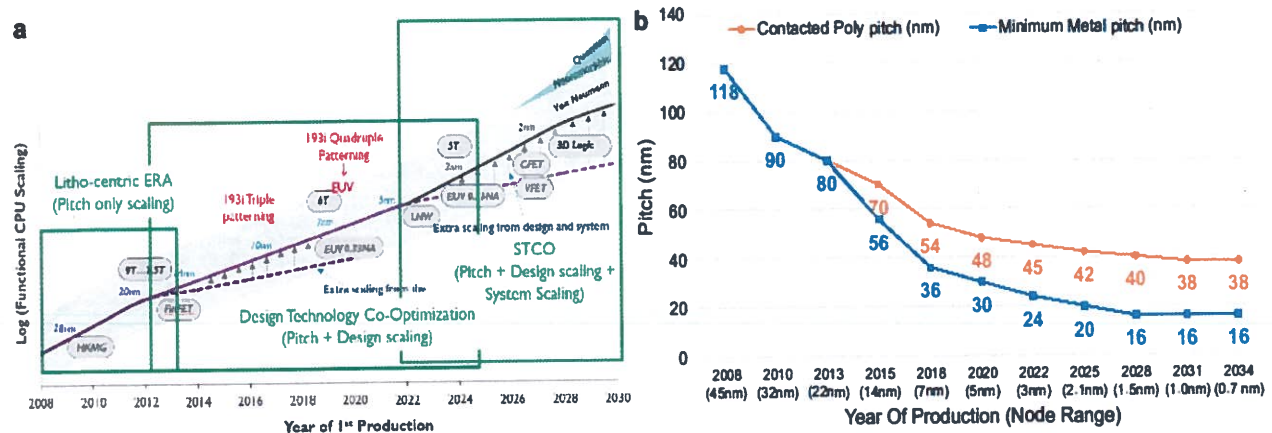
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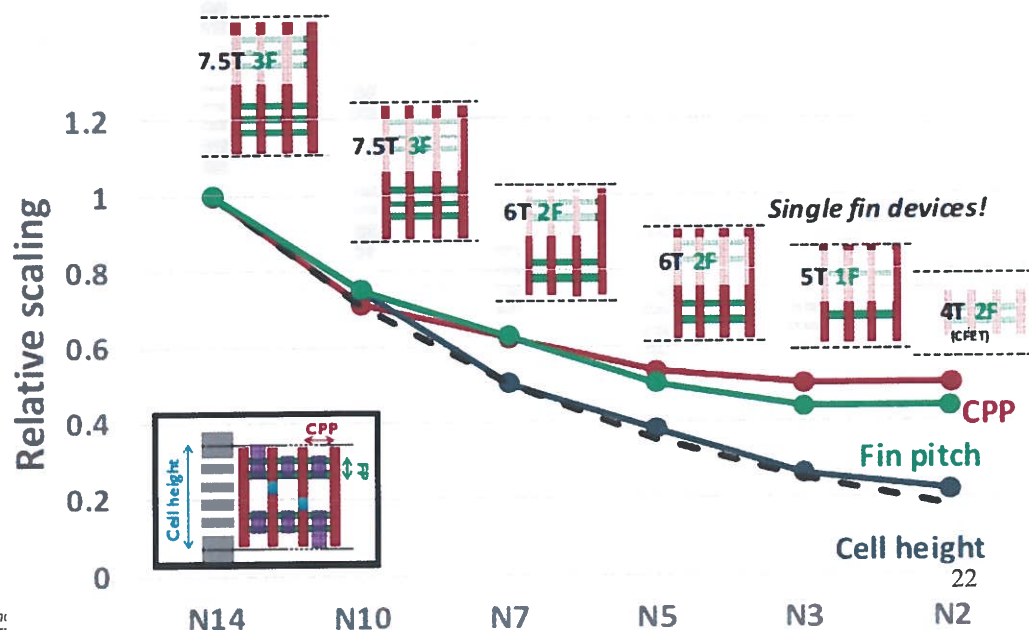
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Artificial Intelligence

- Logic and Reasoning
- Boolean Satisfiability (SAT)
 - Product of sum clauses
 - Diagnosis
- States and Sequences
 - Sequential Machines
 - Reachability
 - Controllability

One example of the applications and opportunities

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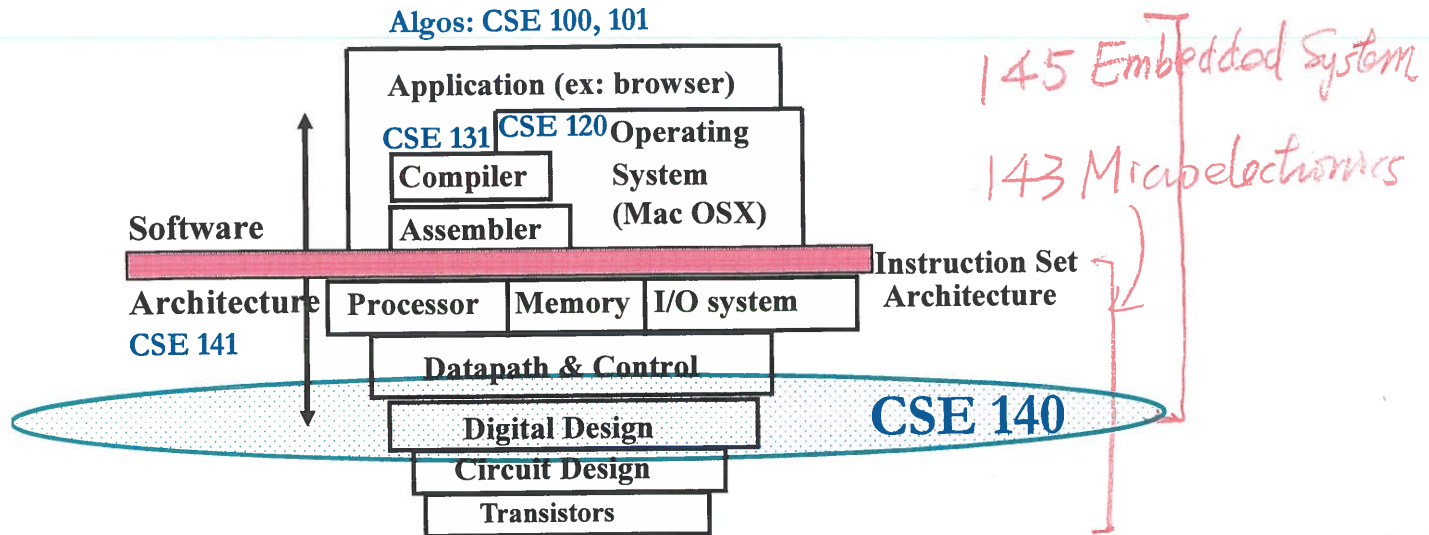
Scope

The purpose of this course is that we:

- Learn the principles of digital design
- Learn to systematically debug increasingly complex designs
- Design and build digital systems
- Learn what's under the hood of an electronic component
- Prepare for the future technology revolution

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Position among CSE Courses

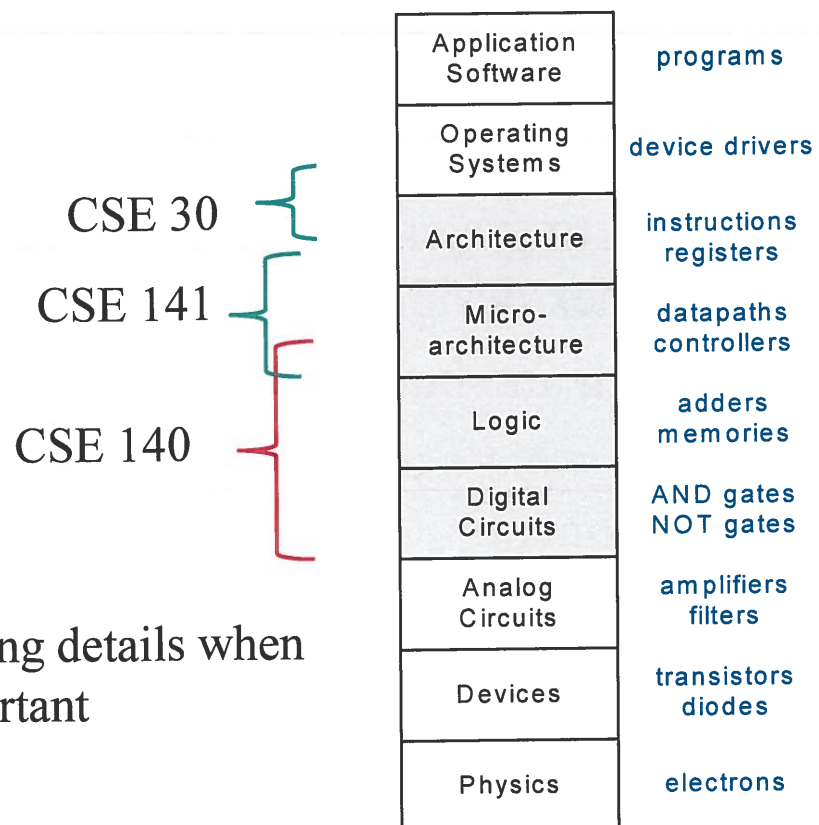


- Big idea: Coordination of many *levels of abstraction*

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Dan Garcia®

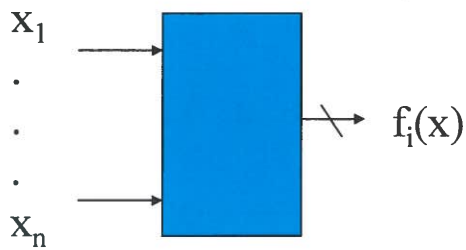
Principle of Abstraction



Abstraction: Hiding details when they are not important

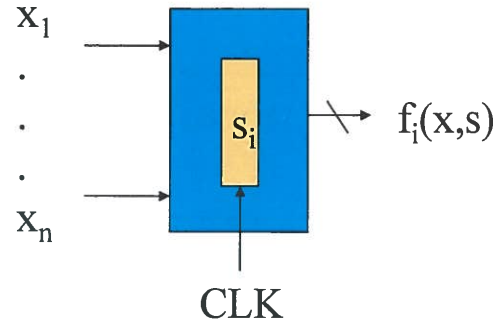
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Combinational Logic vs Sequential Network



Combinational logic:

$$y_i = f_i(x_1, \dots, x_n)$$



Sequential Networks

1. Memory
2. Time Steps (Clock)

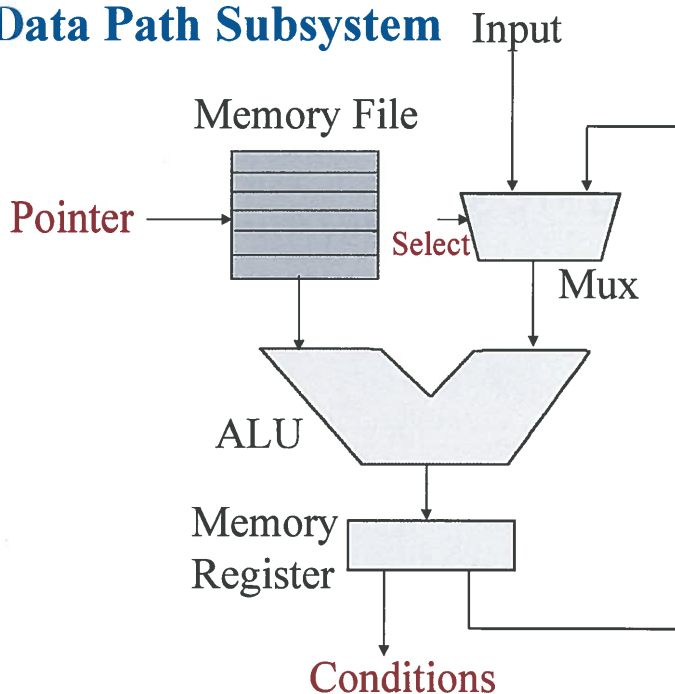
$$y_i^t = f_i(x_1^t, \dots, x_n^t, s_1^t, \dots, s_m^t)$$

$$s_i^{t+1} = g_i(x_1^t, \dots, x_n^t, s_1^t, \dots, s_m^t)$$

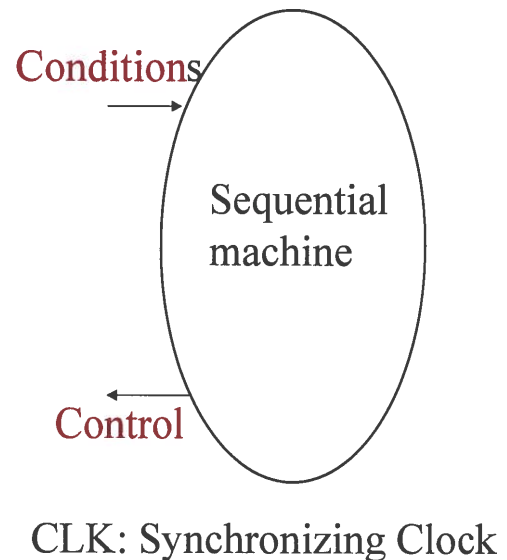
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Scope: Overall Picture of CS140

Data Path Subsystem



Control Subsystem



Scope

Subjects	Building Blocks	Theory
Combinational Logic	AND, OR, NOT, XOR	Boolean Algebra
Sequential Network	AND, OR, NOT, FF <i>Flip-Flop</i>	Finite State Machine
Standard Modules	Operators, Interconnects, Memory	Arithmetics, Universal Logic
System Design	Data Paths, Control Paths	Methodologies

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Combinational Logic Basics