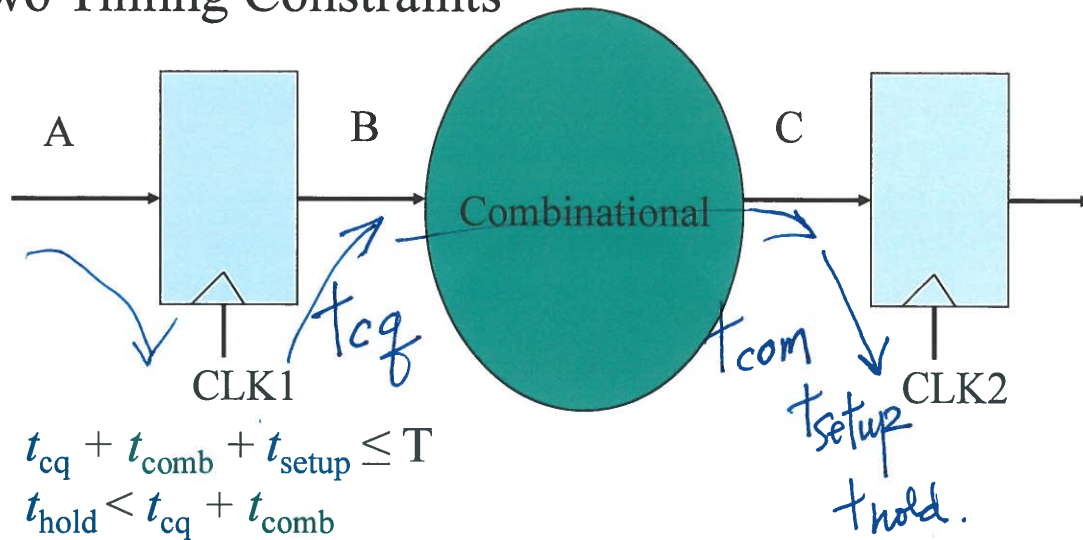


## Two Timing Constraints



$t_{cq}$ : time from rising edge of clock to Q update (CLK1  $\Rightarrow$  B)

$t_{comb}$ : time of combinational logic delay (B  $\Rightarrow$  C)

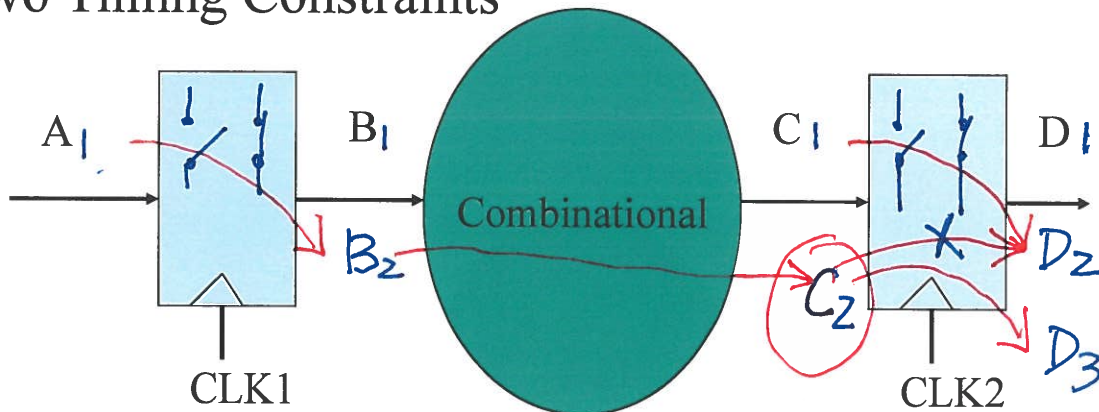
$t_{setup}$ : setup time before rising edge of clock (C  $\Rightarrow$  CLK2)

$t_{hold}$ : hold time after the rising edge of clock

T: clock period (CLK1  $\Rightarrow$  CLK2)

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## Two Timing Constraints



*Setup time constraint*      Longest delay from CLK1 to CLK2

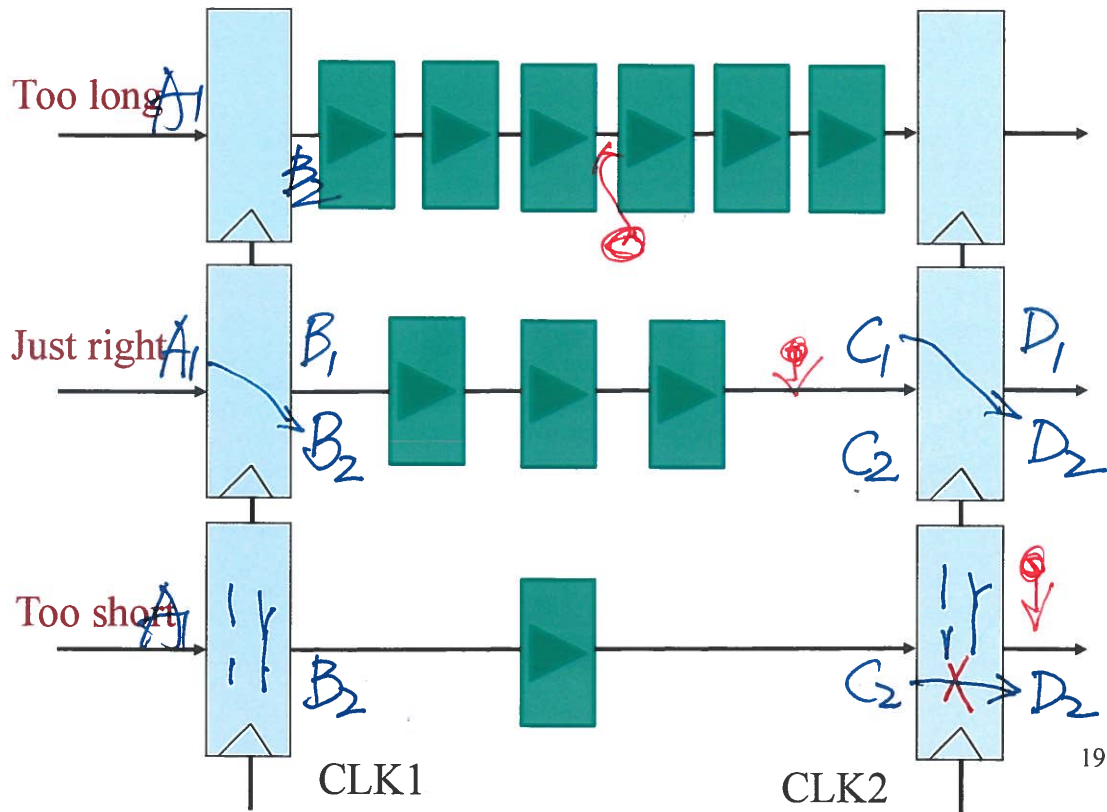
$$t_{cq} + t_{comb} + t_{setup} \leq T \quad \Longrightarrow \quad \max(t_{cq} + t_{comb} + t_{setup}) \leq T$$

*Hold time constraint*      Shortest delay from CLK1 to CLK2

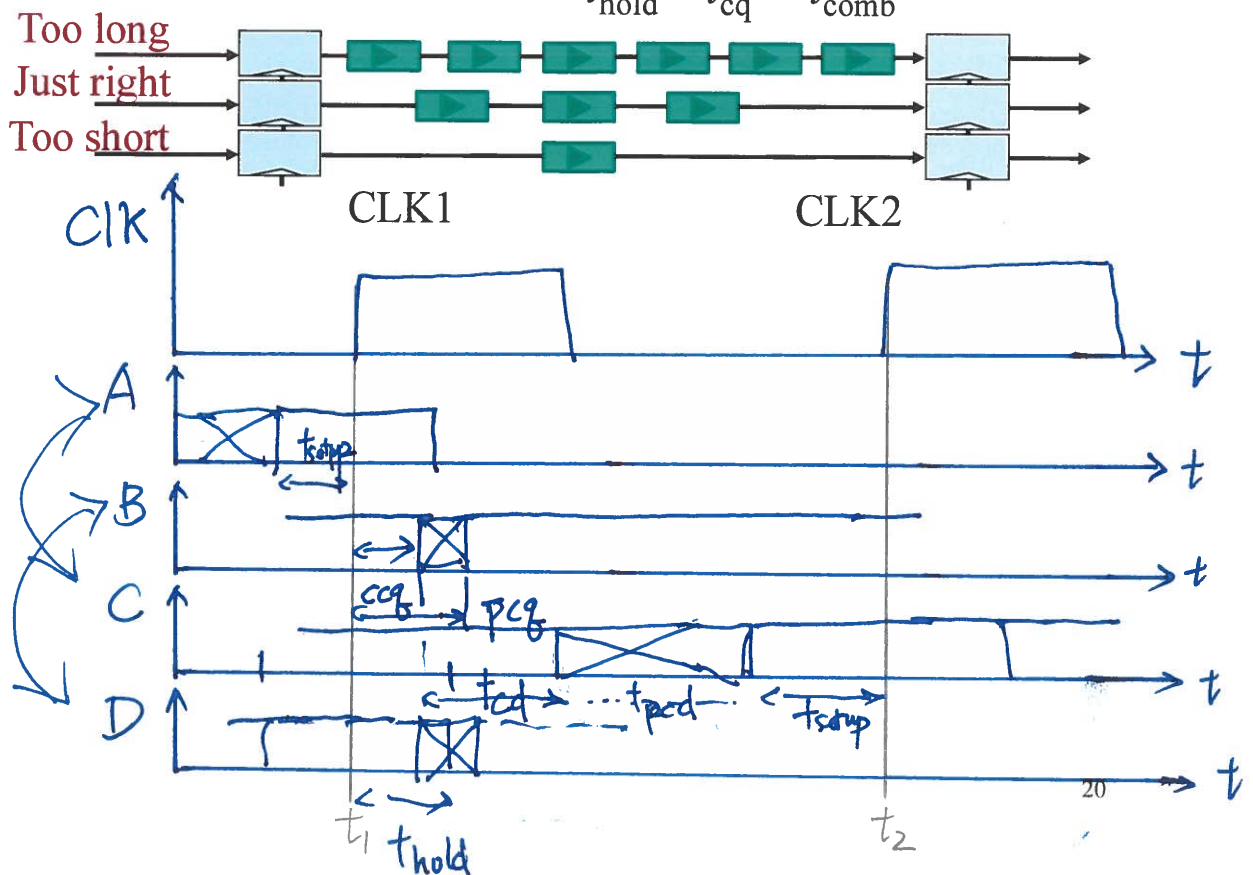
$$t_{hold} < t_{cq} + t_{comb} \quad \Longrightarrow \quad t_{hold} < \min(t_{cq} + t_{comb})$$

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Two Timing Constraints  $t_{cq} + t_{comb} + t_{setup} \leq T$   
 $t_{hold} < t_{cq} + t_{comb}$

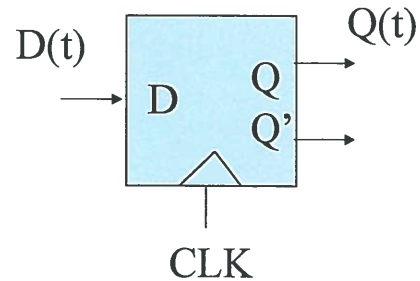


Two Timing Constraints  $t_{cq} + t_{comb} + t_{setup} \leq T$   
 $t_{hold} < t_{cq} + t_{comb}$



**Example:** The timing of which of the following signals can cause a setup-time violation?

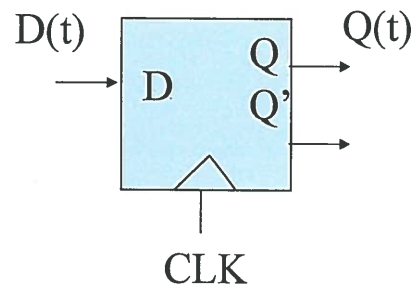
- A. Signal D arrives too early
- B. Signal D arrives too late
- C. Clock CLK arrives too late
- D. Output Q(t) responds too early
- E. None of the above



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**Example:** A hold time violation is likely to occur when

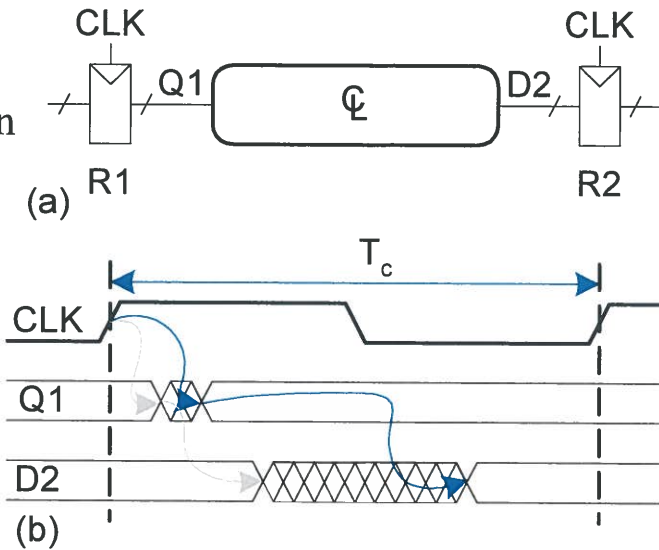
- A. Signal D changes too early
- B. Signal D changes too late
- C. Clock CLK arrives too early
- D. Clock CLK arrives too late



22

PI Q: Suppose CLK rises at  $t_1$ , what is the maximum delay (from  $t_1$ ) after which D2 reaches a stable value?

- A. Setup time of R1 +  
Propagation delay of CL +  
Propagation delay of R2
- B. Hold time of R1 + Propagation  
delay of CL + setup time of  
R1
- C. Propagation delay of R1 +  
Propagation delay of CL +  
Propagation delay of R2
- D. Propagation delay of R1 +  
Propagation delay of CL
- E. Propagation delay of CL +  
Propagation delay of R2



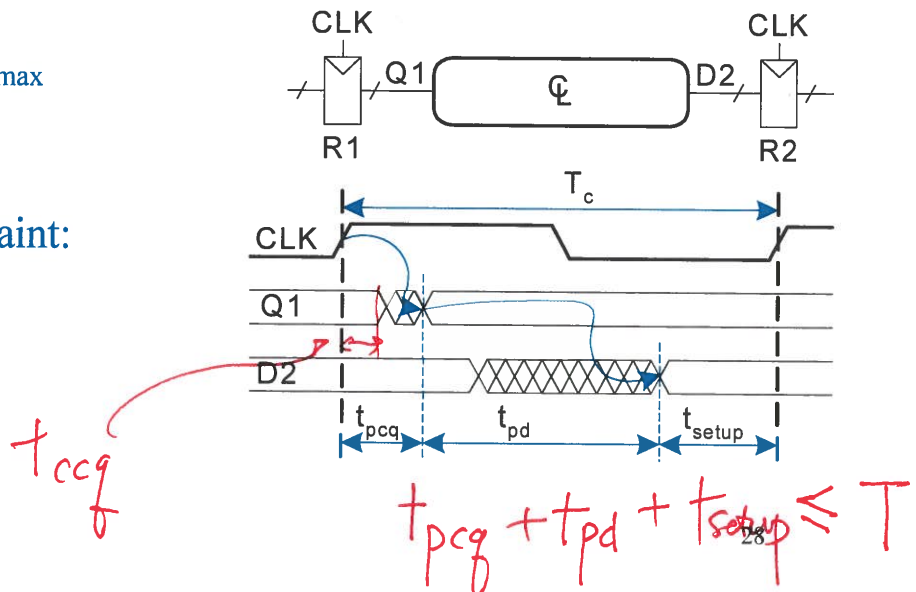
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## Setup Time Constraint

- The setup time constraint depends on the **maximum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable at least  $t_{\text{setup}}$  before the clock edge.

Maximum delay,  $t_{\text{max}}$   
=

Setup Time Constraint:

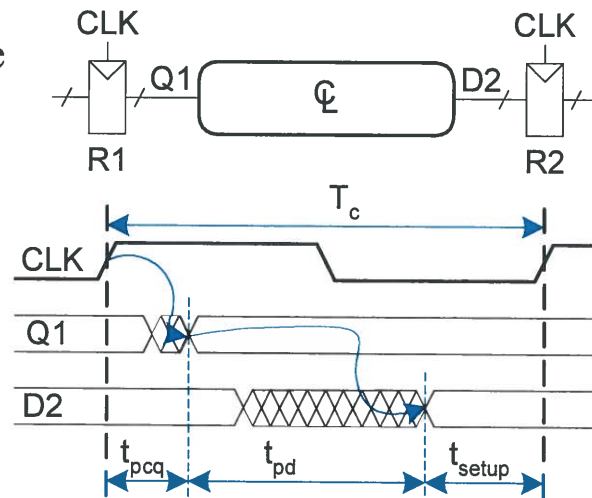


# Setup Time Constraint

$$T \geq t_{pcq} + t_{pd} + t_{setup}$$

PI Q: As a designer, which of the following parameters would you modify to meet the set up time constraint?

- A. The clock period,  $T$
- B. The prop. delay of R1,  $t_{pcq}$
- C. The prop. delay of CL,  $t_{pd}$
- D. The setup time of R2,  $t_{setup}$
- E. All of the above



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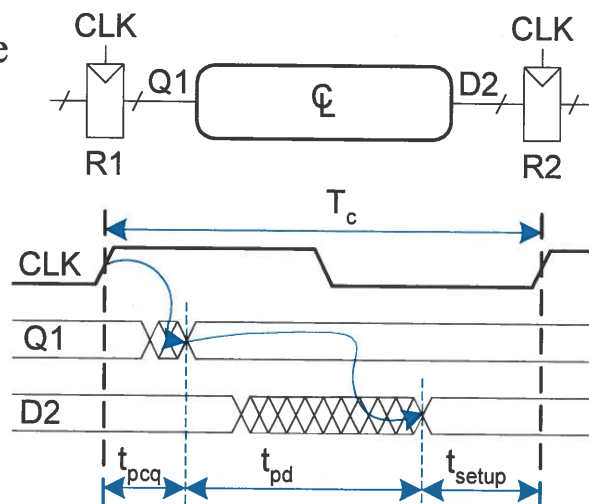
# Setup Time Constraint

$$T \geq t_{pcq} + t_{pd} + t_{setup}$$

$$t_{pd} \leq T - (t_{pcq} + t_{setup})$$

PI Q: As a designer, which of the following parameters would you modify to meet the set up time constraint?

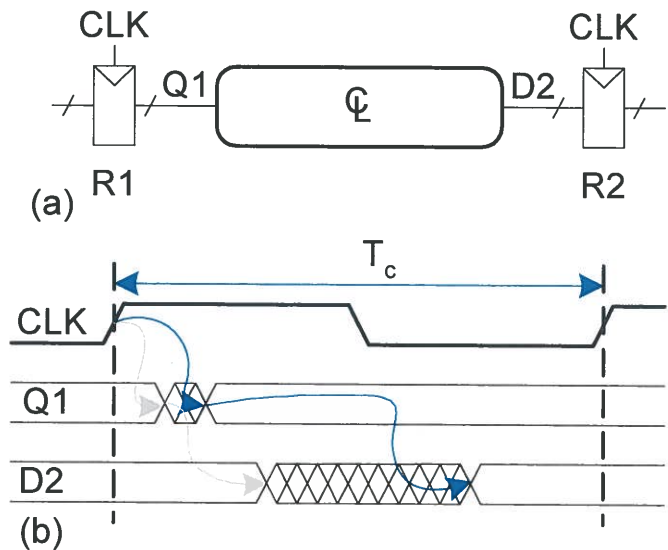
- A. The clock period,  $T$
- B. The prop. delay of R1,  $t_{pcq}$
- C. The prop. delay of CL,  $t_{pd}$
- D. The setup time of R2,  $t_{setup}$
- E. All of the above



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PI Q: Suppose CLK rises at  $t_1$ , what is the minimum delay (from  $t_1$ ) after which D2 starts to change?

- A. Setup time of R1 + propagation delay of CL + propagation of R2
- B. Hold time of R1 + propagation time of CL + setup time of R1
- C. Hold time of R1 + Contamination delay of CL + Propagation time of R2
- D. Contamination delay of R1 + Contamination delay of CL
- E. Contamination delay of CL + Contamination delay of R2



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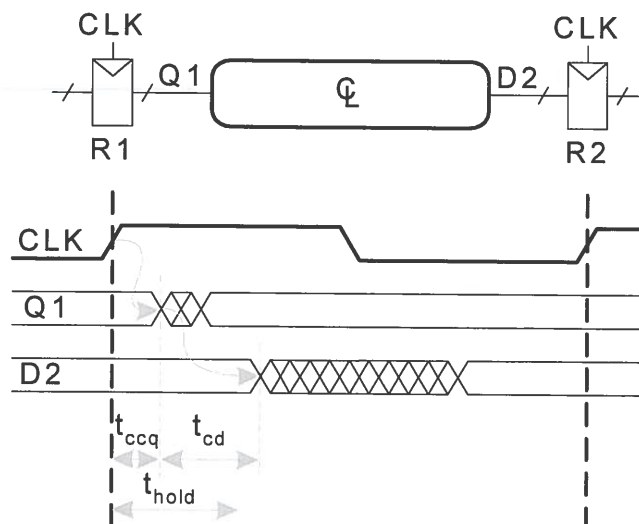
## Hold Time Constraint

- The hold time constraint depends on the **minimum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable for at least  $t_{hold}$  after the clock edge.

Minimum delay,  $t_{min}$

=

Hold Time Constraint:

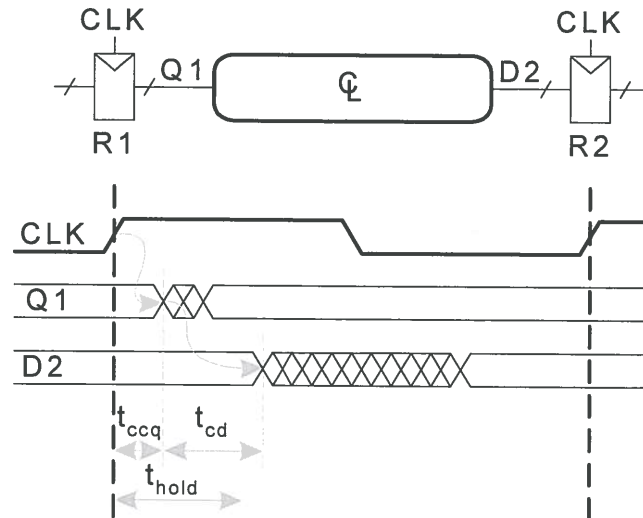


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# Hold Time Constraint

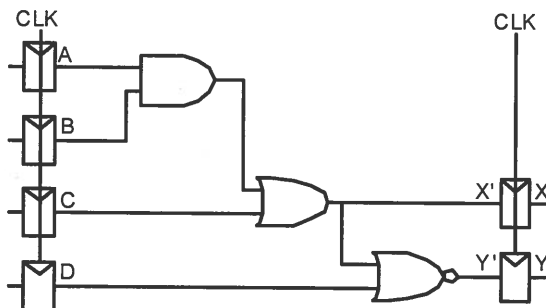
$$t_{\text{hold}} < t_{\text{ccq}} + t_{\text{cd}}$$

$$t_{\text{cd}} > t_{\text{hold}} - t_{\text{ccq}}$$



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## Timing Analysis: Example



### Timing Characteristics

$$FFs \quad t_{\text{ccq}} = 30 \text{ ps}$$

$$t_{\text{pcq}} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$Gates \quad t_{\text{pd}}(g) = 35 \text{ ps}$$

$$t_{\text{cd}}(g) = 25 \text{ ps}$$

$$t_{\text{pd}}(\text{com}) = 3 \times t_{\text{pd}}(g) = 3 \times 35 = 105 \text{ ps}$$

$$t_{\text{cd}}(\text{com}) = 1 \times t_{\text{cd}}(g) = 1 \times 25 = 25 \text{ ps}$$

Setup time constraint: Hold time constraint:

$$T_c \geq t_{\text{pcq}} + t_{\text{pd}}(\text{com}) + t_{\text{setup}} \quad t_{\text{ccq}} + t_{\text{cd}}(\text{com}) > t_{\text{hold}} ?$$

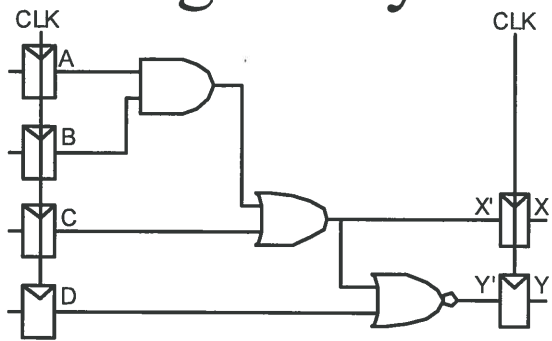
$$f_c = 1/T_c =$$

$$= 50 + 105 + 60$$

$$= 215 \text{ ps}$$

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# Timing Analysis: Example



$$t_{pd}(\text{com}) = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd}(\text{com}) = 25 \text{ ps}$$

Setup time constraint:

$$T \geq t_{pcq} + t_{pd}(\text{com}) + t_{\text{setup}}$$

$$= 50 + 105 + 60 = 215 \text{ ps}$$

$$f_c = 1/T_c = 4.65 \text{ GHz}$$

$10^9$

$$\text{FFs } t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$\text{Gates } t_{pd}(g) = 35 \text{ ps}$$

$$t_{cd}(g) = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} ?$$

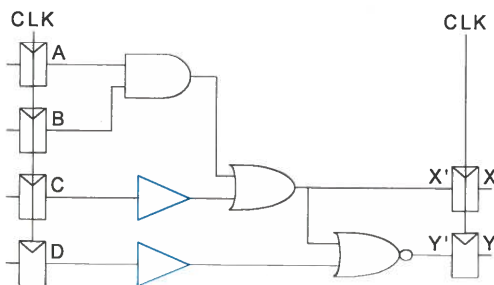
$$(30 + 25) \text{ ps} > 70 \text{ ps} ?$$

No!

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## Example: Fix Hold Time Violation

Add buffers to the short paths:



$$t_{pd}(\text{com}) =$$

$$t_{cd}(\text{com}) = 2 \times t_{cd}(g) = 2 \times 25 = 50 \text{ ps}$$

Setup time constraint:

$$T \geq$$

$$f_c =$$

Timing Characteristics

$$\text{FFs } t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$\text{Gates } t_{pd}(g) = 35 \text{ ps}$$

$$t_{cd}(g) = 25 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} ?$$

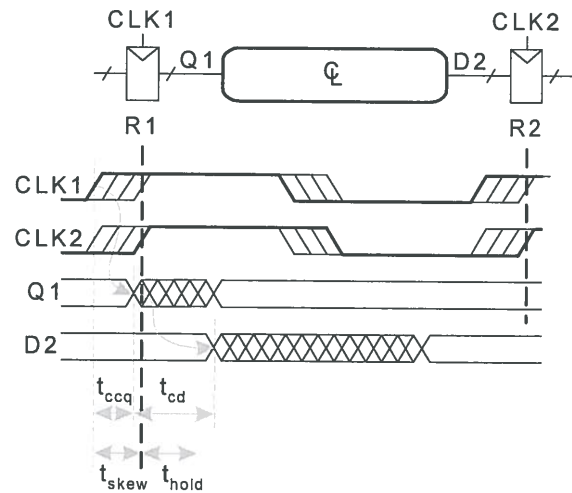
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# Time Constraint with Clock Skew: Example

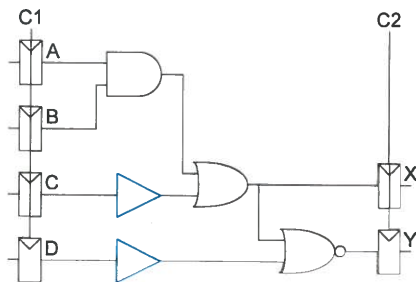
- In the worst case for hold time, CLK2 is later than CLK1

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} + t_{\text{skew}}$$



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## Clock Skew: Example



$$t_{pd}(\text{com}) = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd}(\text{com}) = 2 \times 25 \text{ ps} = 50 \text{ ps}$$

Hold time constraint:

$$t_{ccq} + t_{cd}(\text{com}) > t_{\text{hold}} + t_{\text{skew}}?$$

$$(30 + 50) > (70 + 50) \text{ ps} ?$$

### Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{\text{setup}} = 60 \text{ ps}$$

$$t_{\text{hold}} = 70 \text{ ps}$$

$$t_{pd}(\text{g}) = 35 \text{ ps}$$

$$t_{cd}(\text{g}) = 25 \text{ ps}$$

$$t_{\text{skew}} = 50 \text{ ps}$$

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# Time Constraint with Clock Skew (Noise)

In the worst case, the CLK2 is:

- Earlier than CLK1 for setup time

- Later than CLK1 for hold time.

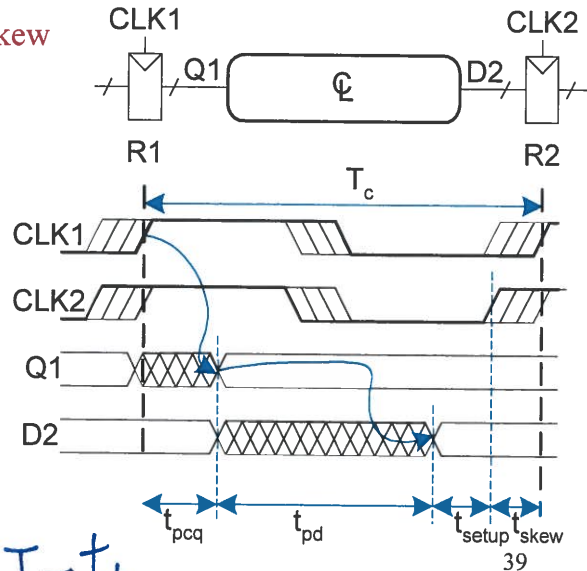
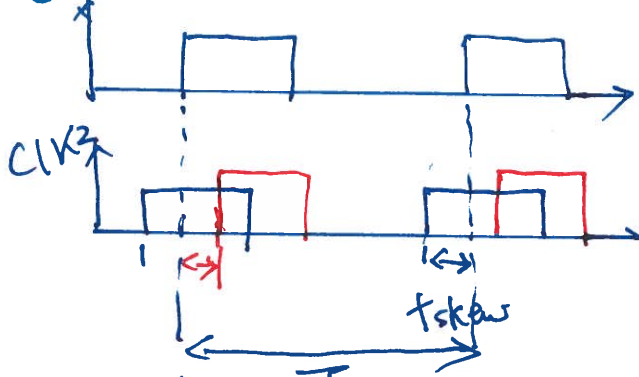
$$t_{CLK2} = t_{CLK1} \pm t_{skew}$$

$$t_{CLK2} = t_{CLK1} - t_{skew}$$

$$t_{CLK2} = t_{CLK1} + t_{skew}$$

$$1. T_c \geq t_{pcq} + t_{pd}(com) + t_{setup} + t_{skew}$$

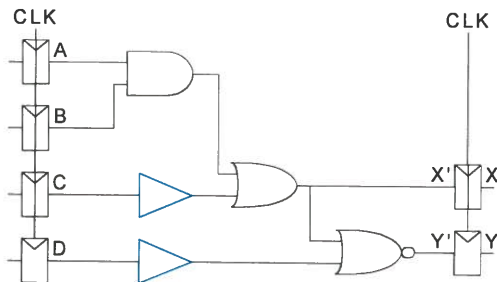
$$2. t_{ccq} + t_{cd}(com) > t_{hold} + t_{skew}$$



$$①. t_{pcq} + t_{pd}(comb) + t_{setup} \leq T - t_{skew}$$

$$②. t_{ccq} + t_{cd}(comb) > t_{hold} + t_{skew}$$

## Timing Analysis with Clock Skew: Example



$$t_{pd} = 3 \times 35 \text{ ps} = 105 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

Setup time constraint:

$$T_c \geq 225 \text{ ps}$$

$$f_c = 1/T_c = 4.44 \text{ GHz}$$

Without skew we got  $f_c = 4.65 \text{ GHz}$

## Timing Characteristics

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{setup} = 60 \text{ ps}$$

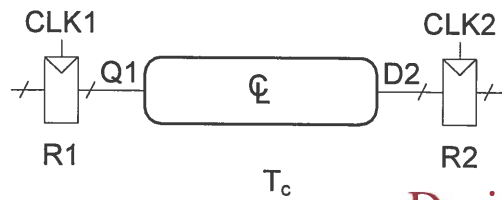
$$t_{hold} = 70 \text{ ps}$$

$$t_{pd} = 35 \text{ ps}$$

$$t_{cd} = 25 \text{ ps}$$

$$t_{skew} = 10 \text{ ps}$$

# Retiming with Designated Skew



Skew as noise (worst case)

Designated skew

$$t_{CLK2} = t_{CLK1} \pm t_{skew}$$

$$t_{CLK2} = t_{CLK1} + t_{skew}$$

$$T \geq t_{pcq} + t_{pd}(\text{com}) + t_{setup} + t_{skew} \quad T \geq t_{pcq} + t_{pd}(\text{com}) + t_{setup} - t_{skew}$$

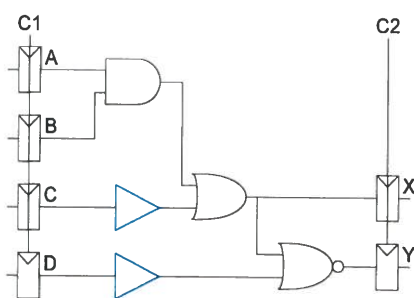
$$t_{ccq} + t_{cd}(\text{com}) > t_{hold} + t_{skew}$$

$$t_{ccq} + t_{cd}(\text{com}) > t_{hold} + t_{skew}$$

Linear Programming Obj: min T.

const: longest path<sub>ij</sub> ≤ T - t<sub>skew</sub><sub>ij</sub>

shortest path<sub>ij</sub> ≥ t<sub>hold</sub> + t<sub>skew</sub><sub>ij</sub>



Retiming: Example

$$t_{ccq} = 30 \text{ ps}$$

$$t_{pcq} = 50 \text{ ps}$$

$$t_{setup} = 60 \text{ ps}$$

$$t_{hold} = 70 \text{ ps}$$

$$t_{pd}(g) = 35 \text{ ps}$$

$$T_c \geq t_{pcq} + t_{pd}(\text{com}) + t_{setup} - t_{skew}$$

$$t_{ccq} + t_{cd}(\text{com}) \geq t_{hold} + t_{skew}$$

$$\begin{cases} T_c \geq 50 + 105 + 60 - t_{skew} \\ 30 + 50 \geq 70 + t_{skew} \end{cases} \quad \begin{cases} T_c \geq 215 - t_{skew} \\ 80 \geq 70 + t_{skew} \end{cases} \quad \begin{cases} t_{cd}(g) = 25 \text{ ps} \\ t_{cd}(g) = 25 \text{ ps} \end{cases}$$

$$\boxed{20 \text{ ps}}$$

Example: The minimum clock period T can be:

A. 195

B. 205

C. 215

D. None of the above

$$\begin{cases} T_c \geq 215 - t_{skew} \\ 10 \geq t_{skew} \end{cases}$$

$$t_{cd}(\text{comb}) = 40 \text{ ps} \quad (2 \times t_{cd}(g))$$

$$t_{ccq} + t_{cd}(\text{comb}) > t_{hold} + t_{skew} \\ 30 + 40 + t_{skew} > 70 + t_{skew}$$

# Timing and Retiming

- Retiming: Adjust the clock skew so that the clock period can be reduced.
- Add a few more examples on timing and retiming.

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## Conclusion

- Clock to Clock: Range of shortest and longest paths
- Design revision and retiming to adjust the constraints
- Research: Variation aware designs

Extra materials:

- C. Leiserson and J. Saxe, "Retiming Synchronous Circuitry," *Algorithmica*, pp. 6:5-35, 1991.
- L.T. Liu, M. Shih, N.C. Chou, C.K. Cheng, and W. Ku, "Performance-Driven Partitioning Using Retiming and Replication," *IEEE Int. Conf. on Computer-Aided Design*, pp. 296-299, Nov. 1993.

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