

Outlines

- Staff
 - Instructor, TAs, Tutors
- Logistics
 - Websites, Textbooks, Grading Policy
- Motivation *Chapter 1*
 - Moore's Law, Deep Learning, Quantum Computing
- Scope
 - Position among CSE courses
 - Coverage

2

Lecture 1: Introduction to Digital Logic Design

CSE 140: Components and Design Techniques for Digital Systems

Spring 2021

CK Cheng

Dept. of Computer Science and Engineering
University of California, San Diego

1. Historical event
2. Digit
3. Complexity
10 variables $2^{10} = 10^3$
1000 " $2^{1000} \approx 10^{300}$
Finger $\rightarrow 0-9 \rightarrow 0,1$ Binary
10⁷⁸ 10⁸² atoms

1

*Hardware
Design*

Staff: the Instructor

- Instructor: CK Cheng
- Education: Ph.D. in EECS UC Berkeley
- Industrial Experiences: Engineer of AMD, Mentor Graphics, Bellcore; Consultant for technology companies
- Email: ckcheng+140@ucsd.edu
- Office: Room 2130 CSE Building
- Office hours
 - 3:00-4:00PM Monday; 2:00-3:00PM Wednesday
- Websites
 - <http://cseweb.ucsd.edu/~kuan>
 - <http://cseweb.ucsd.edu/classes/sp21/cse140-a>

3

Staff: TAs and Tutors

TAs

- Abraham, Elizabeth, email: eabraham@ucsd.edu
- Holtz, Chester, email: chholtz@ucsd.edu
- Hsu, Po-Ya, email: p8hsu@ucsd.edu
- Ravindrakumar, Vaishakh, email: varavind@ucsd.edu
- Wu, (Connie) Yen-Yi, email: yew001@ucsd.edu

Tutor(s)

- Jang, (Tim) Wonsuk, email: wljang@ucsd.edu
- Serrano, Evan, email: eserran@ucsd.edu

Office hours will be posted on the course website (piazza)

4

Logistics: Class Schedule

- Lecture: TR 12:30-1:50PM
- Discussion: F 3-350PM
- 5-6 Homework Assignments, 3 Exams
- The Third Exam: Due time M 230PM, 6/7/2021

5

Logistics: Textbooks

Reserved at library

- Digital Design and Computer Architecture by David Money Harris and Sarah L. Harris, Morgan Kaufmann (Reading Activities)
- Digital Systems and Hardware/Firmware Algorithms, Milos D. Ercegovic and Tomas Lang (System Designs, pdf file will be released)

6

Logistics: Sites for the Class

- Class website
 - <http://cseweb.ucsd.edu/classes/sp21/cse140-a/index.html>
 - Index: Staff Contacts and Office Hrs
 - Syllabus
 - Grading policy
 - Class notes
 - Assignment: Homework and Reading Activities
 - Exercises: Solutions and Rubrics
- Forum (Piazza): Online Discussion *make sure you have access
- Score keepers: Gradescope, Canvas

7

Logistic: Class Expectation

- Level 1: Concepts and Methods (Lecture and slides)
 - Class attendance of video record
- Level 2: Hands on Practices (Exercises)
 - Homework
- Level 3: Command of Materials (Samples of exams)
 - Exams: Type 1
- Level 4: Extension and Exploration (Content beyond the textbook)
 - Exams: Type 2

8

Logistics: Grading

Grade on style, completeness and correctness

- Homework: 25pts (grade based on a subset of problems)
- Exam 1: 25pts Week 4
- Exam 2: 25pts Week 7
- Exam 3: 25pts (due 230PM, Monday 6/7/2021)
- Grading: The better choice of the following two categories
 - Exact score (100pts)
 - A>93, A- >90, B+>87, B>83, B->80, C+>77, C>73
 - C- >50.
 - The curve (100% of class)
 - A+ top x% ($x < 5$)
 - (A,A-) top $33 \pm \epsilon\%$; (B+,B,B-) top $66 \pm 2\epsilon\%$

Handwritten notes: 25pts, 25pts, 25pts are circled. A bracket groups Exam 1, 2, and 3 with the number 35. An arrow points from 35 to the text "32.5 for 2 exams". The phrase "the best" is written next to Exam 3.

9

Logistic: grading components

- Homework:
 - Due Monday night on gradescope
 - Group discussion is encouraged. However, we are required to write individually
 - Discount 10% loss of credit for each day after the deadline but no credit **after the solution is posted.**
 - Some parts will be graded by completion only
 - **Standard: Posted solutions and rubrics**

10

Logistic: 3 Exams

Exams: Asynchronous exam taken within 48 hours

- Open book, notes, free to check websites
- Solution and grading policy will be posted after the exam.
- Exams are not cumulative but requires a good command of the previous exam content
- Two timeframe options for the class to decide
 - I. 80 minutes time frame: Finish the exam in 80 minutes after you start the exam.
 - II. 48 hours time frame: Deliver the result in 48 hours after the exam is posted.
- Exam schedule
 - I. Weekends
 - II. Weekdays

11

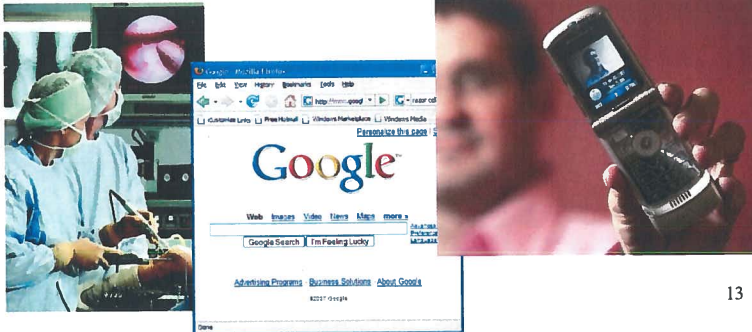
Course Problems...Cheating

- What is cheating?
 - Studying together in groups is not cheating but encouraged
 - Turned-in work must be *completely* your own.
 - Copying someone else's solution on a HW or Exam is cheating
 - Both "giver" and "receiver" are equally culpable
- We will be better off to work on the problem alone during the exam.
- We have to address the issue once the cheating is reported by someone (e.g. TA, Tutor, Student, etc.).

12

Motivation

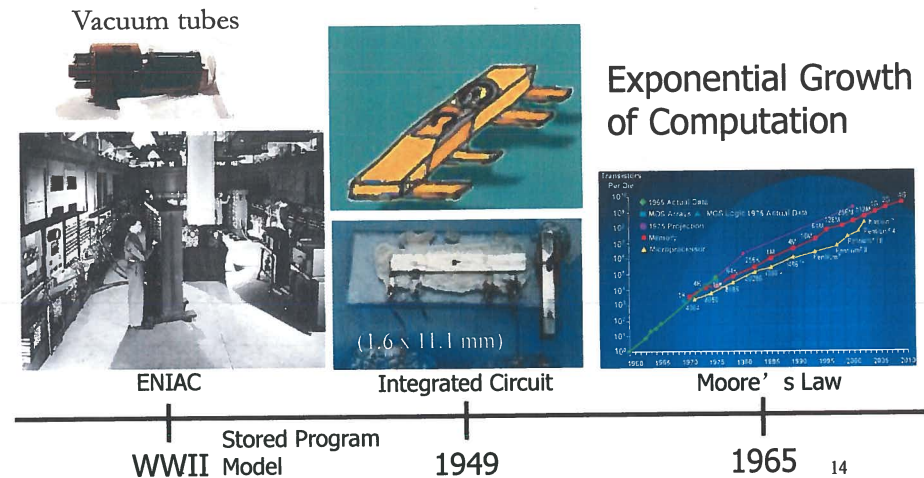
- Microelectronic technologies have revolutionized our world: cell phones, internet, rapid advances in medicine, etc.
- The semiconductor industry has grown from \$21 billions in 1985, \$335 billions in 2015, to \$478 billions in 2018.



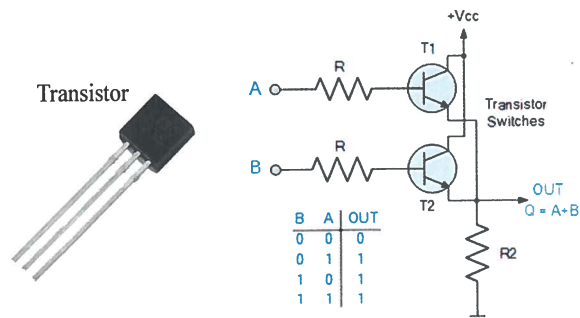
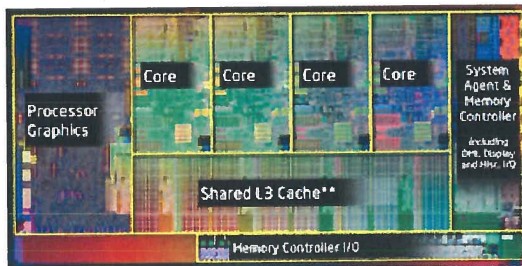
13

The Digital Revolution

Integrated Circuit: Many digital operations on the same material



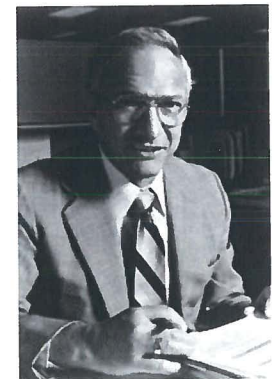
Building complex circuits



15

Robert Noyce, 1927 - 1990

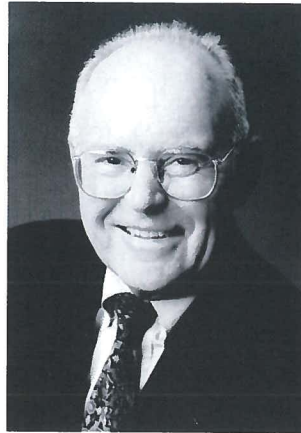
- Nicknamed "Mayor of Silicon Valley"
- Cofounded Fairchild Semiconductor in 1957
- Cofounded Intel in 1968
- Co-invented the integrated circuit



16

Gordon Moore

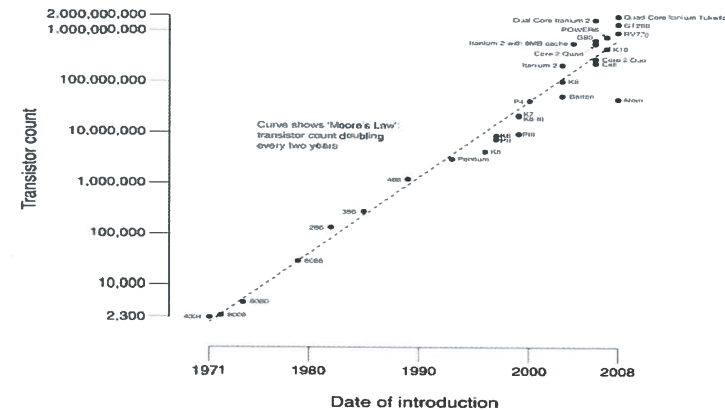
- Cofounded Intel in 1968 with Robert Noyce.
- **Moore's Law:** the number of transistors on a computer chip doubles every 1.5 years (observed in 1965)



17

Technology Trends: Moore's Law

CPU Transistor Counts 1971-2008 & Moore's Law



- Since 1975, transistor counts have doubled every two years.
- **Moore's law: wider applications: larger market: higher revenue: more R&D**

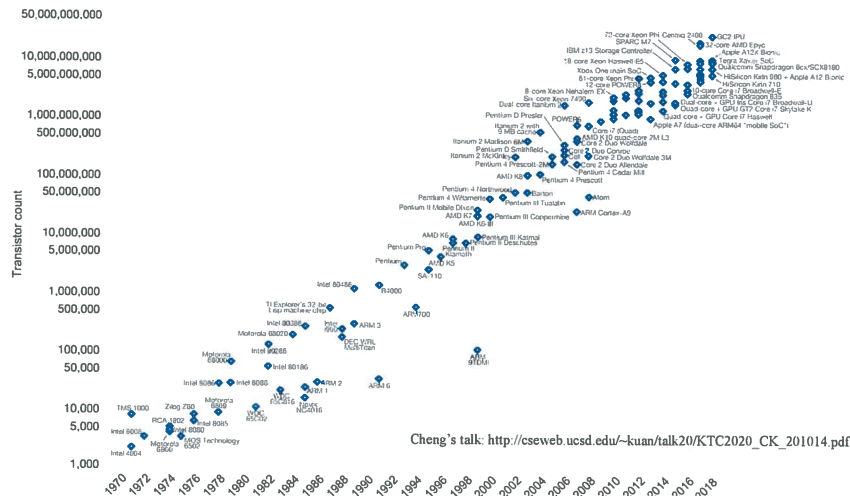
18

Introduction: Moore in 1965

The complexity for minimum component costs has increased at a rate of roughly a factor of two/yr.

Moore's Law – The number of transistors on integrated circuit chips (1971-2018)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.



Cheng's talk: http://cseweb.ucsd.edu/~kuan/talk20/KTC2020_CK_201014.pdf

New Technologies

- New materials and fabrication for devices
 - Low power devices
 - Three dimensional integrated circuits
 - Graphene
- New architecture
 - Machine learning, deep learning
- Quantum computing

Understand the principles to explore the future

20

Artificial Intelligence

- Logic and Reasoning
- Boolean Satisfiability (SAT)
 - Product of sum clauses
 - Diagnosis
- States and Sequences
 - Sequential Machines
 - Reachability
 - Controllability

One example of the applications and opportunities

21

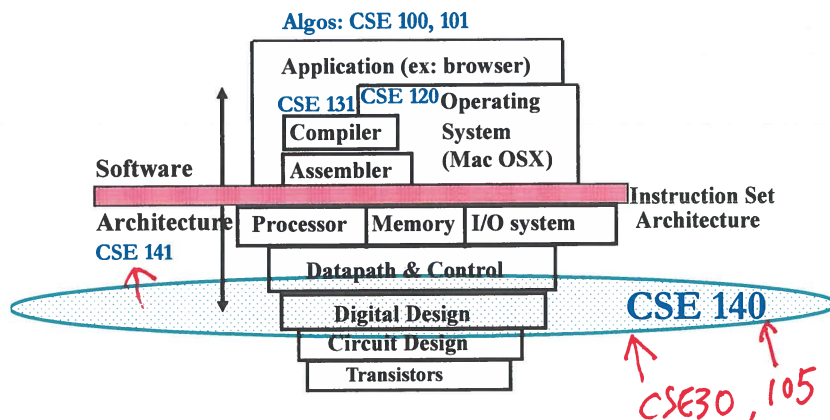
Scope

The purpose of this course is that we:

- Learn the principles of digital design
- Learn to systematically debug increasingly complex designs
- Design and build digital systems
- Learn what's under the hood of an electronic component
- Prepare for the future technology revolution

22

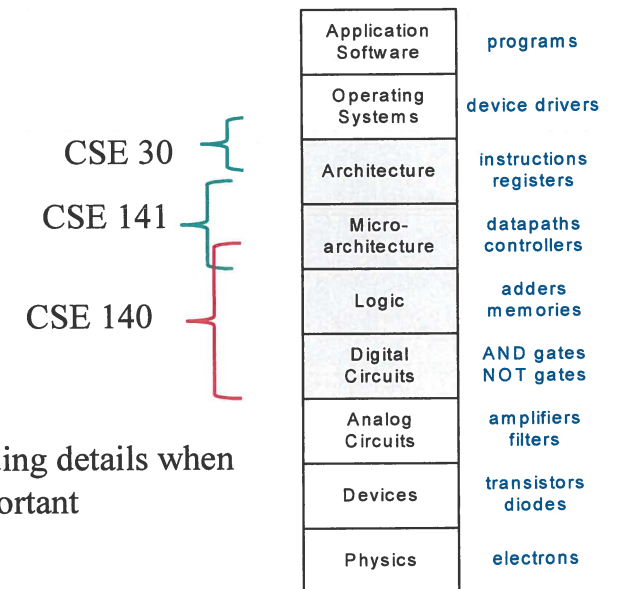
Position among CSE Courses



- Big idea: Coordination of many *levels of abstraction*

Dan Garcia©

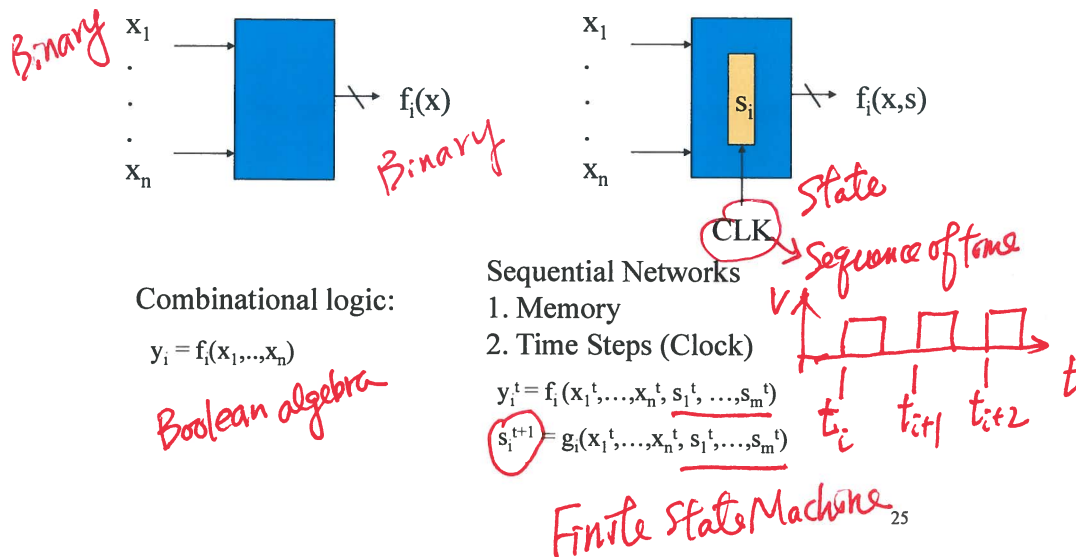
Principle of Abstraction



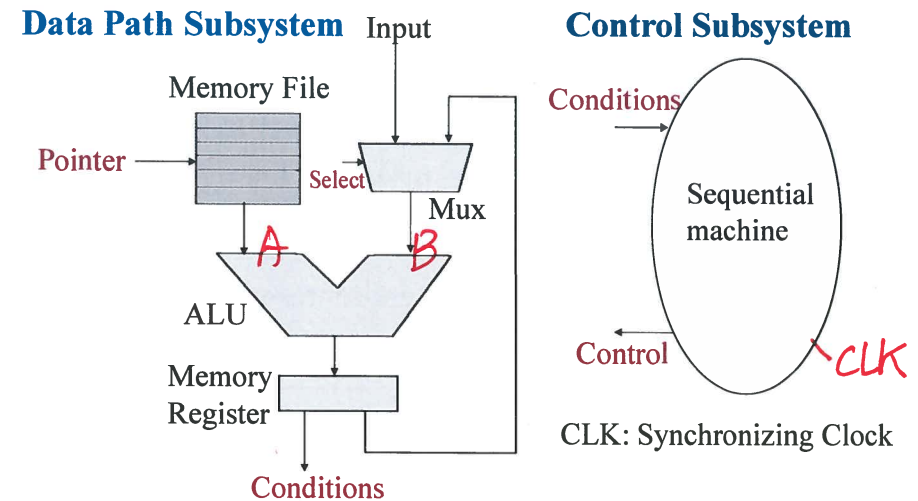
Abstraction: Hiding details when they are not important

24

Combinational Logic vs Sequential Network



Scope: Overall Picture of CS140



BSV: Design specification and modular design methodology²⁶

Scope

Subjects	Building Blocks	Theory
Combinational Logic	AND, OR, NOT, XOR	Boolean Algebra
Sequential Network	AND, OR, NOT, FF <i>Flip-Flop</i>	Finite State Machine
Standard Modules	Operators, <u>Interconnects</u> , Memory	Arithmetics, Universal Logic
System Design	Data Paths, Control Paths	Methodologies

↓
CPU ASIC

Ex 1

Ex 2

Ex 3

Combinational Logic Basics

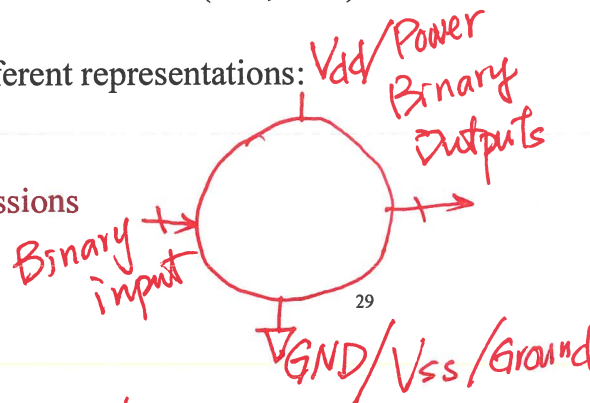
What is a combinational circuit?

Binary Digital Logic

- No memory
- Realizes one or more functions
- Inputs and outputs can only have two discrete values
 - Physical domain (usually, voltages) (Ground 0V, Vdd 1V)
 - Mathematical domain : Boolean variables (True, False)

Differentiate between different representations:

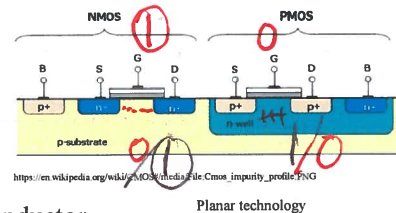
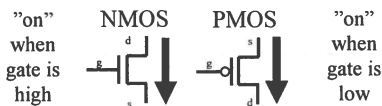
- physical circuit
- schematic diagram
- mathematical expressions



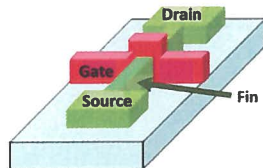
- Simplest representation is "1" and "0" (base-2).
- Choose a physical quantity to represent "1" and "0"
 - Usually voltage, but not always (e.g. current, resistance, magnetic polarization, quantum spin, ...)
- Use a transistor to make the switch (operating as a digital instead of analog device)
 - Two states – on / off
 - Signals can be high voltage ("1") or low voltage ("0")

30

Basic CMOS PMOS/NMOS



Planar technology

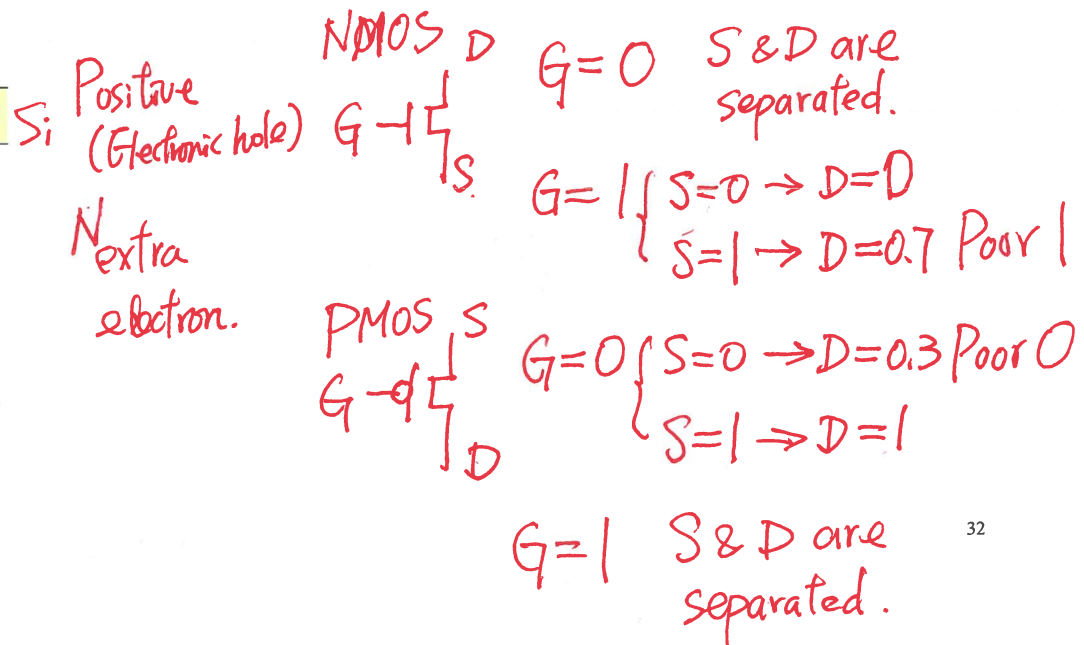


FINFET technology

- Complementary Metal Oxide Semiconductor
- Invented in the 1960's, but took over in the 80's
- "on" means low resistance, "off" means high resistance
- Logic "1" and Logic "0" values are arbitrary e.g. logic "1" == 1.0 V, logic "0" == 0.0 V

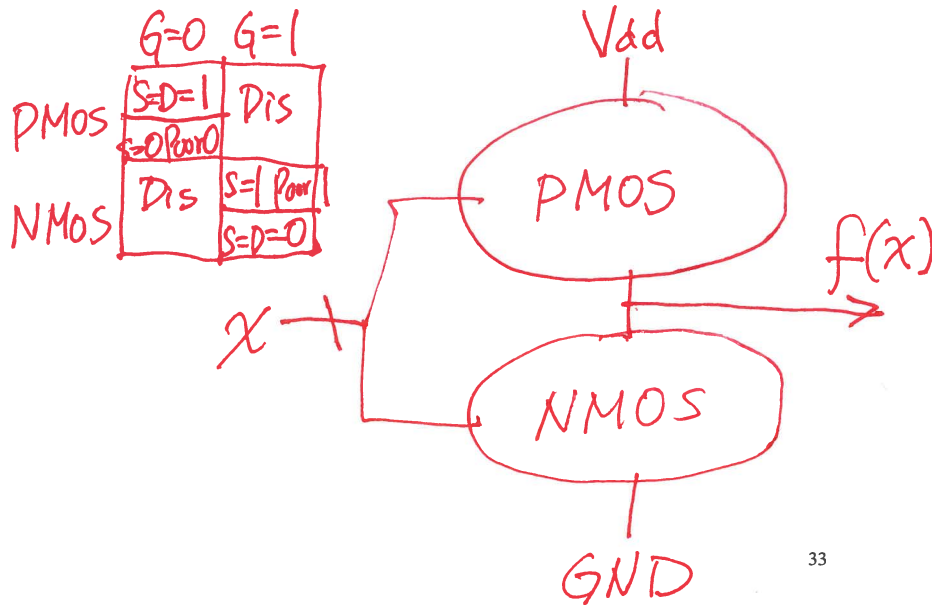
31

Transistors as Switches



32

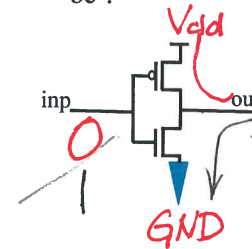
Transistors as Switches



33

The most basic CMOS gate - inverter

- When "inp" is "1", then the nmos is on and the pmos is off – output will be ?
- When "inp" is "0", then the nmos is off and the pmos is on – output will be ?



Schematic



Truth Table

in	out
0	1
1	0

Equation

out = in'
 out = $\overline{\text{in}}$

34

Basic Gates – (N)AND gate

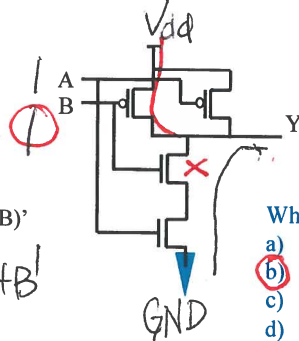
AND $Y = A \& B$, $Y = AB$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

NAND $Y = (A \& B)'$, $Y = (AB)'$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Handwritten: Schematic diagram



What kind of gate is this?

- a) AND
 b) NAND
 c) Inverter
 d) None of the above

Handwritten: $= A' + B'$

1. NMOS gates are in serial
2. PMOS gates are in parallel
3. Y is connected to either V_{dd} or GND all the time but not the both

35

Basic Gates – (N)OR gate

OR $Y = A + B$, $Y = A | B$

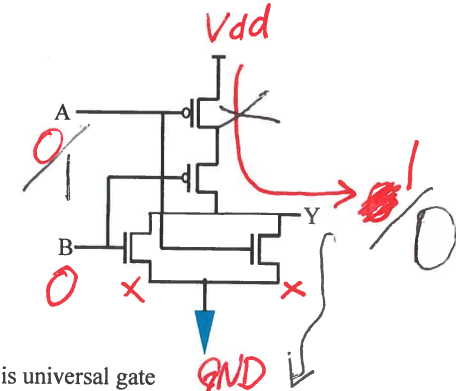
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NOR $Y = (A + B)'$, $Y = (A | B)'$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Bubble means Invert

NOR is universal gate



36

Boolean Algebra

A branch of algebra in which the values of the variables belong to a set B (e.g. $\{0, 1\}$), has two operations $\{+, \cdot\}$ that satisfy the following four sets of laws.

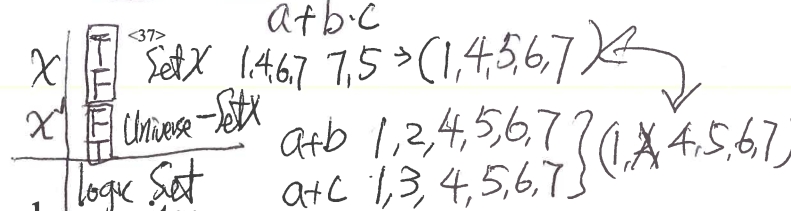
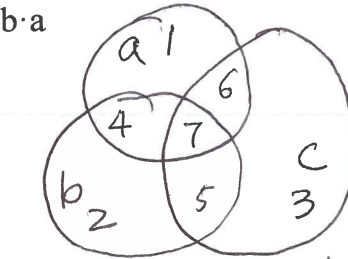
- Associative laws: $(a+b)+c = a+(b+c)$, $(a \cdot b) \cdot c = a \cdot (b \cdot c)$
- Commutative laws: $a+b = b+a$, $a \cdot b = b \cdot a$
- Distributive laws: $a+(b \cdot c) = (a+b) \cdot (a+c)$,
 $a \cdot (b+c) = a \cdot b + a \cdot c$

• Identity laws: $a+0=a$, $a \cdot 1=a$

• Complement laws: $a+a'=1$, $a \cdot a'=0$

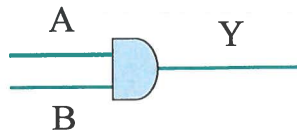
(x' : the complement element of x)

0	False	Empty	+	OR	Union
1	True	Universe	•	AND	Intersect
	Logic Set	Logic Set		Logic Set	Logic Set



Representations of combinational circuits:

The Schematic



- What is the simplest combinational circuit that you know?

Duality

- Swap $(+, \cdot)$ and complement all 0's and 1's
- If we can prove a statement using laws of Boolean algebra true, then the duality of the statement is also true.

Laws and their duals

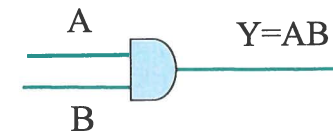
Associative	$(a \cdot b) \cdot c = a \cdot (b \cdot c)$	$(a + b) + c = a + (b + c)$
Commutative	$a \cdot b = b \cdot a$	$a + b = b + a$
Distributive*	$a \cdot (b + c) = a \cdot b + a \cdot c$	$a + (b \cdot c) = (a + b) \cdot (a + c)$
Identity	$a \cdot 1 = a$	$a + 0 = a$
Compliment	$a \cdot a' = 0$	$a + a' = 1$

Representations of combinational circuits

Truth Table: Enumeration of all combinations

Example: AND

id	A	B	Y
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	1



Boolean Algebra

Similar to regular algebra but defined on sets with only three basic 'logic' operations:

1. Intersection: AND (2-input); Operator: $\cdot$, $\&$
2. Union: OR (2-input); Operator: $+$, $|$
3. Complement: NOT (1-input); Operator: $'$, $!$

$\&$, $|$, $!$ Symbols in BSV

<41>

Some Def's

- Complement : variable with a "BAR" over it or $'$ after it
 A'
- Literal : variable or its complement
- Implicant: product of literals
 ABC
- Implicate: sum of literals
 $(A+B+C)$

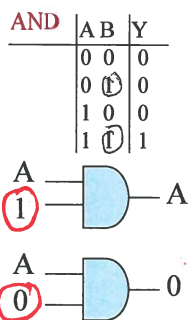
Minterm, maxterm (implicant or implicate that includes all the inputs)

$$f(A,B,C,D): ABCD, (A+B+C+D)$$

42

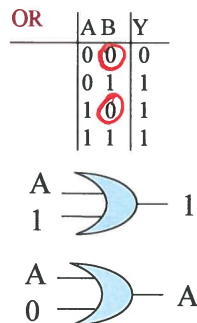
Boolean algebra and switching functions

Two-input AND ($\cdot$)



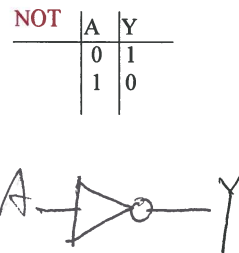
For an AND gate,
0 at input blocks the other inputs
and dominates the output
1 at input passes signal A

Two-input OR ($+$)



For an OR gate,
1 at input blocks the other inputs
and dominates the output
0 at input passes signal A

One-input NOT
(Complement, $'$)



Boolean Algebra

For two Boolean variables X and Y with X=1, Y=0,
what is function $f(X,Y)=X+Y$?

A. $f(X,Y)=0$

B. $f(X,Y)=1$

C. $f(X,Y)=2$

43

<44>

Boolean Algebra

iClicker Q: For two Boolean variables X and Y with $X=1$, $Y=0$, what is function $f(X,Y)=X+X+Y$?

- A. $f(X,Y)=0$
- B. $f(X,Y)=1$
- C. $f(X,Y)=2$

<45>

Boolean Algebra

For two Boolean variables X and Y with $X=1$, $Y=0$, what is function $f(X,Y)=X+XY$?

- A. $f(X,Y)=0$
- B. $f(X,Y)=1$
- C. $f(X,Y)=2$

<46>

Boolean Algebra

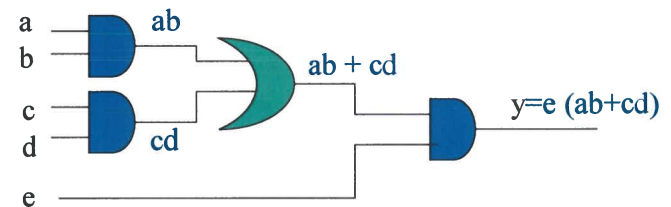
For two Boolean variables X and Y with $X=1$, $Y=0$, what is function $f(X,Y)=(X+Y)Y$?

- A. $f(X,Y)=0$
- B. $f(X,Y)=1$
- C. $f(X,Y)=2$

<47>

So, what is the point of representing gates as symbols and Boolean expressions?

- Given the Boolean expression, we can draw the circuit it represents by cascading gates (and vice versa)



Logic circuit vs. Boolean Algebra Expression

Simplify the Boolean expression: Reduce the complexity of the circuit

48

- Switching Expression –

- Equations - # literals, # variables, # operators

- Literal is a variable or its complement (e.g. a , a')

- Variables (e.g. x)

- Operator (e.g. $+$, $\cdot$)

- Schematic / Logic Diagram - # of gates, # nets (wires), # of pins

- Gate (and, or, etc) – can be more than 2 inputs (e.g. 3 input AND gate)

- Net – wire that connects gates

- Pin - input or output of a gate.

Associativity Laws

$$(A+B) + C = A + (B+C)$$



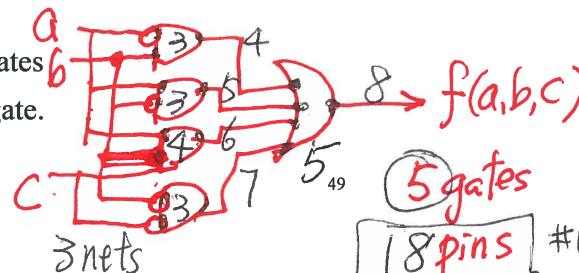
$$f(a,b,c) = a'b + ab' + abc + b'c'$$

1 2 3 4 5 6 7 8 9

3 variables
9 literals

5 operators 4 AND 1 OR

$$(AB)C = A(BC)$$



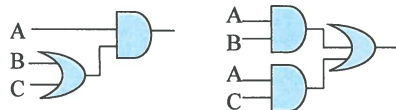
5 gates 9 + 10 - 1
18 pins #literals + 2#operators - 1
8 nets 3#variables
5 + #gates

Laws and Logic Diagrams

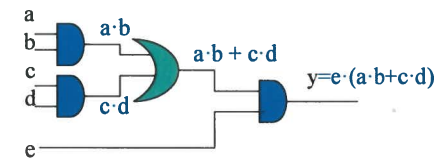
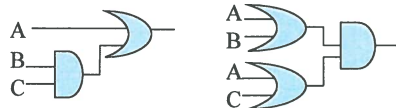
Switching Expression and Logic

Distributive Laws

$$A \cdot (B+C) = A \cdot B + A \cdot C$$



$$A+B \cdot C = (A+B) \cdot (A+C)$$



Schematic Diagram:

5 primary inputs

1 primary output

4 components (gates)

9 signal nets

12 pins

Boolean Algebra:

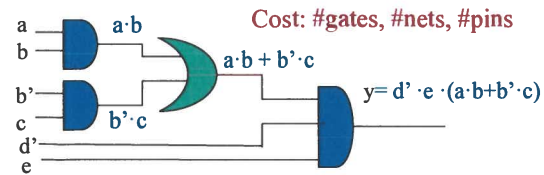
5 variables

1 expression

4 operators

5 literals

Switching Expression and Logic



Schematic Diagram:

6 primary inputs

1 primary output

4 gates (3 ANDs, 1 OR)

10 signal nets

11 pins

Nets are wires, Gates $\rightarrow$ transistors

Switching Expression:

5 variables

1 expression

4 operators (3 ANDs, 1 OR)

6 literals

Example: $f(a, b, c) = ab + a'b + a'b'$

# variables	
# literals	
# gates	

54

Which statement is not true in general?

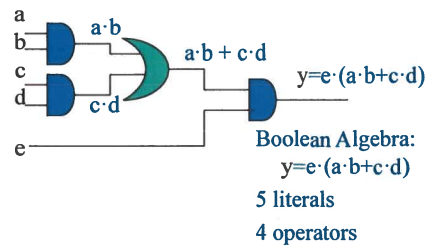
Schematic Diagram:

5 primary inputs

4 components (gates)

9 signal nets

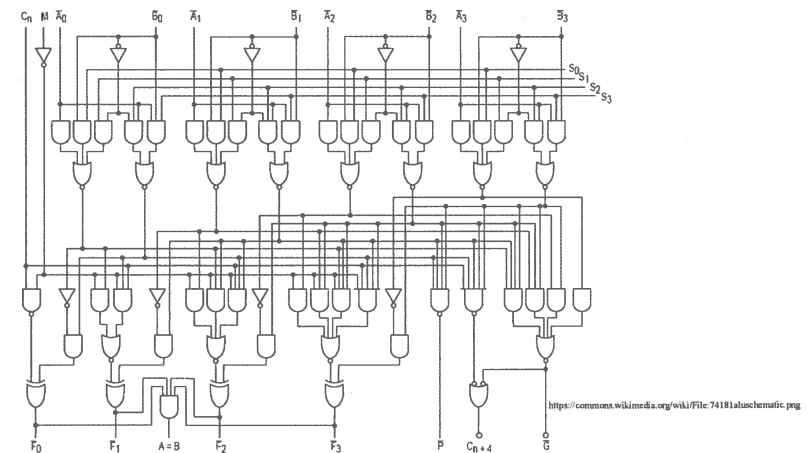
12 pins



- A. #primary inputs = # literals
 B. #gates = # operators
 C. #nets = #variables + # operators
 D. #pins = # literals + 2 * #operators - 1
 E. All of them

Based on CK Cheng - CSE140 Spr18

Logic Diagram/Schematics



- Logic circuit vs. Boolean Algebra Expression
- Simplify the Boolean expression: Reduce the complexity of the circuit

56