

1. Historical event

2. Digit

3. Complexity

10 variables $2^{10} = 10^3$

1000 " $2^{1000} \approx 10^{300}$

10⁷⁸ 82

Finger $\rightarrow 0-9 \rightarrow 0,1$ Binary #atoms

Introduction to Digital Logic Design

CSE 140: Components and Design Techniques for Digital Systems

Spring 2021

CK Cheng

Dept. of Computer Science and Engineering
University of California, San Diego

Hardware

Design

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Outlines

- Staff
 - Instructor, TAs, Tutors
- Logistics
 - Websites, Textbooks, Grading Policy
- Motivation *Chapter 1*
 - Moore's Law, Deep Learning, Quantum Computing
- Scope
 - Position among CSE courses
 - Coverage

Staff: the Instructor

- Instructor: CK Cheng
- Education: Ph.D. in EECS UC Berkeley
- Industrial Experiences: Engineer of AMD, Mentor Graphics, Bellcore; Consultant for technology companies
- Email: ckcheng+140@ucsd.edu
- Office: Room 2130 CSE Building
- Office hours
 - 3:00-4:00PM Monday; 2:00-3:00PM Wednesday
- Websites
 - <http://cseweb.ucsd.edu/~kuan>
 - <http://cseweb.ucsd.edu/classes/sp21/cse140-a>

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Staff: TAs and Tutors

- TAs
- Abraham, Elizabeth, email: eabraham@ucsd.edu
 - Holtz, Chester, email: chholtz@ucsd.edu
 - Hsu, Po-Ya, email: p8hsu@ucsd.edu
 - Ravindrakumar, Vaishakh, email: varavind@ucsd.edu
 - Wu, (Connie) Yen-Yi, email: yew001@ucsd.edu
- Tutor(s)
- Jang, (Tim) Wonsuk, email: w1jang@ucsd.edu
 - Serrano, Evan, email: e1serran@ucsd.edu
- Office hours will be posted on the course website (piazza)

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Logistics: Class Schedule

- Lecture: TR 12:30-1:50PM
- Discussion: F 3-350PM
- 5-6 Homework Assignments, 3 Exams
- The Third Exam: Due time M 230PM, 6/7/2021

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Logistics: Sites for the Class

- Class website
 - <http://cseweb.ucsd.edu/classes/sp21/cse140-a/index.html>
 - Index: Staff Contacts and Office Hrs
 - Syllabus
 - Grading policy
 - Class notes
 - Assignment: Homework and Reading Activities
 - Exercises: Solutions and Rubrics
- Forum (Piazza): Online Discussion *make sure you have access
- Score keepers: Gradescope, Canvas

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Logistics: Textbooks

Reserved at library

- Digital Design and Computer Architecture by David Money Harris and Sarah L. Harris, Morgan Kaufmann (Reading Activities)
- Digital Systems and Hardware/Firmware Algorithms, Milos D. Ercegovac and Tomas Lang (System Designs, pdf file will be released)

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Logistic: Class Expectation

- Level 1: Concepts and Methods (Lecture and slides)
 - Class attendance of video record
- Level 2: Hands on Practices (Exercises)
 - Homework
- Level 3: Command of Materials (Samples of exams)
 - Exams: Type 1
- Level 4: Extension and Exploration (Content beyond the textbook)
 - Exams: Type 2

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Logistics: Grading

Grade on style, completeness and correctness

- Homework: 25pts (grade based on a subset of problems)
- Exam 1: 25pts Week 4
- Exam 2: 25pts Week 7
- Exam 3: 25pts (due 230PM, Monday 6/7/2021)
- Grading: The better choice of the following two categories
 - Exact score (100pts)
 - A->93, A- >90, B+>87, B>83, B->80, C+>77, C>73
 - C- >50.
 - The curve (100% of class)
 - A+ top x% ($x < 5$)
 - (A,A-) top $33 \pm 2\%$; (B+,B,B-) top $66 \pm 2\%$

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Logistic: 3 Exams

Exams: Asynchronous exam taken within 48 hours

- Open book, notes, free to check websites
- Solution and grading policy will be posted after the exam.
- Exams are not cumulative but requires a good command of the previous exam content
- Two timeframe options for the class to decide
 - I. 80 minutes time frame: Finish the exam in 80 minutes after you start the exam.
 - II. 48 hours time frame: Deliver the result in 48 hours after the exam is posted.
- Exam schedule
 - I. Weekends
 - II. Weekdays

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Logistic: grading components

- Homework:
 - Due Monday night on gradescope
 - Group discussion is encouraged. However, we are required to write individually
 - Discount 10% loss of credit for each day after the deadline but no credit **after the solution is posted**.
 - Some parts will be graded by completion only
 - **Standard: Posted solutions and rubrics**

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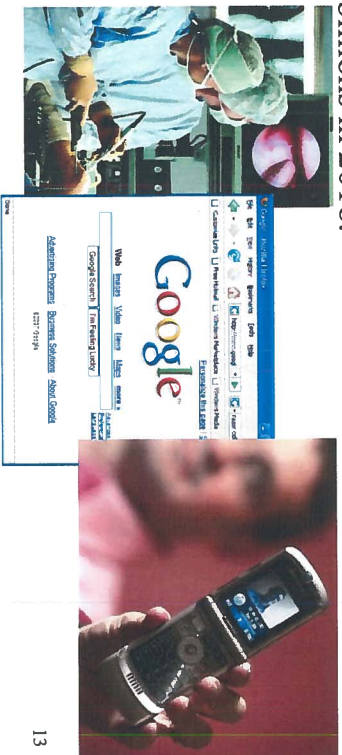
Course Problems...Cheating

- What is cheating?
 - Studying together in groups is not cheating but encouraged
 - Turned-in work must be *completely* your own.
 - Copying someone else's solution on a HW or Exam is cheating
 - Both “giver” and “receiver” are equally culpable
- We will be better off to work on the problem alone during the exam.
- We have to address the issue once the cheating is reported by someone (e.g. TA, Tutor, Student, etc.).

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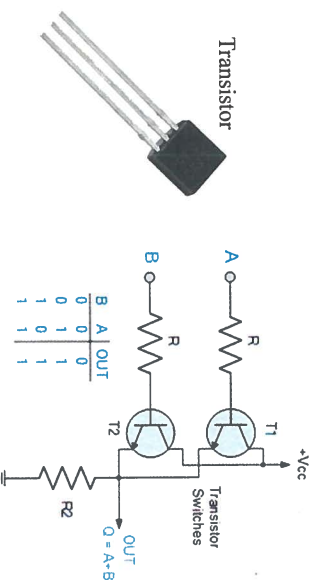
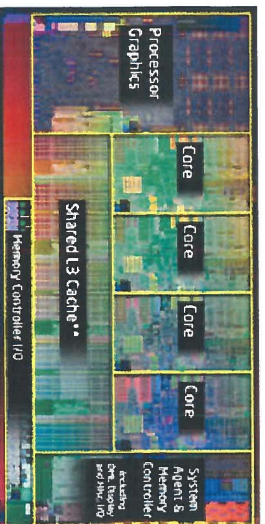
Motivation

- Microelectronic technologies have revolutionized our world: cell phones, internet, rapid advances in medicine, etc.
- The semiconductor industry has grown from \$21 billions in 1985, \$335 billions in 2015, to \$478 billions in 2018.



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Building complex circuits



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The Digital Revolution

Integrated Circuit: Many digital operations on the same material

Vacuum tubes

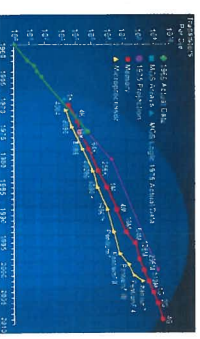


ENIAC



Integrated Circuit

Exponential Growth of Computation



Moore's Law

Stored Program Model

1949

1965

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Robert Noyce, 1927 - 1990

- Nicknamed "Mayor of Silicon Valley"
- Cofounded Fairchild Semiconductor in 1957
- Cofounded Intel in 1968
- Co-invented the integrated circuit



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Gordon Moore

- Cofounded Intel in 1968 with Robert Noyce.
- **Moore's Law:** the number of transistors on a computer chip doubles every 1.5 years (observed in 1965)

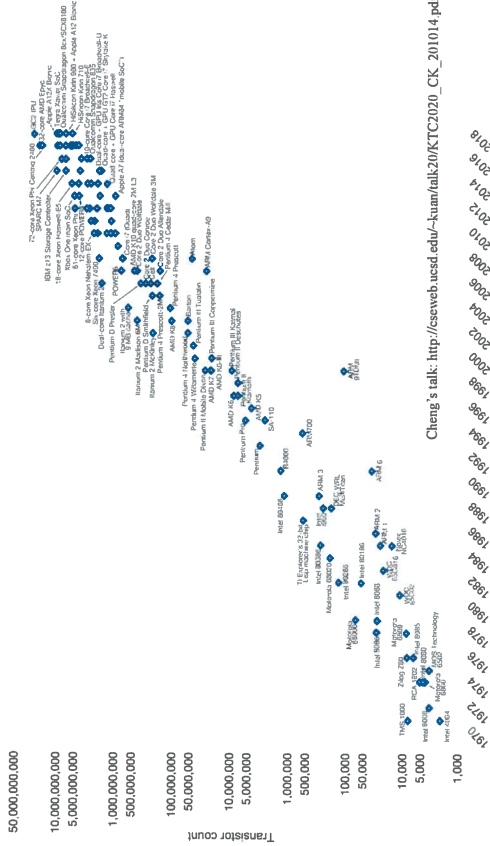


Introduction: Moore in 1965

The complexity for minimum component costs has increased at a rate of roughly a factor of two/yr.

Moore's Law – The number of transistors on integrated circuit chips (1971-2018)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.



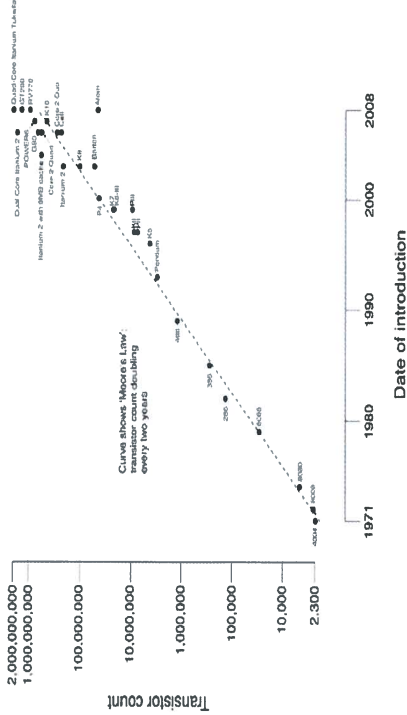
Cheng's talk: http://cseweb.ucsd.edu/~kuan/talk/20KTC2020_CK_201014.pdf

Data source: Wikipedia https://en.wikipedia.org/wiki/Transistor_count. The data visualization is available at [OurWorldIndata.org](https://ourworldindata.org). There you find more visualizations and research on this topic.

Licensed under CC-BY-SA by the author Max Roser.

Technology Trends: Moore's Law

CPU Transistor Counts 1971-2008 & Moore's Law



- Since 1975, transistor counts have doubled every two years.
- **Moore's law: wider applications: larger market: higher revenue: more R&D**

New Technologies

- New materials and fabrication for devices
 - Low power devices
 - Three dimensional integrated circuits
 - Graphene
- New architecture
 - Machine learning, deep learning
- Quantum computing

Understand the principles to explore the future

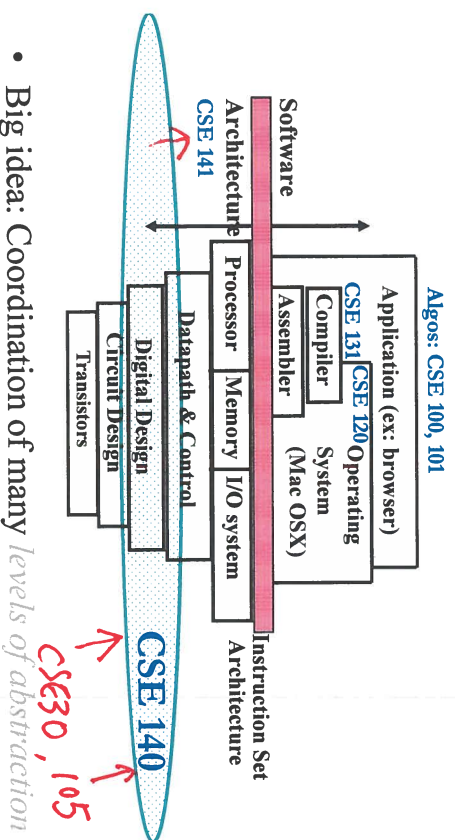
Artificial Intelligence

- Logic and Reasoning
- Boolean Satisfiability (SAT)
 - Product of sum clauses
 - Diagnosis
- States and Sequences
 - Sequential Machines
 - Reachability
 - Controllability

One example of the applications and opportunities

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Position among CSE Courses



- Big idea: Coordination of many levels of abstraction

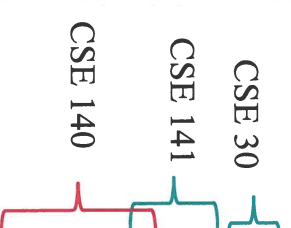
Dan Garcia®

Scope

- The purpose of this course is that we:
- Learn the principles of digital design
 - Learn to systematically debug increasingly complex designs
 - Design and build digital systems
 - Learn what's under the hood of an electronic component
 - Prepare for the future technology revolution

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Principle of Abstraction



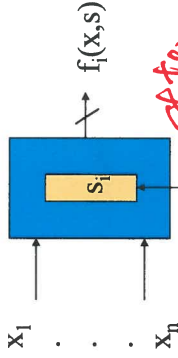
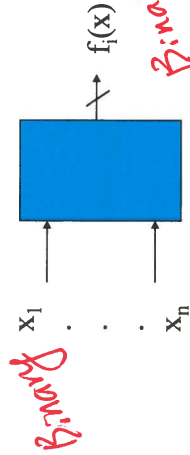
Application Software	programs
Operating Systems	device drivers
Architecture	instructions registers
Micro-architecture	datapaths controllers
Logic	adders memories
Digital Circuits	AND gates NOT gates
Analog Circuits	amplifiers filters
Devices	transistors diodes
Physics	electrons

Abstraction: Hiding details when they are not important

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Scope: Overall Picture of CS140

Combinational Logic vs Sequential Network



Combinational logic:

$$y_i = f_i(x_1, \dots, x_n)$$

Boolean algebra

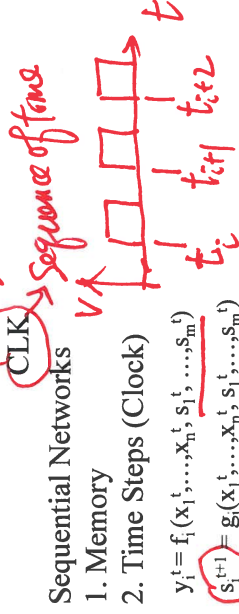
Sequential Networks

1. Memory

2. Time Steps (Clock)

$$y_i^t = f_i(x_1^t, \dots, x_n^t, s_i^t, \dots, s_m^t)$$

$$s_i^{t+1} = g_i(x_1^t, \dots, x_n^t, s_i^t, \dots, s_m^t)$$



Finite State Machine

Scope

Subjects	Building Blocks	Theory
Combinational Logic	AND, OR, NOT, XOR	Boolean Algebra
Sequential Network	AND, OR, NOT, FF, ~~Flip-Flop~~	Finite State Machine
Standard Modules	Operators, <u>Interconnects</u> , Memory	Arithmetics, Universal Logic
System Design	Data Paths, Control Paths	Methodologies

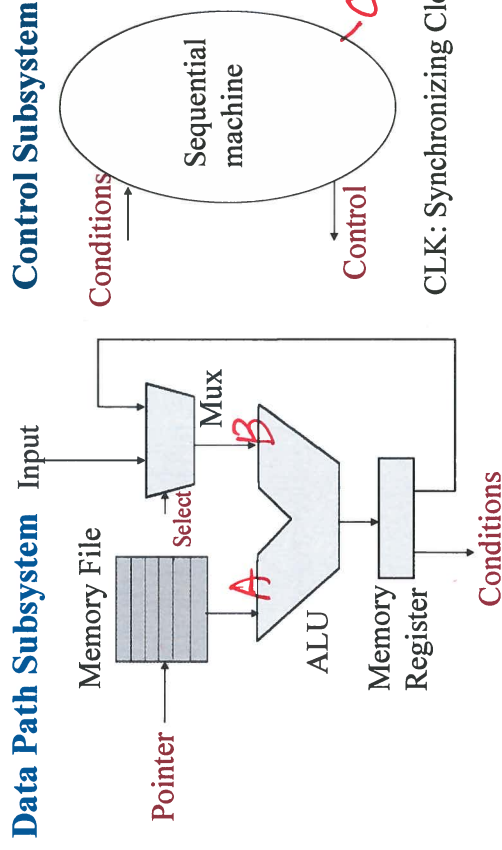
Ex 1

Ex 2

Ex 3

↓

CPU ASIC



BSV: Design specification and modular design methodology²⁶

A > B

A < B

=

Overflow

Combinational Logic Basics

What is a combinational circuit?

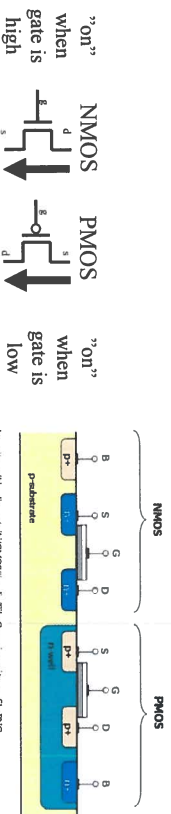
- No memory
- Realizes one or more functions
- Inputs and outputs can only have two discrete values
 - Physical domain (usually, voltages) (Ground 0V, Vdd 1V)
 - Mathematical domain : Boolean variables (True, False)

Differentiate between different representations:

- physical circuit
- schematic diagram
- mathematical expressions

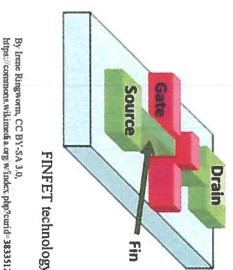
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Basic CMOS



Planar technology

- Complementary Metal Oxide Semiconductor
- Invented in the 1960's, but took over in the 80's
- "on" means low resistance, "off" means high resistance
- Logic "1" and Logic "0" values are arbitrary e.g. logic "1" == 1.0 V, logic "0" == 0.0 V



By: James R. Ruppert, CC BY-SA 3.0
<https://commons.wikimedia.org/wiki/File:FinFET.jpg?curid=3833312>

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Binary Digital Logic

- Simplest representation is "1" and "0" (base-2).
- Choose a physical quantity to represent "1" and "0"
 - Usually voltage, but not always (e.g. current, resistance, magnetic polarization, quantum spin, ...)
- Use a transistor to make the switch (operating as a digital instead of analog device)
 - Two states – on / off
 - Signals can be high voltage ("1") or low voltage ("0")

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Transistors as Switches

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